A Bit-by-Bit Re-Writable Eflash in a Generic Logic Process for Moderate-Density Embedded Non-Volatile Memory Applications

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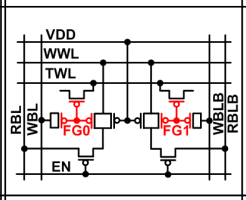
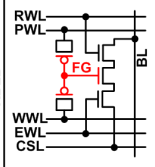
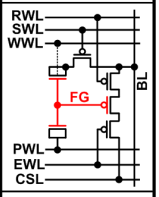
***Abstract*- A bit-by-bit re-writable embedded flash memory is demonstrated in a generic 65nm logic process for moderate-density embedded non-volatile memory applications. The proposed 6T embedded flash memory cell improves the overall cell endurance by eliminating redundant program/erase cycles without disturbing cells in the unselected wordlines. A multi-story high voltage switch utilizes four boosted supply levels generated by a compact voltage doubler based on-chip negative charge pump.**

I. Introduction

Embedded Non-Volatile Memory (ENVM) technology has been employed in a number of applications such as post-silicon tuning, memory repair, on-line field test, and secure ID storage [1-6]. ENVM is also a critical component for self-healing applications where information regarding time dependent failure mechanisms such as circuit aging must be retained during system power off periods. Anti-Fuse One-Time-Programmable (AF-OTP) NVM memory [1, 2] has been extensively used for memory repair in standard logic processes; however, it does not allow the cell to be re-programmed after the anti-fuse has been programmed. Moreover, the Charge Pump (CP) has to provide a relatively large program current which incurs a significant area overhead. A single-poly embedded flash (eflash) memory, on the other hand, utilizes Fowler-Nordheim tunneling [3-6] which can support multiple program and erase operations (e.g., >1000 times) without a significant program current.

Table I compares the key features of the various single poly eflash memories. The 10T differential eflash cell [4] stores both the true and complementary values for high voltage margin at the expense of a large cell size and is capable of a bit-by-bit write; however, the high write voltage (VPP) and write protection voltage (hVPP) are applied to the BL's during the write operation which results in disturbance issues in the unselected WL cells. Another prior WL-by-WL erasable eflash [6] does not require boosted BL's, allowing disturbance free erase and program operations for multiple unselected WL's; however, it cannot erase the cell data on a bit-by-bit basis, as every cell on a selected WL is exposed to a high voltage stress and is erased simultaneously prior to the program operation. This inadvertently results in some '0' cells being cycled unnecessarily (Fig. 1). Since only 32 out of 128 cells are updated at a time, for a 32b data bus and a 128 cells/WL architecture, the '0' cells in the unselected columns and some '0' cells in the selected columns are unnecessarily erased to '1' state and then programmed again to '0' state. Thus, the overall cell endurance can be severely impacted especially when only a small fraction of the stored data needs to be updated frequently.

TABLE I. Single Poly Eflash Memory Options

Logic Eflash	10T Eflash [4]	5T Eflash [6]	6T Eflash (This Work)
Unit Cell Schematic			
Process	0.18μm Logic	65nm Logic	65nm Logic
Tunnel Oxide	~7nm	~5nm	~5nm
Write Method	FN Tunneling	FN Tunneling	FN Tunneling
Write Voltage	10V	10V	-7.2V
Unsel. WL's	Disturbed	Not Disturbed	Not Disturbed
Bit-by-Bit Write	Supported	Not Supported	Supported
Capacity	192b	2kb	4kb
Cell Size	220μm^2	8.62μm^2	15.3μm^2

Prior WL-by-WL erasable single-poly eflash [6]

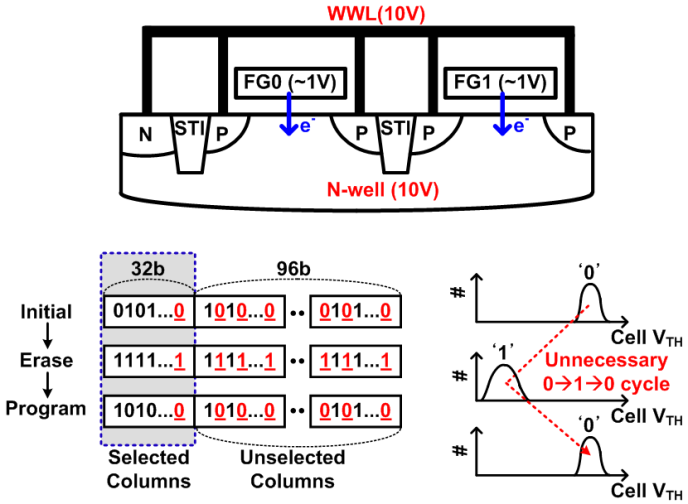


Fig. 1. In prior WL-by-WL erasable eflash memories, high voltage is applied to the tunnel oxide in the entire cells of the selected WL, causing an electron tunneling from the floating gate, which adds an unnecessarily erase/program cycle for the unchanged '0' cells in the selected and unselected columns.

To improve the overall cell endurance characteristic without disturbing multiple unselected WL's, we present a fully logic-compatible eflash memory capable of writing data on a bit-by-bit basis without utilizing boosted BL voltages by applying high voltages to the selected cell tunnel oxide in a

bit-by-bit manner via selective FG boosting technique. It eliminates the aforementioned redundant cycling issue in the proposed 6T eflash cell which consists of a coupling transistor (M_1), a program transistor (M_2), a read transistor (M_3), and three select transistors (S_1-S_3). The proposed bit-by-bit re-writable eflash memory includes a 4kb eflash cell array, a multi-stage negative CP, multi-story High Voltage Switches (HVS), and low voltage Sense Amplifiers (SA) & BL drivers and was implemented using 1.2V core and 2.5V I/O transistors readily available in a standard CMOS process (Fig. 2).

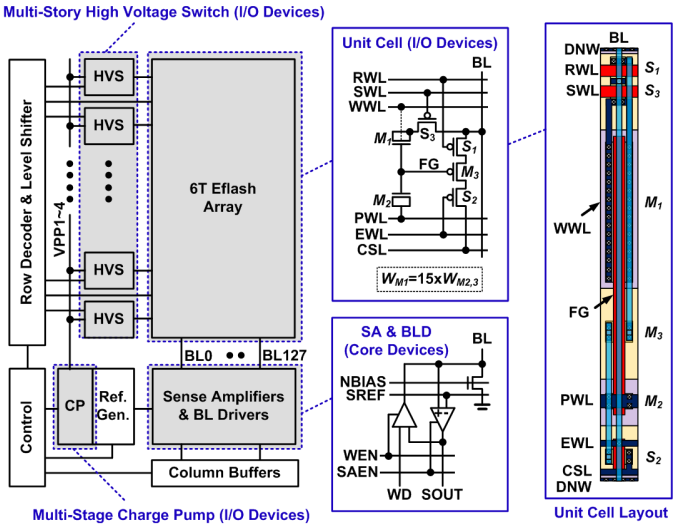


Fig. 2. Proposed bit-by-bit re-writable embedded flash memory including 6T cell array, charge pump, high voltage switch, sense amplifiers & BL drivers was implemented using core and I/O devices in a standard CMOS process.

II. Proposed Eflash Cell for Bit-by-Bit Write

To enable a bit-by-bit write, the proposed eflash cell boosts the floating gate (FG) of the each cell selectively via preferential coupling as illustrated in Fig. 3. Compared to the prior WL-by-WL erasable eflash (Fig. 1), the proposed cell does not share the source and drain node (SD) between adjacent cells in the WL direction, allowing it to have different voltage levels for each bit cell in the same WL. During write operations of the proposed eflash, WWL is switched to the negative boosted voltage (i.e. -7.2V), making FG node of '0' BL cell coupled down greater than the FG node of '1' BL cell. This is because the select TR (S_{3A} in Fig. 4) of '0' BL cells is turned off and the source and drain node of '0' BL cells (SD0) is floated, while the select TR (S_{3B} in Fig. 4) of '1' BL cells is turned on and the source and drain node of '1' BL cells (SD1) is tied to VDD (i.e. 1.2V). This FG node voltage difference can be utilized for the bit-by-bit write operations of the proposed 6T eflash cell.

The bias conditions for bit-by-bit write operations of the proposed 6T eflash cell are illustrated in Fig. 4. During write '0' phase (Fig. 4 top), PWL is switched to 1.6V and the large voltage difference between FG0 and PWL node enables only '0' BL cells to be selectively written to '0' states, making lose electrons from FG. During write '1' phase (Fig 4 bottom), PWL is switched to -7.2V and the large voltage difference between FG1 and PWL nodes enables only '1' BL cells to be selectively written to '1' states, making gain electrons in FG.

Fig. 5 shows a read bias condition where the '1' cell flows higher current than '0' cell, raising BL voltage level above the SA reference (SREF). The read reference level (VRD) is provided through multi-story HVS in the WL driver (Fig. 8). The negative boosted writing voltage associated with NMOS coupling transistor (M_1) enables non-negative VRD levels, while not inverting the coupling transistor (M_1) with a floating channel during read operation. The overall bit-by-bit data update sequence of the selected WL can consist of the original eflash data read from the selected WL to column buffers (step 1), modify the column buffers to new data (step 2), and conduct write '0' and '1' phases (step 3).

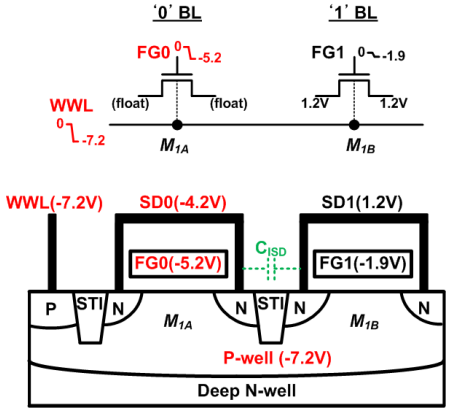


Fig. 3. Selective FG boosting is enabled by the preferential coupling for '0' BL cells where the source and drain node (SD0) of the coupling transistor (M_{1A}) is floated, while the corresponding node (SD1) for '1' BL cells is tied to VDD (1.2V). The differently boosted FG voltage levels for '0' and '1' BL's are utilized for the bit-by-bit electron tunneling occurred in the program transistor M_{2A}, M_{2B} (shown in Fig. 4) during write operations.

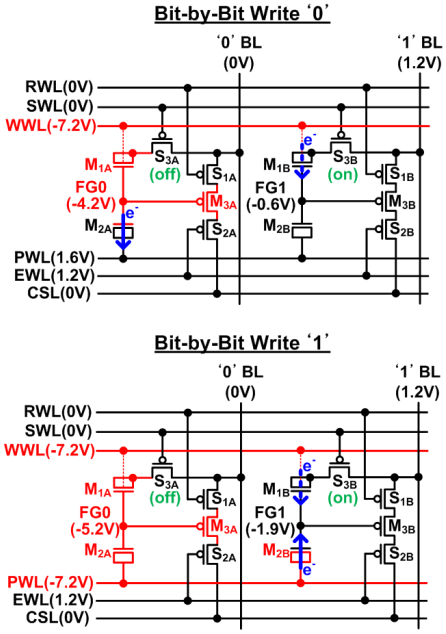


Fig. 4. Bias conditions for bit-by-bit write operations of the proposed 6T eflash cell. '0' BL cell loses electrons from FG during bit-by-bit write '0' operation, while '1' BL cell gains electrons in FG during bit-by-bit write '1' operation.

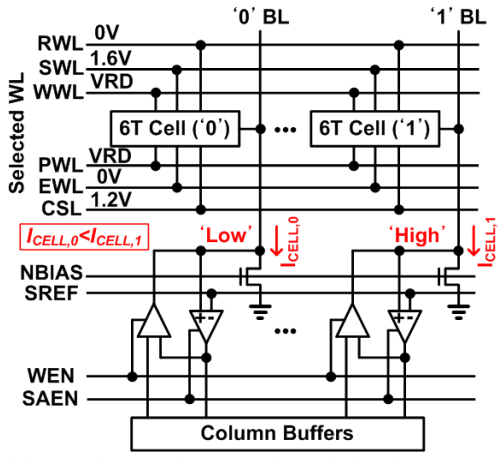


Fig. 5. Read bias condition of the proposed 6T eflash cell.

III. Negative Charge Pump and High Voltage Switch

The proposed 6T eflash cell requires a negative high voltage to be applied to WWL/PWL in the selected WL during write operations. In this work, a compact voltage doubler circuit [7] was cascaded to generate multiple negative supply levels VPP1-VPP4 (Fig. 6). Parasitic metal-to-metal capacitors (C_M) were utilized for the pumping capacitors. The write voltage level (VPP4) is regulated by comparing the resistively divided voltage level against a reference voltage (REF) and gating on or off the pumping clock. A deep n-well surrounds the VPP1-VPP4 p-wells for isolation purposes. All the devices are 1.2V core and 2.5V I/O devices provided in 65nm standard logic process. The measured CP output characteristic shows a reliable output voltage beyond the typical cell write current range (<1μA) (Fig. 7).

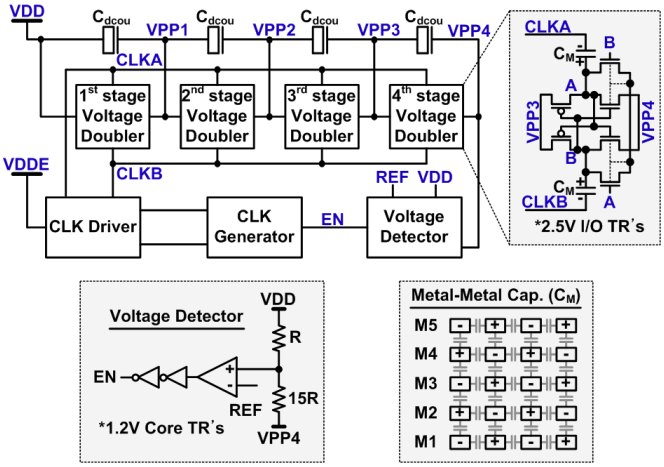


Fig. 6. Voltage doubler based negative charge pump generating VPP1-VPP4 levels is implemented in a 65nm standard logic process.

The proposed multi-story negative HVS, a refined version of the positive HVS presented in [6], utilizes the boosted negative supply levels VPP1-VPP4 (Fig. 8). All TR's in this HVS are implemented using 2.5V standard I/O devices. When SEL switches from VPP1 to VDD, nodes C and E are pulled-down to VPP3 and VPP2, and nodes A, B, D are pulled-up to VPP3, VPP2 and VPP1, respectively, making intermediate node 'M' and output node WWL/PWL are connected to VPP3 and VPP4 levels, respectively. When SEL switches from VDD to VPP1, nodes C and E are pulled-up to VPP2 and VPP1, and nodes A, B, D are pulled-down to VPP4, VPP3 and VPP2, respectively. As a result, node 'M' and the output node WWL/PWL are driven to VPP1 and VRD/VSS. Similar to the previous HVS design [6], the pulse width and transistor sizes are optimized such that the intermediate latch states switch reliability while static power consumption kept small so as to minimize the current load to CP. The measured waveforms (Fig. 9) show VPP4 signal generated from the CP and WWL/PWL signals applied to the selected WL via the designed HVS for a bit-by-bit write '0' operation.

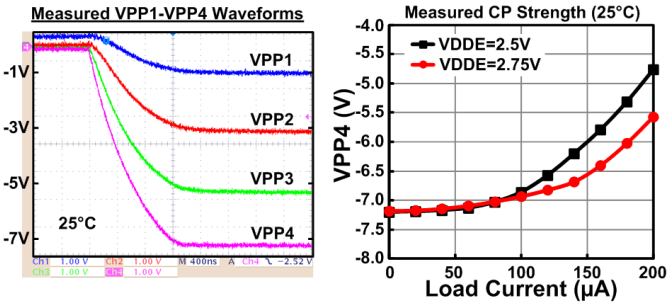


Fig. 7. Measured output characteristic of the voltage doubler based negative charge pump.

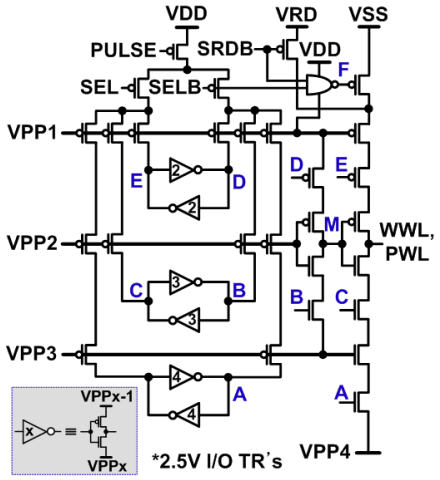


Fig. 8. Multi-story negative HVS implemented in a standard logic process.

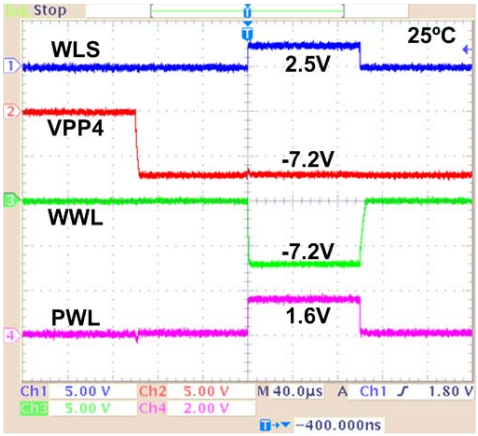


Fig. 9. Measured CP and HVS waveforms for a bit-by-bit write '0' pulse.

IV. Eflash Test Chip Results

A 4kb eflash test macro was implemented in a 65nm low power standard CMOS logic process. Fig. 10 shows the measured bit-by-bit write '0'/'1' phases and disturbance characteristic of the proposed 6T eflash cell. The inhibited '1' BL cells are disturbed increasing the cell V_{TH} and the sensing margin during bit-by-bit write '0' phase, while no apparent disturbance in the inhibited '0' BL cells is observed during bit-by-bit write '1' phase. Table II shows various write patterns tested in this work producing the different inter-cell SD capacitance (C_{ISD} in Fig. 3) values. The measurement result shows that (0101) pattern needs 10× more pulses than (0000) pattern to complete the write '0' phase, as higher C_{ISD} reduces the boosting effect of FG node of '0' BL cell, slowing down the write '0' speed. Fig. 11 shows the measured cell endurance and retention characteristic. The die photograph and feature summary of the fabricated test chip are shown in Fig. 12.

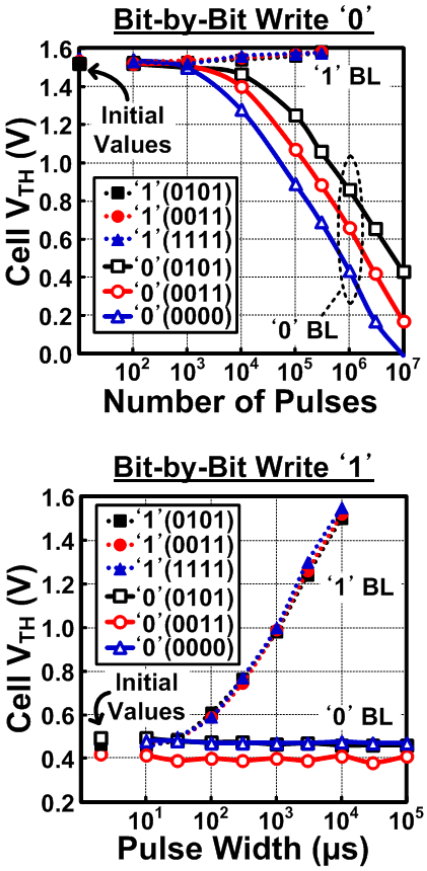


Fig. 10. Measured bit-by-bit write '0'/'1' phase and disturb results.

Table II. Test pattern dependency of the inter SD coupling (C_{ISD})

Pattern Name	BL # 0	1	2	3	•••	C_{ISD}
(1111)	1	1	1	1	•••	0
(0101)	0	1	0	1	•••	++
(0011)	0	0	1	1	•••	+
(0000)	0	0	0	0	•••	0

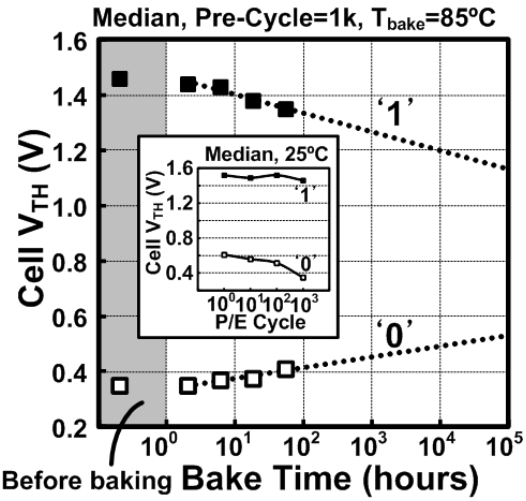
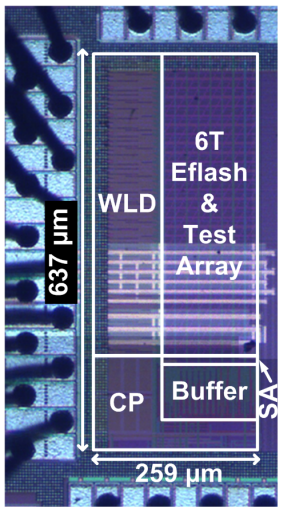


Fig. 11. Measured cell endurance and retention characteristic of the proposed 6T eflash cells.



Process	65nm LP CMOS
Main Feature	Bit-by-bit Re-Writable 6T Eflash
Supply Voltage	1.2V (Core), 2.5V (I/O)
Tunnel Oxide	5nm (I/O)
Array Dimension	32 WL, 128 BL
Unit Cell Area	15.3μm^2
CP Area	0.0214mm^2

Fig. 12. Die photograph and chip summary.

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