A Fully-Digital Beat-Frequency Based ADC Achieving 39dB SNDR for a 1.6mV$_{pp}$ Input Signal

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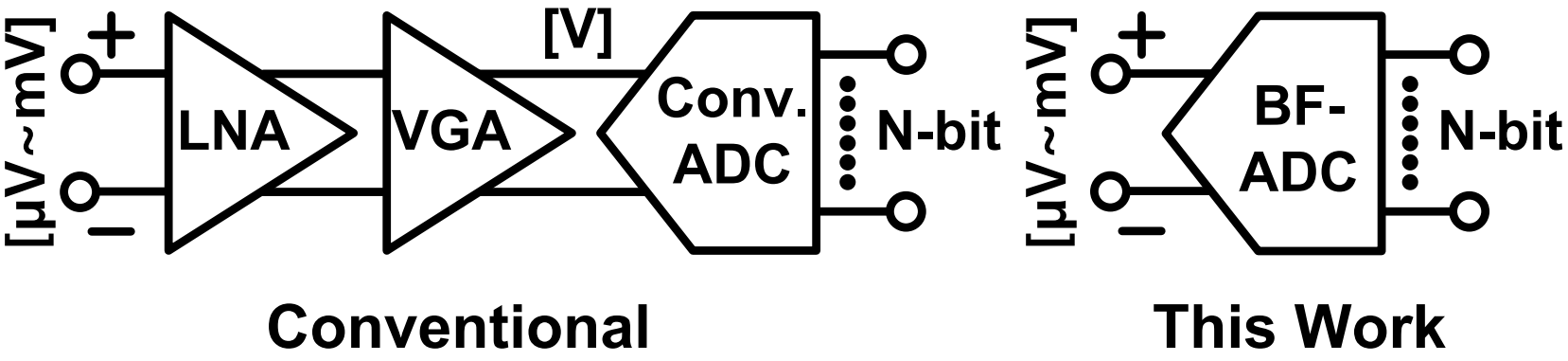
Agenda

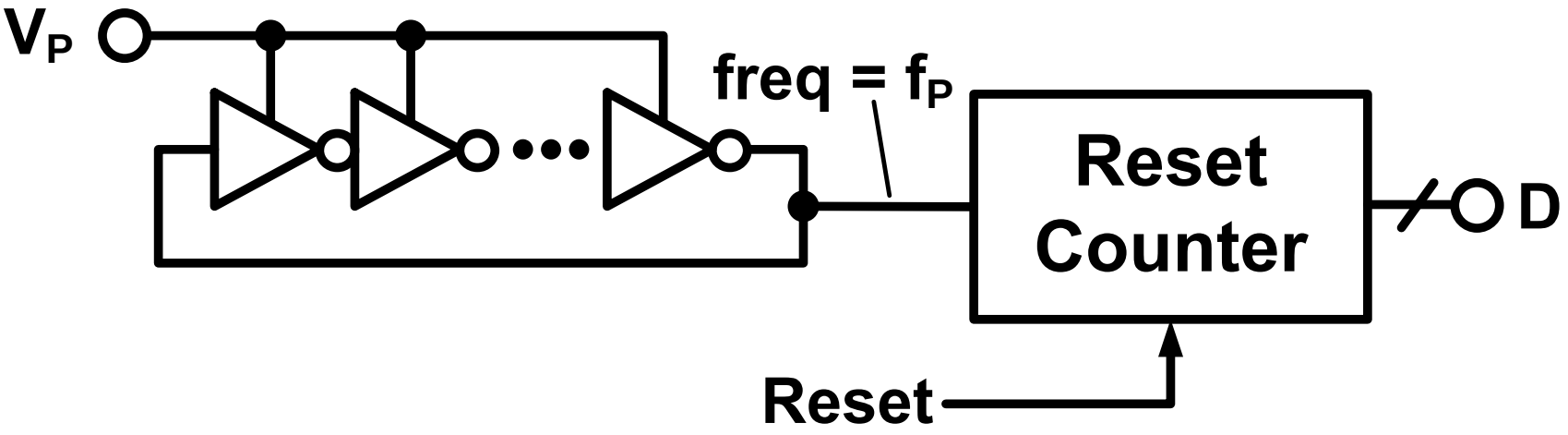
- **Motivation**
- **Conventional VCO-based ADC**
- **Proposed beat freq.(BF) based ADC**
- **65nm BF-ADC test chip configuration**
- **Measurement results**
- **Conclusion**

Data Acquisition Systems w/ Low Input Range : Conventional vs. This Work



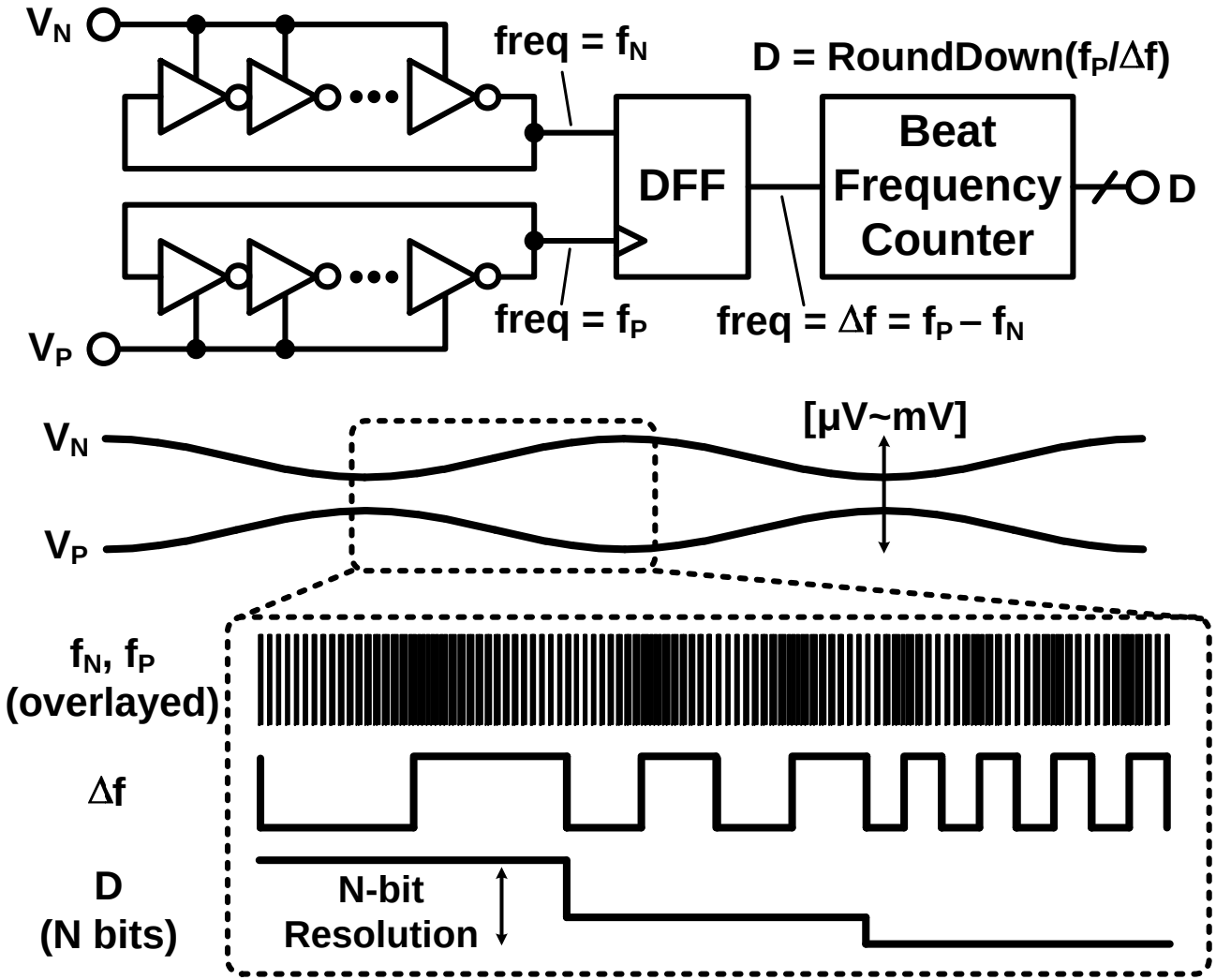
- **Conventional**
  - **Signal amplification w/ low-noise (LNA/VGA)**
  - **Conventional ADC for rail-to-rail input range**
- **This Work (BF-ADC)**
  - **Direct A-to-D conversion w/o signal amplification**

Conventional VCO-based ADC



- **Linear freq. detection using VCO and linear counter**
- **1st-order delta-sigma**
  - **Sigma (integrator) : VCO**
  - **Delta (differentiator) : Reset counter**

Proposed Beat Frequency Based ADC



- **High-resolution Beat frequency (BF) detection [1]**

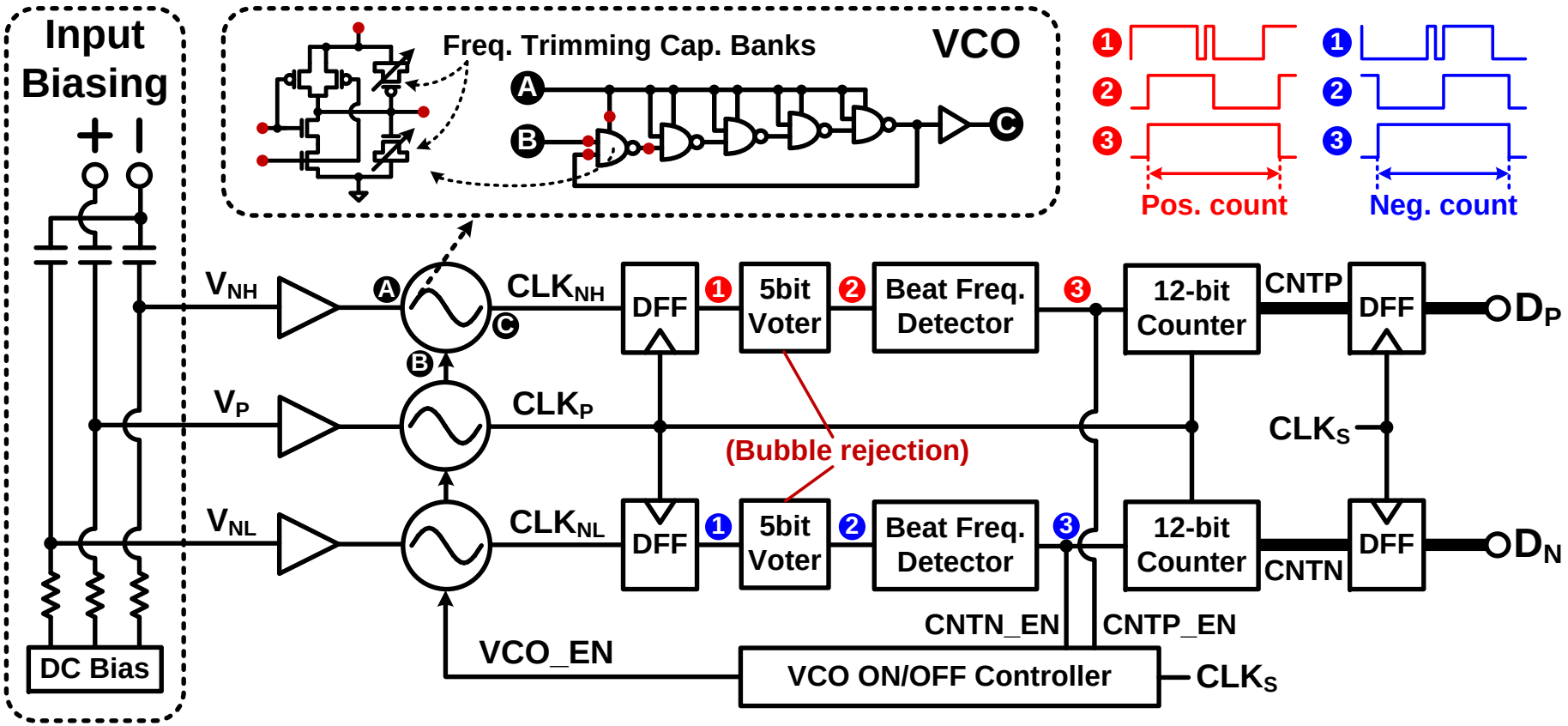
[1] T. Kim et al., VLSI Circuit Symposium 2007

Conv. VCO-based ADC vs. BF-ADC

	Conv. VCO-based ADC	Proposed BF-based ADC
ADC Type	Delta-sigma	Nyquist rate
Main Feature	1^{st}-order noise-shaping	Beat frequency detection
Input Range	Large [V]	Small [μV~mV]
VCO Linearity	Nonlinear K_{VCO} (large range)	Linear K_{VCO} (small range)
Key Circuit Block	VCO + linear counter	VCO + beat freq. counter
Counting Period	Fixed sample period	Variable beat freq. period
Sampling Rate	High speed [MS/s]	Low speed [kS/s]
Reconfigurability	No	Reconfigurable resolution
Applications	Wireless receiver [6, 7]	Sensor applications

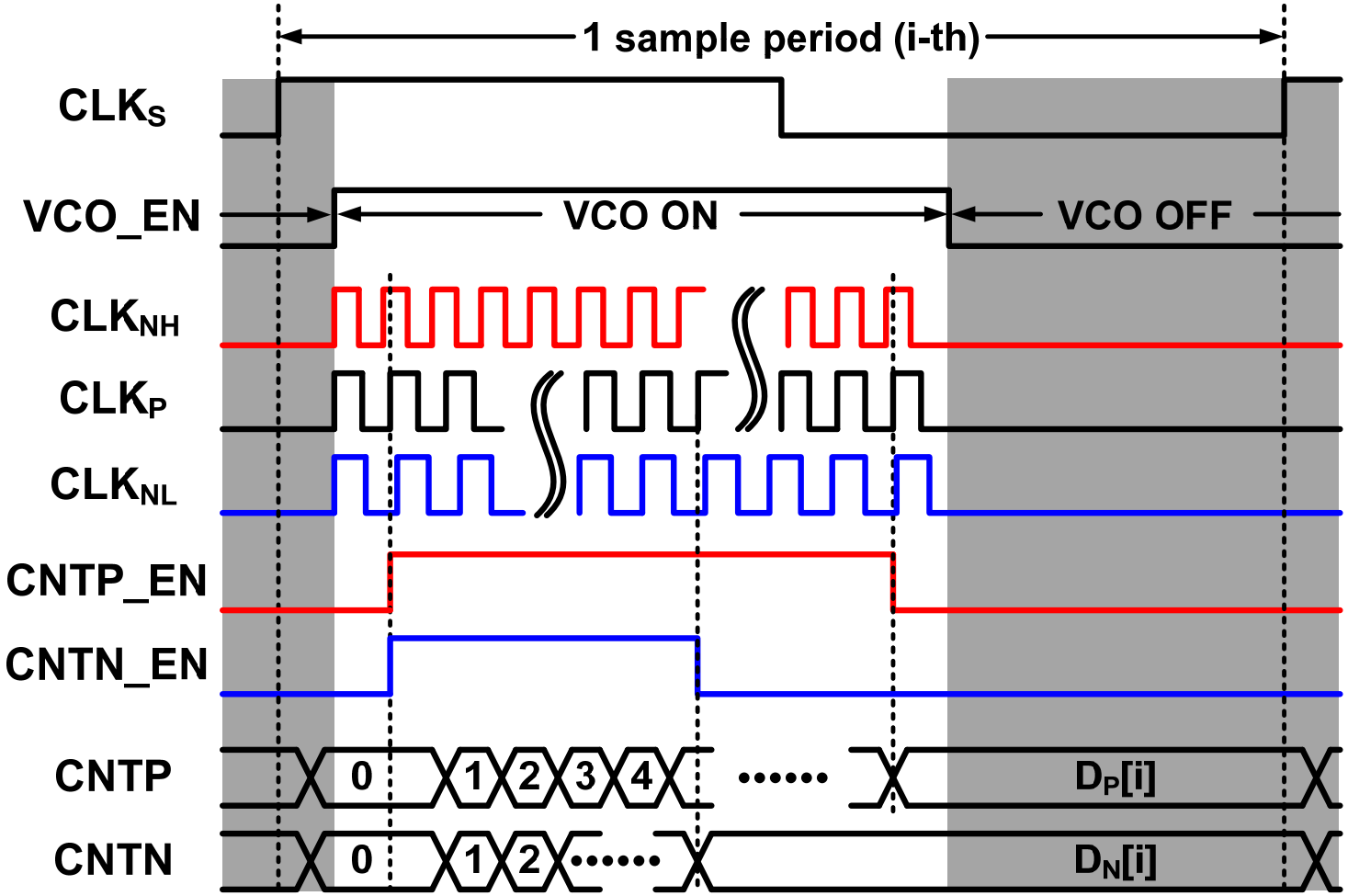
- **BF-ADC can be used for high-resolution sensors**

65nm BF-ADC Test Chip Configuration



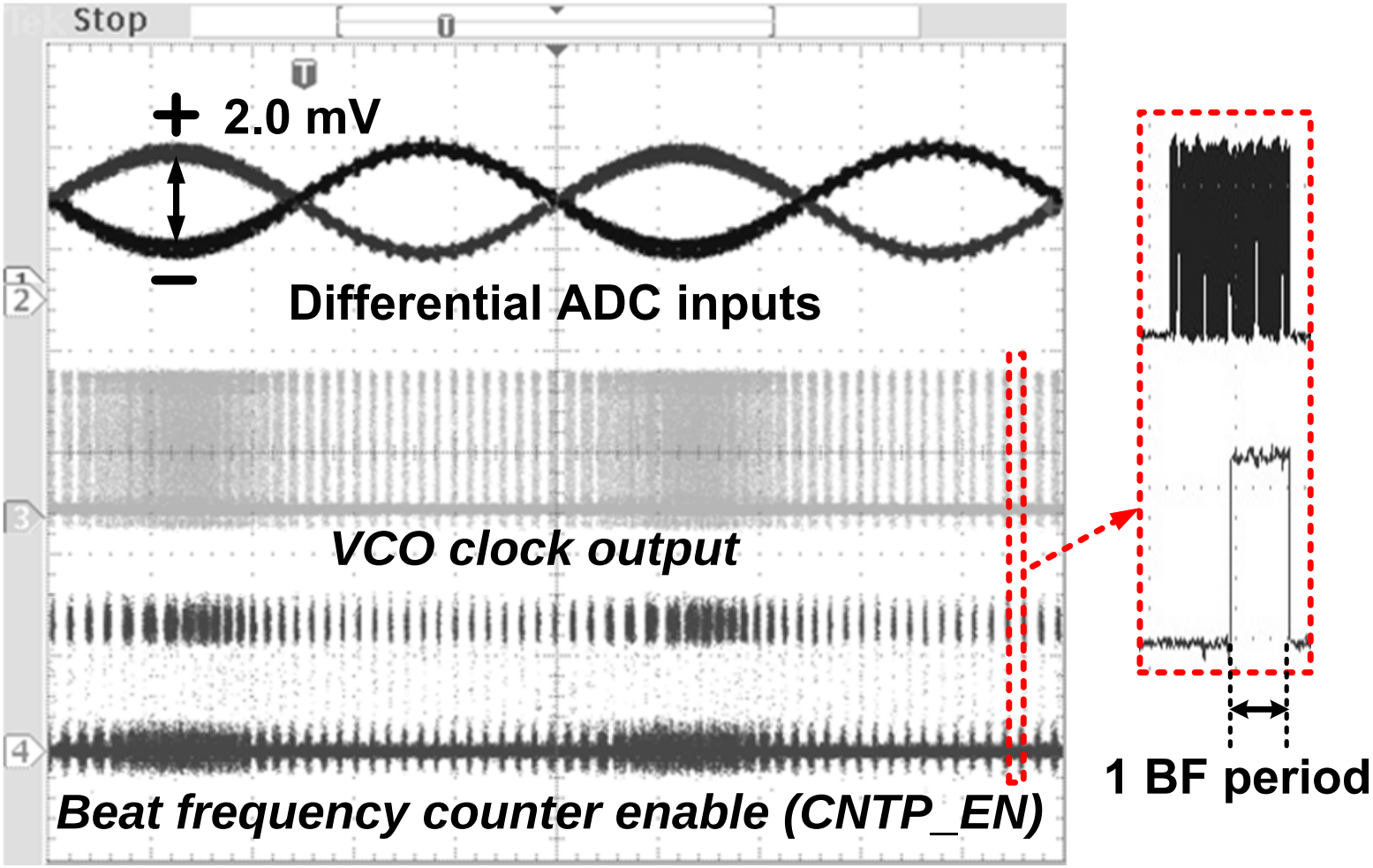
- Dual-reference BF-ADC for improved resolution
- VCO: 5-stage NAND w/ programmable cap. banks
- Positive/negative beat frequency detections

BF-ADC Timing Diagram



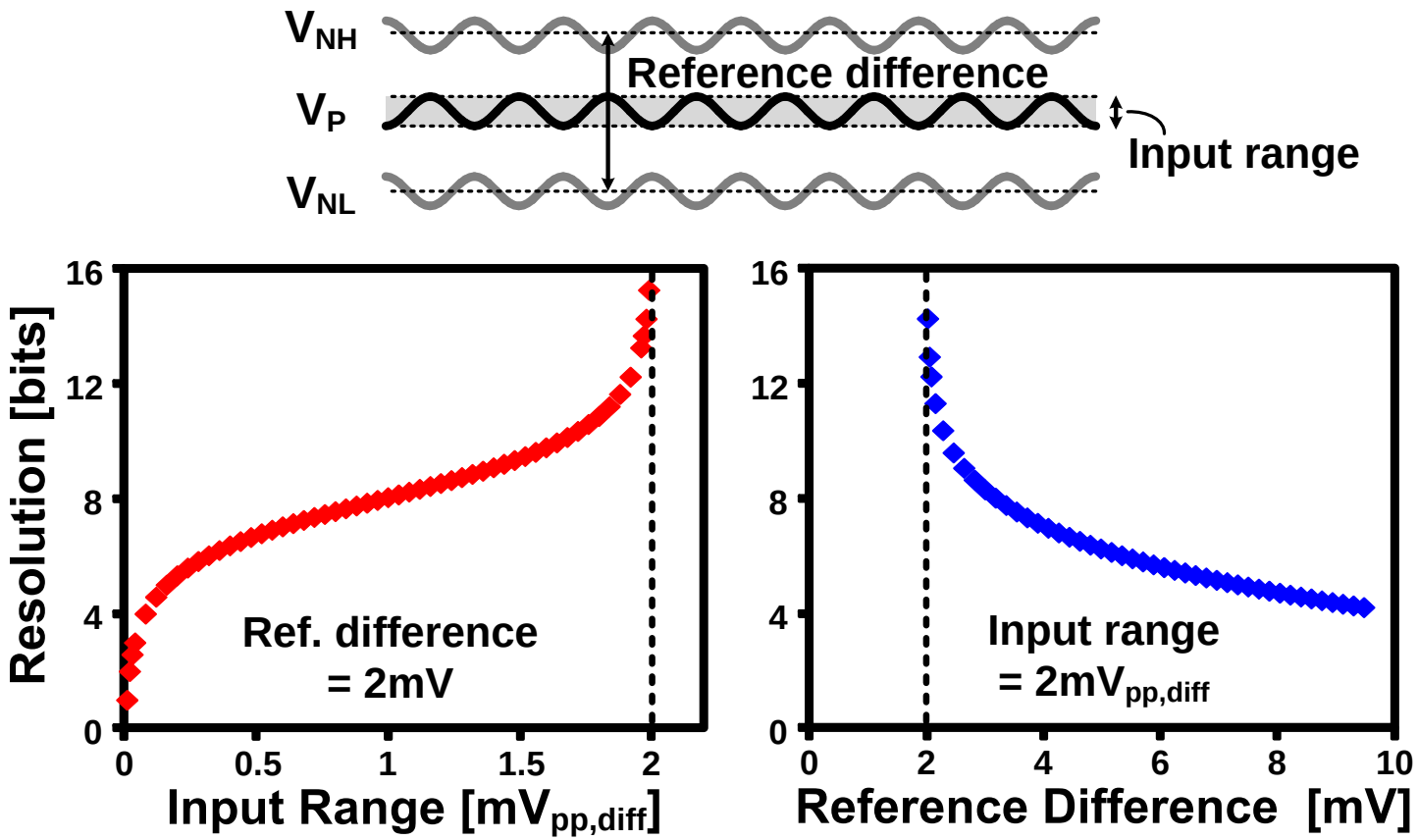
- Timing diagram for 1 sampling period of BF-ADC
- VCOs are turned off once the sampling is complete

Measured BF-ADC Waveforms



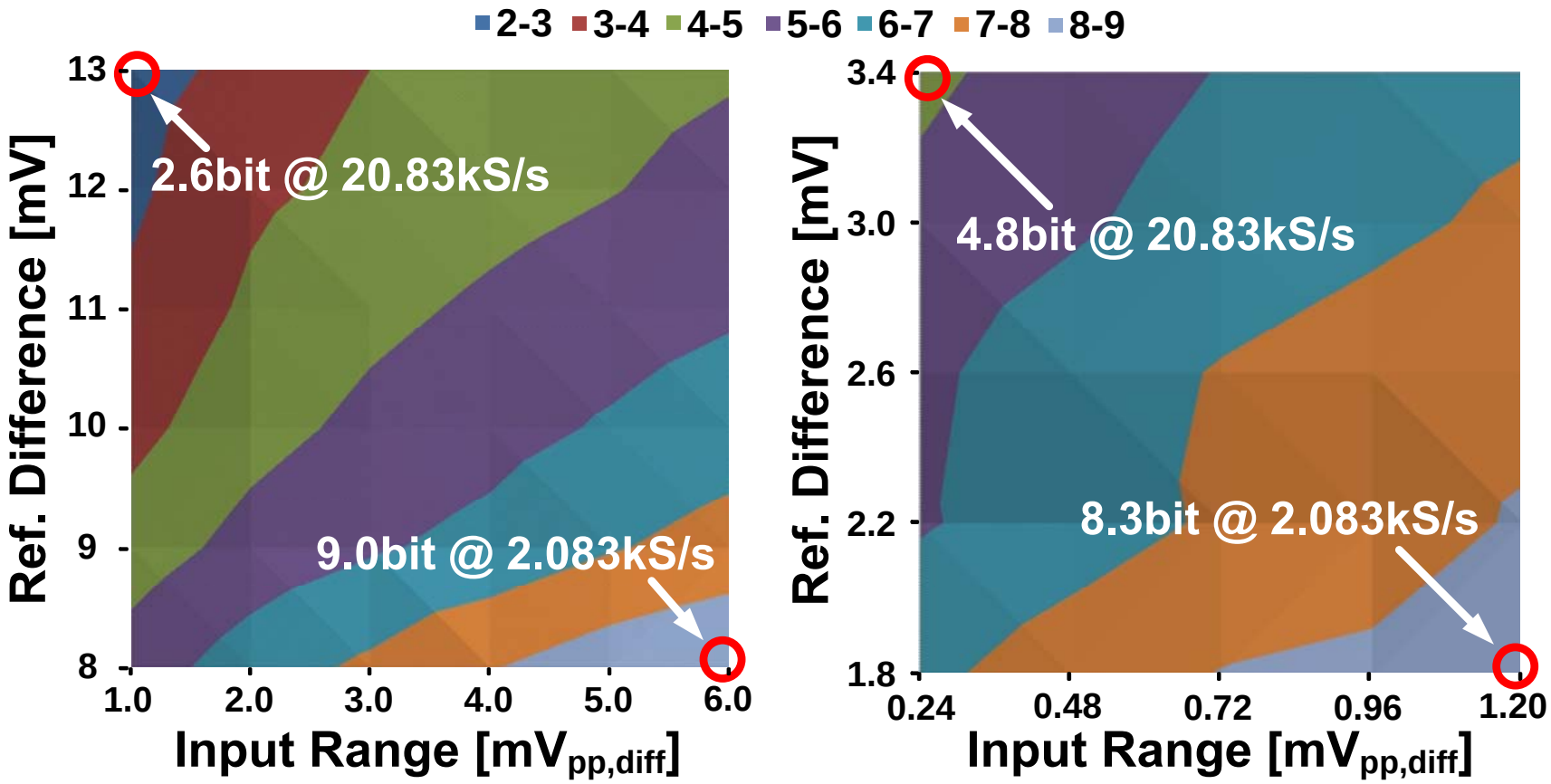
- 4mVppd BF-ADC inputs, VCO clock and BF signal

Resolution vs. BF-ADC Parameters



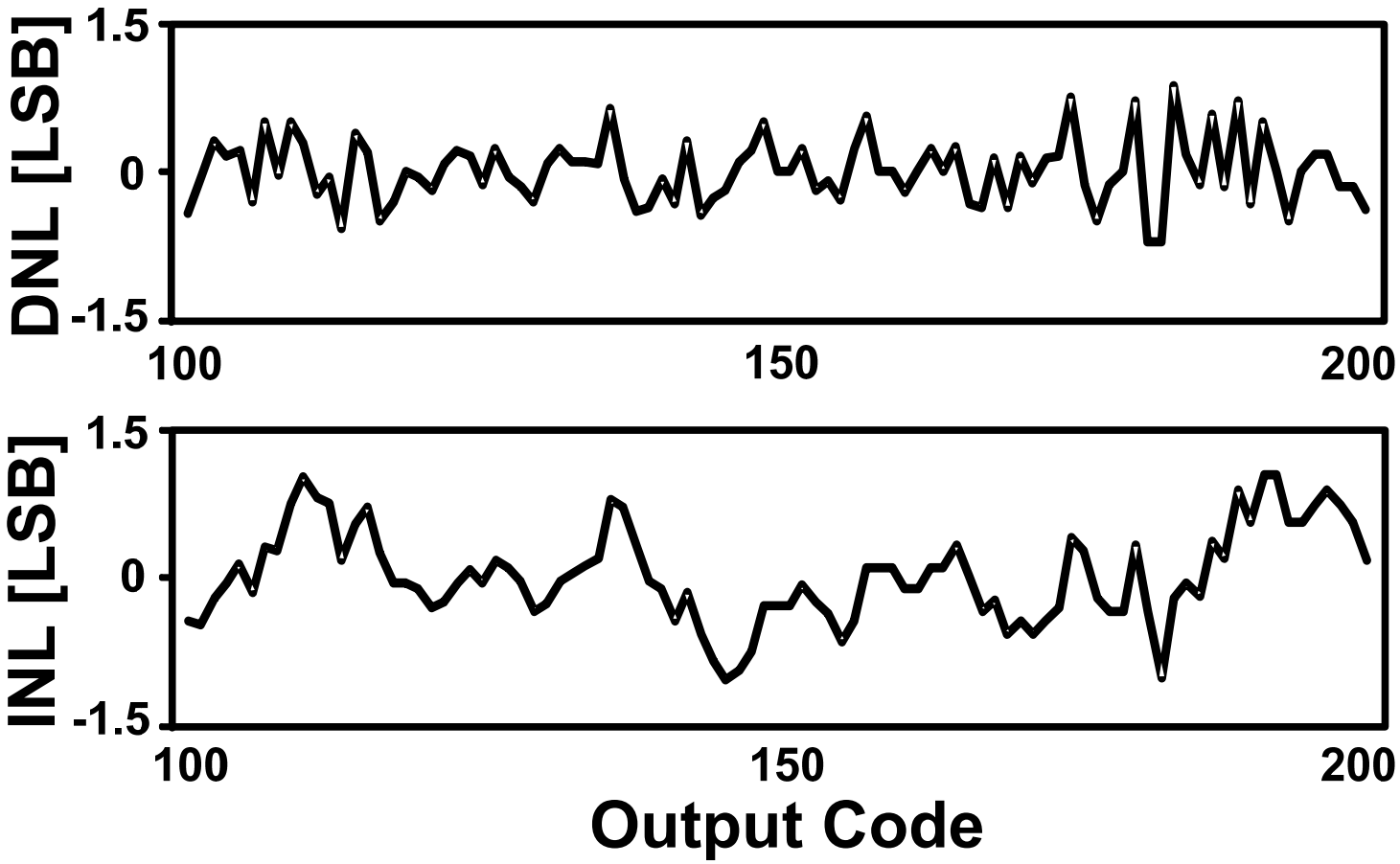
- **Resolution increases as input range and reference difference approaches each other**
- **In practice, ENOB is limited by noise levels**

Measured BF-ADC Resolution



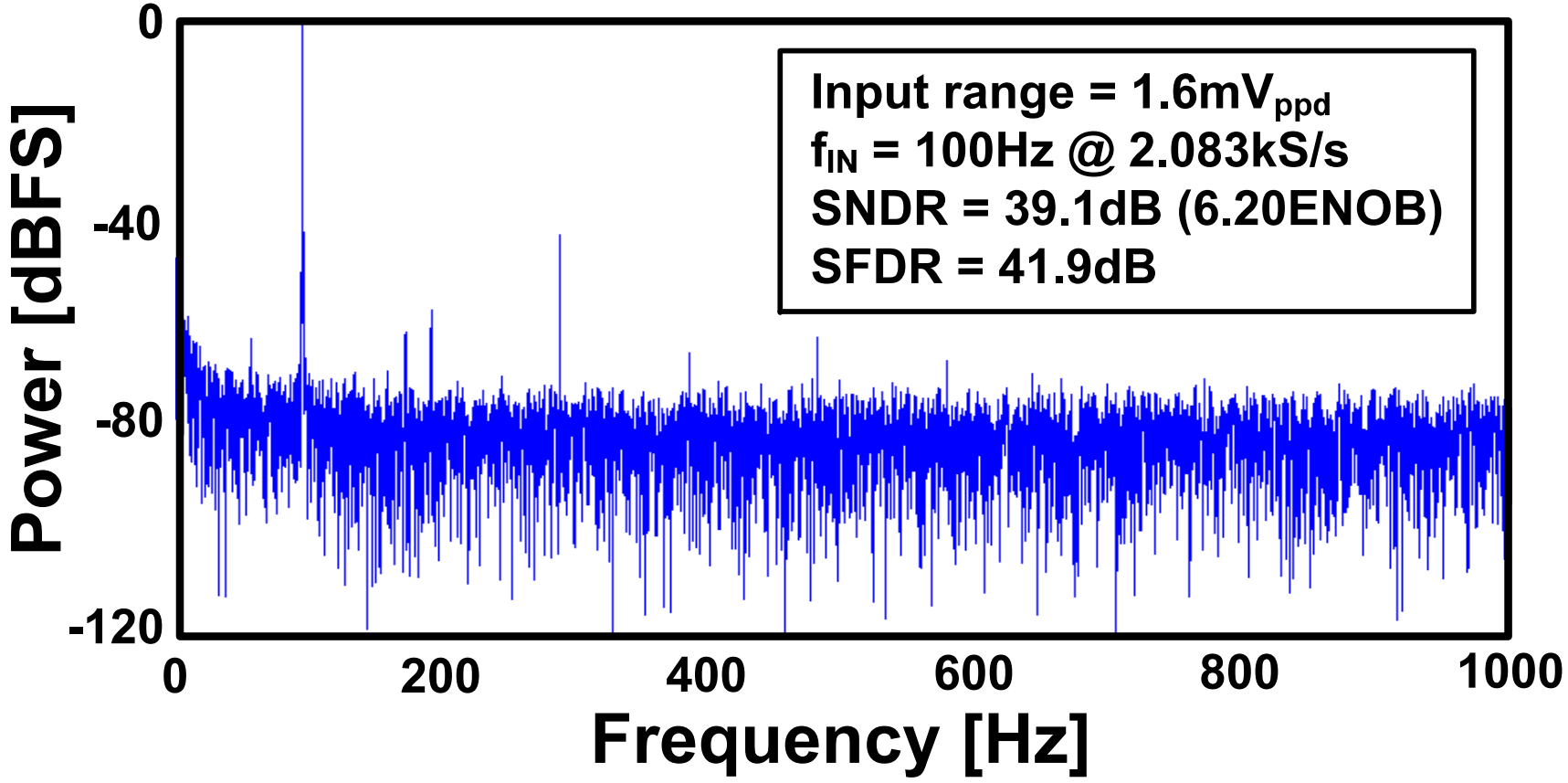
- **9bit ~ 5bit @ 8mV ~ 13mV ref. difference under a fixed input range of 6mV**

Measured DNL/INL Results



- DNL : -0.71 / +0.86 LSB
- INL : -1.05 / +1.12 LSB

Measured FFT & ENOB vs. Freq. Result



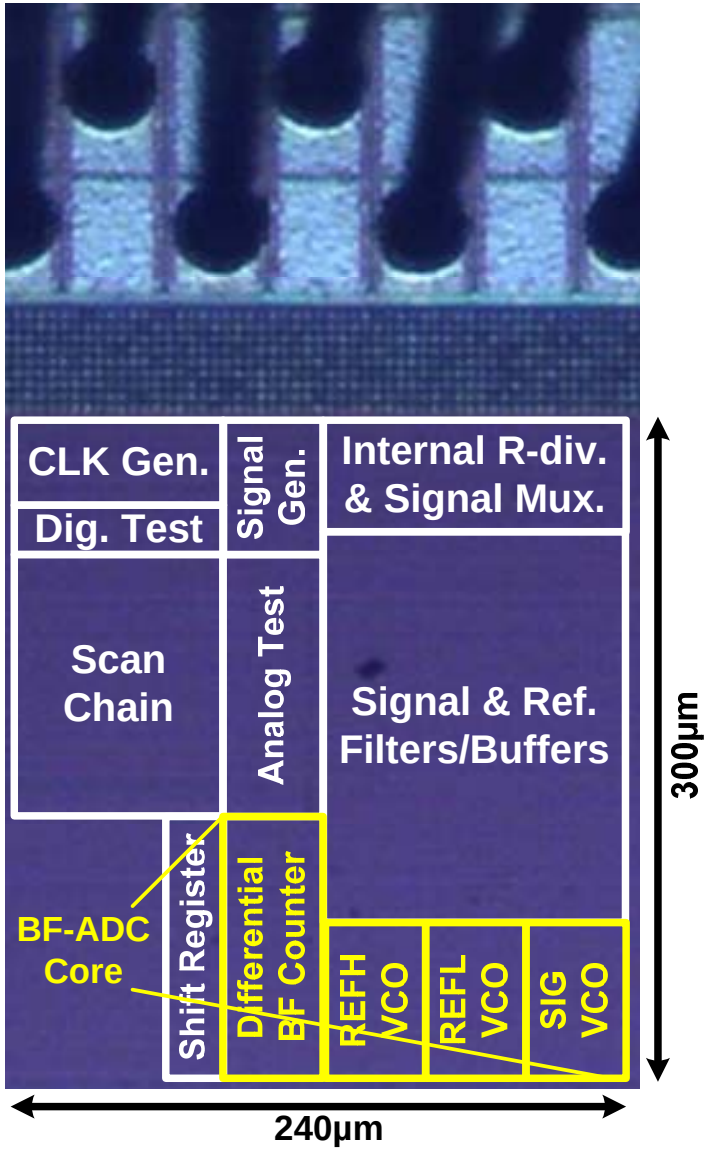
- SNDR = 39.1dB, SFDR = 41.9dB @ 1.6mV$_{ppd}$

Comparison w/ State-of-the-art ADCs

	[8] VLSI'07	[4] ISSCC'09	[9] VLSI'12	[1] ISSCC'11	[2] ISSCC'12	This work
ADC Type	Nonlinear Pipelined	VCO-based Delta-Sigma	Pipelined	SAR	SAR	Nonlinear Beat-Freq.
Input Range	Large[V]	Large[V]	Large[V]	Large[V]	Large[V]	Small[mV]
Process / Supply Voltage	0.18μm /1.62V	0.13μm /1.5V	0.18μm /1.3V	65nm /0.4V~1.0V	90nm /1.1V	65nm /0.5V~1.2V
Sampling Rate(f_S) / Power(P)	22MS/s /2.54mW	900MS/s /87mW	30MS/s /2.6mW	20kS/s /206nW	4MS/s /17.44μW	4.17kS/s /0.92μW
Energy Efficiency (P/f_S or $P/(2 \cdot f_{BW})$ for ΔΣ)	115.5pJ	2175pJ	86.7pJ	10.3pJ	4.36pJ	220.6pJ
SNDR [dB] @ Input Range	35.6@1V	78.1@2.28V	61.5@2.2V	55.0@1.1V	58.3@1.36V	39.1@1.6mV
ENOB [bit] @ Input Range	2.8@1mV	12.7@2.28V	9.9@2.2V	8.84@1.1V	9.4@1.36V	6.2@1.6mV
Conversion-steps per mV	6.96	2.92	0.43	0.42	0.50	45.95
*FOM_{1mV} [pJ/conv-step]	16.59	744.86	199.64	24.72	8.78	4.80
**Min. Input Amplitude [mV] (Dynamic Range)	0.10 (80dB)	0.28 (78dB)	1.85 (57dB)	1.96 (54dB)	1.65 (58dB)	***0.03 (89dB)
Area [mm^2]	0.560	0.450	0.500	0.212	0.047	0.013

*FOM normalized to 1mV (=-60dB), ** Input amplitude at SNDR = 0dB
*** based on measured SNDR of 10dB @0.12mV

Die Photo & Performance Summary



Process		65nm LP CMOS
Operating Voltage		0.5V ~ 1.2V
Area	Test chip	0.072mm²
	BF-ADC core	0.013mm²
Input Range		120μV ~ 6mV
Max. Sampling Rate		20.83kS/s
ADC Resolution		2.6bit ~ 9bit
DNL		-0.71/+0.86 [LSB]
INL		-1.05/+1.12 [LSB]
Dynamic Range		89dB
SNDR @ 1.6mV		39.1dB (ENOB=6.20)
SFDR @ 1.6mV		41.9dB
Power	VCO @ 2MHz	0.86μW
	Digital Power	0.06μW

Conclusions

- **A Beat Frequency based ADC is proposed and designed using 65nm process for a direct A-to-D conversion of sub-mV input signal**
- **39dB SNDR (6.2 ENOB) has been achieved for a 1.6mVppd input signal**
- **Fully-digital low area (0.013mm^2) and low power (<1μW) ADC-based frontend w/o amplifier for sensor applications**