A Fully-Digital Beat-Frequency Based ADC Achieving 39dB SNDR for a 1.6mV$_{pp}$ Input Signal

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***Abstract*- A fully-digital VCO-based ADC featuring a novel beat frequency detection scheme is demonstrated in 65nm LP CMOS. The proposed beat frequency based ADC is unique compared to previous VCO-based ADCs in that it is highly effective in measuring extremely small changes (e.g., 0.01%) in the VCO frequency within a short sampling time (e.g., 100 VCO periods). Direct amplifier-less A-to-D conversion of a 1.6mV$_{pp}$ differential input signal with 39dB SNDR and 6.2 ENOB was experimentally verified.**

I. Introduction

To meet the ever-increasing demands of energy-efficient sensor systems, there has been a great deal of circuit research aiming at developing compact low-power ADCs. For example, recent SAR-ADCs have demonstrated microwatt level power consumption while offering a scalable sampling rate and resolution [1-2]. While ADC remains a key building block for most mixed-signal systems, sensor applications do not always benefit from the improvements in the ADC power and performance because of the Low Noise Amplifier (LNA) and Variable Gain Amplifier (VGA) which are typically required for the signal pre-conditioning. Prior ADC designs however, focus on converting a rail-to-rail analog signal thereby neglecting the overhead of these analog components. Not only does this conventional design paradigm incur a large power and area overhead, it is also susceptible to device noise occurring in the signal amplification and filtering stages. In this work, we present a fully-digital Beat Frequency based ADC (BF-ADC) capable of directly measuring sub-mV input signals without an LNA or VGA. Fig. 1 contrasts the usage scenario of the conventional and proposed ADC.

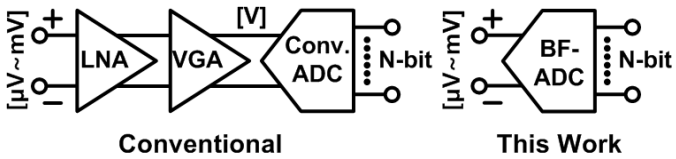


Fig. 1. The focus of this work is on direct acquisition of small input signals without using an LNA or VGA.

II. Beat Frequency (BF) Based ADC

The operating principle of the beat frequency (BF) detection scheme in the context of a VCO-based ADC is illustrated in Fig. 2. The proposed scheme can achieve a high resolution compared to a simple frequency counting method in cases where the frequency difference is extremely small. This is possible by measuring the period of the beat frequency signal which is equivalent to the time it takes for the faster signal to pass, catch up and overtake the slower signal again [3]. To understand better how the BF-ADC scheme works, let's consider a scenario in which the initial difference between the two VCO frequencies is 1%. This gives an output count of 100 as it takes 100 VCO periods for the slow and fast signal edges to overlap again. Now, suppose the frequency difference becomes 1.01% due to a small change in the input signal. This translates into an output count of 99 as it takes one less period for the fast signal to catch up with the slower one [3]. The same count change from 100 to 99 would have required a larger frequency change of 1% using the linear counting method implying a significantly lower sensing resolution. Note that for the beat frequency detection scheme, the frequency measurement resolution increases exponentially as the two VCO frequencies become closer to each other.

The aforementioned BF detection concept can be readily applied to an analog-to-digital converter as further indicated in Fig. 2. The incoming differential input signals V_N and V_P are first AC-coupled to the supply voltages of two VCOs, respectively. To produce high-resolution beat frequency counter outputs, the DC bias of the negative (or positive) input voltage is set to be slightly higher than that of the positive (or negative) input voltage. This ensures that the VCO biased using the negative (or positive) input voltage is always running faster (or slower) than the VCO biased using the positive input voltage. Using this configuration, the BF counter generates an output count value depending on how close the two VCO frequencies are as illustrated in Fig. 2.

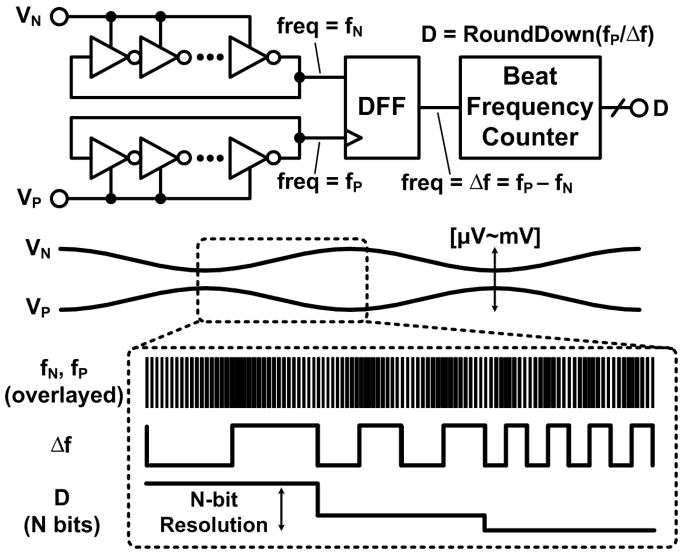


Fig. 2. Operating principle of proposed BF-ADC.

III. Dual Reference BF-ADC

One limitation of a simple BF-ADC scheme described above is that the sensing resolution quickly degrades as the difference between the positive and negative input voltages

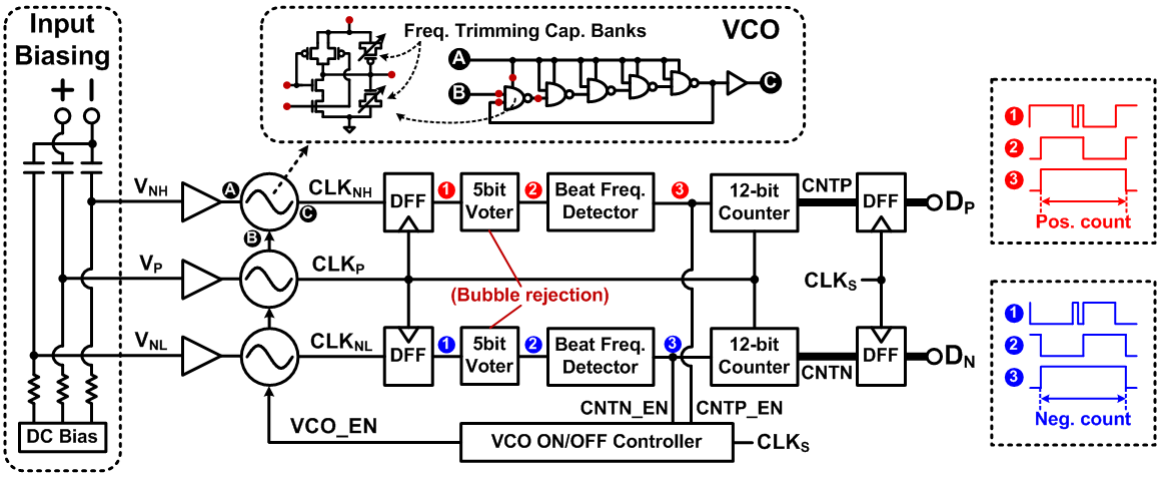


Fig. 3. Dual reference BF-ADC circuit for improved resolution.

becomes larger. To overcome this limitation, we propose a dual reference BF-ADC circuit shown in Fig. 3 where the negative input signal is AC-coupled to the supply voltage of not one but two VCOs with different DC bias levels. Using the two AC-coupled negative input signals as the upper bound and lower bound, we can obtain a high sensing resolution for both positive and negative phases of the differential input signal. The DC bias levels for the two reference VCOs (V_{NH} and V_{NL}) and the main VCO (V_P) in Fig. 3 are set using a simple on-chip voltage bias generator. Each VCO is implemented using 5 static NAND gates with programmable capacitor banks attached to each stage for fine grain frequency trimming. A static D flip-flop and a 5 bit majority voter circuit are used in both the upper and lower paths to generate the beat frequency signal while eliminating any logic bubbles (e.g. lone 1 in a stream of 0's) that may cause logic errors. A 12 bit counter is used to record the number of reference periods corresponding to the period of the beat frequency signal. The output count is then sampled by the main sampling clock CLK_S. The 12 bit positive and negative beat frequency values (D_P and D_N) are used to compute the actual input differential voltage [3]. Fig. 4 shows the timing diagram for a single sampling period of the BF-ADC circuit. To reduce unnecessary switching power, all VCOs are automatically shut off once the sampling is complete. Fig. 5 shows the signal waveforms measured from

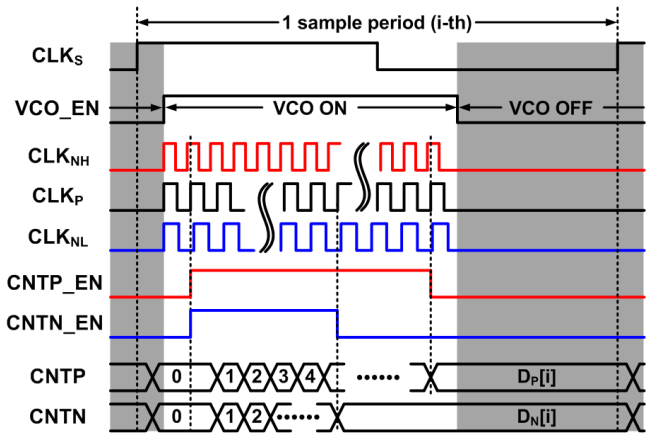


Fig. 4. Timing diagram for one sampling period.

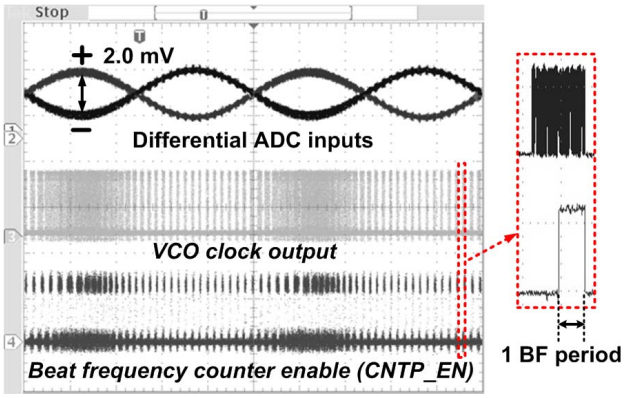


Fig. 5. Waveforms from BF-ADC test chip for a 4 mV_{pp} differential input.

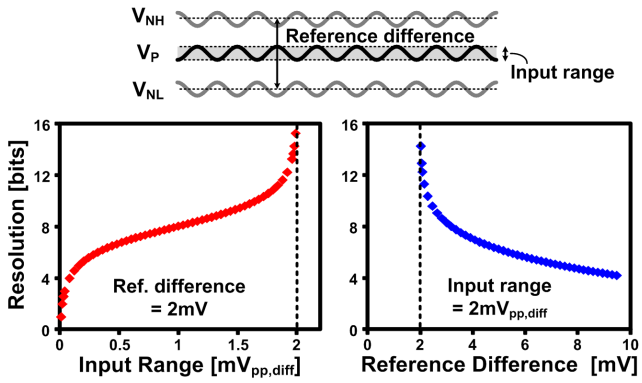


Fig. 6. Simulated resolution as a function of input range and difference between two AC-coupled reference voltages.

the 65nm BF-ADC test chip.

One interesting feature of the proposed BF-ADC is that we can obtain a uniformly high ADC resolution for a range of input signal amplitudes by simply adjusting the reference voltage levels. This eliminates the need for a separate variable gain amplifier reducing the power consumption, area, and complexity of the overall system. This would be particularly attractive for applications such as bio-potential (EEG, ECG, EMG, EOG) acquisition systems which may have to operate across a wide range of input signals with different amplitudes.

Simulation results in Fig. 6 show the BF-ADC resolution as a function of the signal input range and the difference between the upper bound and lower bound reference signals. The resolution increases exponentially as the reference difference approaches the input range, although in practice, the effective resolution, i.e. ENOB, is limited by the noise floor of the input and reference signals as well as the VCO phase noise. Fig. 7 shows the measured BF-ADC resolution from the 65nm test chip illustrating the dependence of the achievable ADC resolution on two key parameters: input range and reference voltage difference. Note that the measured resolution varies with the reference voltage. For instance, the resolution changes from 9bit to 5bit for a 5mV change in the reference voltage difference under a fixed input range of 6mV. Calibration techniques widely used in bio-signal sensing applications can be adopted to compensate for any PVT effects in the reference voltage generator circuit.

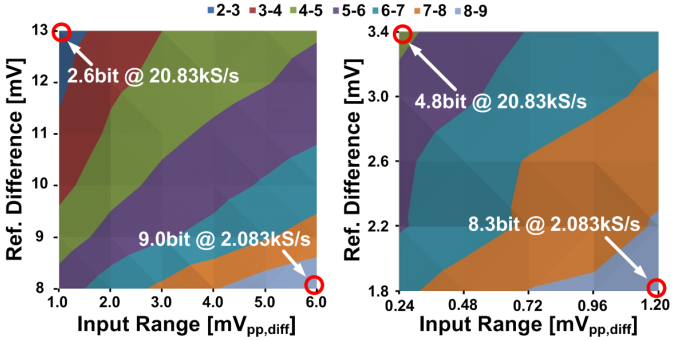


Fig. 7. Measured ADC resolution as a function of input range and reference voltage difference.

IV. Comparison with Conventional VCO-based ADC

VCO-based ADCs have been drawing attention lately owing to their digital-friendly implementation and inherent 1st order noise shaping property. Recent publications have reported high-order CT-ΔΣ loops utilizing a VCO-based ADC as a quantizer achieving very high SNDR (e.g. 78dB [4]). The proposed BF-ADC has the unique property of being able to achieve high resolution for very small input signals when used as a Nyquist rate ADC. Conventional VCO-based ADCs on the other hand take advantage of the noise-shaping property to improve resolution while sampling rail-to-rail input signals.

	Conv. VCO-based ADC	Proposed BF-based ADC
ADC Type	Delta-sigma	Nyquist rate
Main Feature	1st-order noise-shaping	Beat frequency detection
Input Range	Large [V]	Small [μV~mV]
VCO Linearity	Nonlinear K_{VCO} (large range)	Linear K_{VCO} (small range)
Key Circuit Block	VCO + linear counter	VCO + beat freq. counter
Counting Period	Fixed sample period	Variable beat freq. period
Sampling Rate	High speed [MS/s]	Low speed [kS/s]
Reconfigurability	No	Reconfigurable resolution
Applications	Wireless receiver [6, 7]	Sensor applications

Fig. 8. Comparison table of VCO-based ADC versus BF-ADC

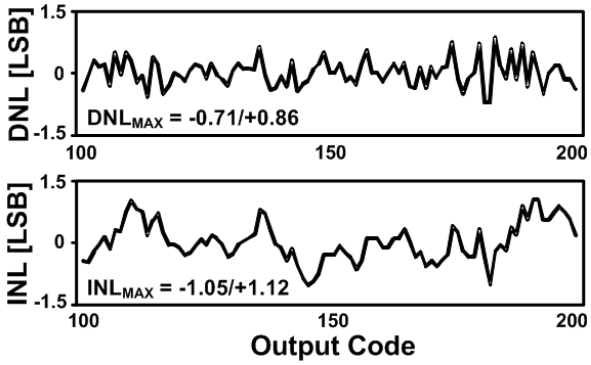


Fig. 9. Normalized DNL and INL from the measured output code.

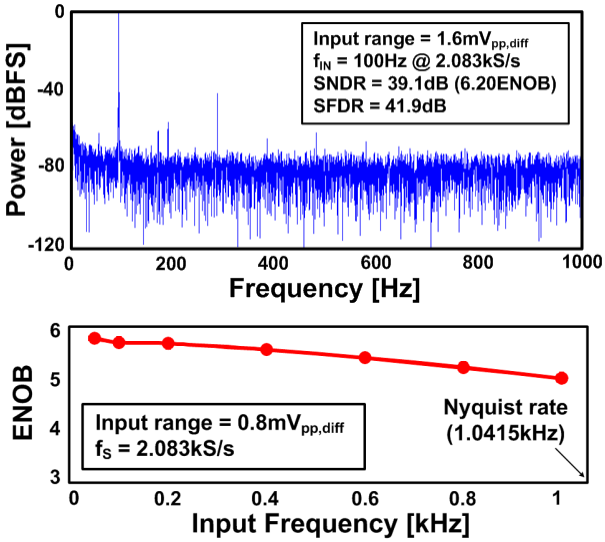


Fig. 10. Measured FFT for a 1.6mV$_{pp}$ AC signal with key ADC specifications (upper). ENOB versus input frequency data (lower).

Another noteworthy difference is that existing VCO-based ADCs have a fixed sampling period while the BF-ADC has a sampling period that is a function of the beat frequency period (i.e. difference between the main and reference frequencies). Finally, as far as linearity is concerned, conventional designs are more susceptible to the VCO's inherent voltage-to-frequency nonlinearity and difficult to achieve high performance unless sophisticated techniques such as the phase-feedback closed-loop [4] or digital calibration [5] are employed. This stems from the rail-to-rail input signal swing requirement of conventional ADCs. In contrast, BF-ADC has a better linearity as it can work for smaller input signals. Simulation results in 65nm show that the variation in K_{VCO} is reduced from ±14% to ±0.1% as the input signal amplitude is reduced from 400mV$_{pp}$ to 1mV$_{pp}$. Fig. 8 compares various features of a conventional VCO-based ADC and the proposed BF-ADC.

V. Test Chip Measurement Results

A BF-ADC test chip was implemented in a 65nm LP process as a proof of concept. The measured DNL and INL were -0.71/+0.86 LSB and -1.05/+1.12 LSB, respectively as shown in Fig. 9. For a sampling rate of 2.083kS/s and an input

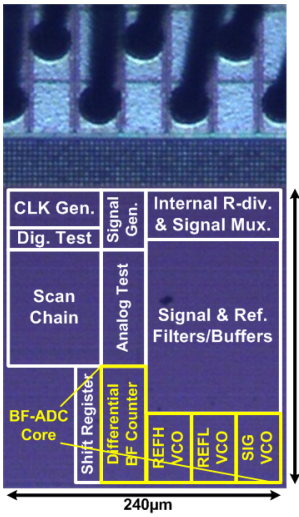
	[8] VLSI'07	[4] ISSCC'09	[9] VLSI'12	[1] ISSCC'11	[2] ISSCC'12	This work
ADC Type	Nonlinear Pipelined	VCO-based Delta-Sigma	Pipelined	SAR	SAR	Nonlinear Beat-Freq.
Input Range	Large[V]	Large[V]	Large[V]	Large[V]	Large[V]	Small[mV]
Process / Supply Voltage	0.18µm /1.62V	0.13µm /1.5V	0.18µm /1.3V	65nm /0.4V~1.0V	90nm /1.1V	65nm /0.5V~1.2V
Sampling Rate(f_S) / Power(P)	22MS/s /2.54mW	900MS/s /87mW	30MS/s /2.6mW	20kS/s /206nW	4MS/s /17.44µW	4.17kS/s /0.92µW
Energy Efficiency (P/f_S or $P/(2{\cdot}f_{BW})$ for ΔΣ)	115.5pJ	2175pJ	86.7pJ	10.3pJ	4.36pJ	220.6pJ
SNDR [dB] @ Input Range	35.6@1V	78.1@2.28V	61.5@2.2V	55.0@1.1V	58.3@1.36V	39.1@1.6mV
ENOB [bit] @ Input Range	2.8@1mV	12.7@2.28V	9.9@2.2V	8.84@1.1V	9.4@1.36V	6.2@1.6mV
Conversion-steps per mV	6.96	2.92	0.43	0.42	0.50	45.95
*FOM_{1mV} [pJ/conv-step]	16.59	744.86	199.64	24.72	8.78	4.80
**Min. Input Amplitude [mV] (Dynamic Range)	0.10 (80dB)	0.28 (78dB)	1.85 (57dB)	1.96 (54dB)	1.65 (58dB)	***0.03 (89dB)
Area [mm^2]	0.560	0.450	0.500	0.212	0.047	0.013

*FOM normalized to 1mV (=-60dB), ** Input amplitude at SNDR = 0dB, *** based on measured SNDR of 10dB @0.12mV

Fig. 11. Comparison with previous ADCs.

signal of $1.6mV_{pp,diff}$, a 39.1dB SNDR (6.2bit ENOB) and a 41.9dB SFDR were achieved (Fig. 10). Fig. 10 also shows the measured ENOB as a function of the input signal frequency, showing a 5.0 to 5.8 ENOB range for a $0.8mV_{pp}$ differential input signal. Here, the Nyquist rate frequency is 1.0415kHz. Fig. 11 compares the performance of the proposed ADC versus prior ADCs including a nonlinear pipeline ADC [8], a VCO-based ADC [4], a linear pipelined ADC [9], and two state-of-the-art SAR-ADCs [1-2]. BF-ADC shows a FOM (normalized to $1mV_{pp,diff}$) of 4.80pJ/conv-step, a dynamic range (normalized to 1.2V) of 89dB, and an area of $0.013mm^2$ which is much smaller than the other ADCs. The compact nature and simplicity of the BF-ADC makes it ideally suited for multi-channel bio-signal sensors which require large and power hungry multi-stage amplifiers and signal filters per channel. In contrast, BF-ADC only requires passive signal filters which have a smaller footprint compared to having dedicated amplifier circuits. The test chip microphotograph and feature summary table are given in Fig. 12.

VI. CONCLUSION



Process		65nm LP CMOS
Operating Voltage		0.5V ~ 1.2V
Area	Test chip	0.072mm²
	BF-ADC core	0.013mm²
Input Range		120µV ~ 6mV
Max. Sampling Rate		20.83kS/s
ADC Resolution		2.6bit ~ 9bit
DNL		-0.71/+0.86 [LSB]
INL		-1.05/+1.12 [LSB]
Dynamic Range		89dB
SNDR @ 1.6mV		39.1dB (ENOB=6.20)
SFDR @ 1.6mV		41.9dB
Power	VCO @ 2MHz	0.86µW
	Digital Power	0.06µW

Fig. 12. Chip microphotograph and feature summary table.

In this paper, we have presented a fully-digital VCO-based ADC utilizing the beat-frequency detection scheme for sampling signals with sub-mV amplitudes. To improve the ADC resolution, we propose a dual reference BF-ADC scheme which employs two reference VCOs. One VCO is running at a frequency higher than the maximum frequency of the main VCO while the other VCO has a frequency that is lower than the minimum frequency of the main VCO. This technique helps maintain a consistently high sensing resolution for both positive and negative phases of the input signal. A 65nm test chip demonstrates 6.2 ENOB for a $1.6mV_{pp}$ input differential signal without any external signal amplification or conditioning circuitry.

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