Deep Trench Capacitor based Step-up and Step-down DC/DC Converters in 32nm SOI with Opportunistic Current Borrowing and Fast DVFS Capabilities

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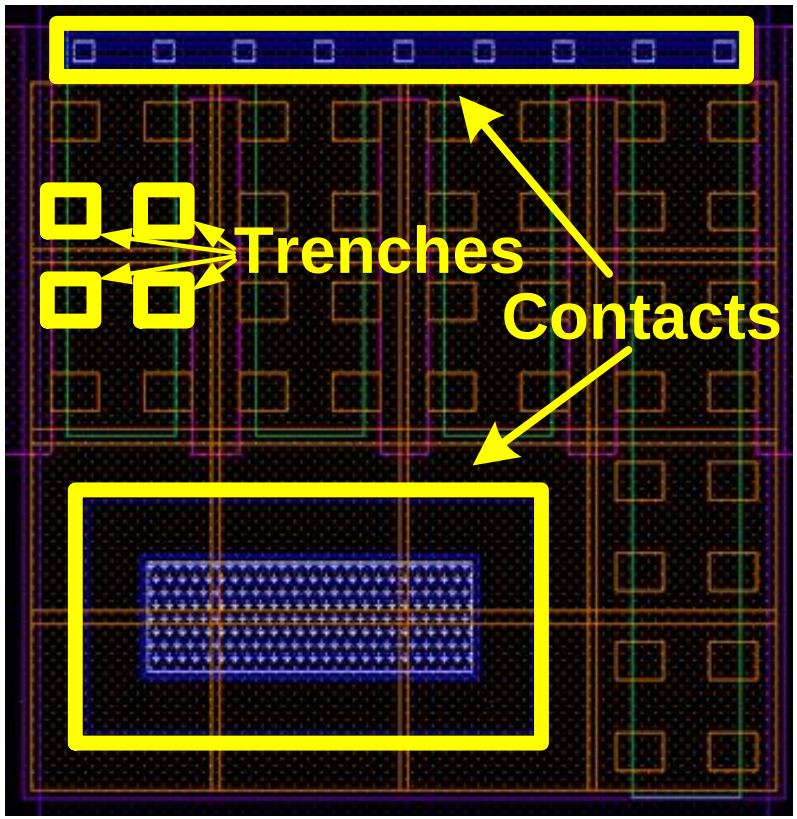
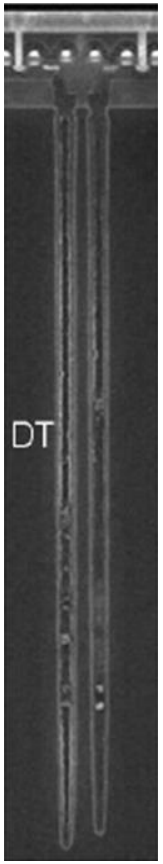
Outline of the Presentation

- **Deep trench capacitors as flying capacitors**
- **Feature1 implementation: Reduction of DVFS rise time**
- **Feature2 implementation: IR noise reduction using current borrowing**
- **32 nm test chip results**
- **Conclusions**

Layout and Cross-sectional View of Deep Trench Capacitor

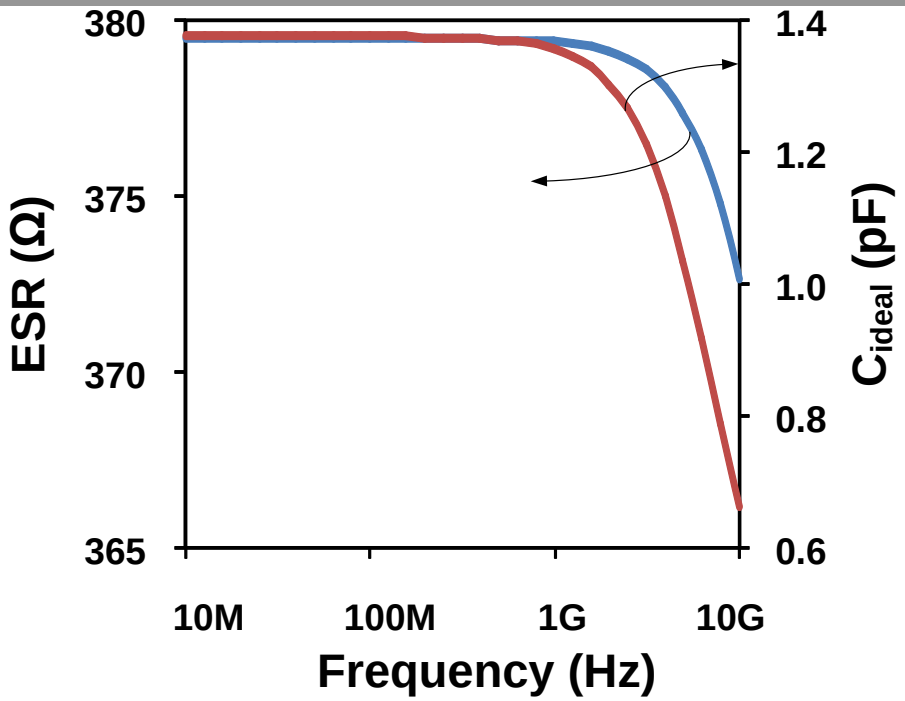


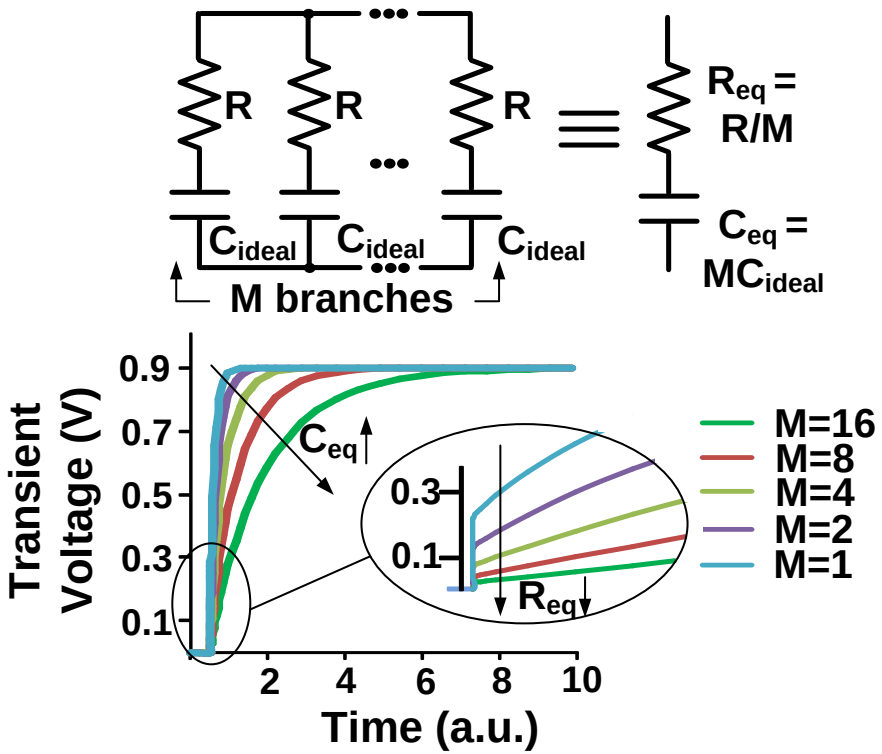


N. Butt et. al., IEDM 2010

- **Originally meant for embedded memory application**
- **20X+ denser than MOS capacitors**

Frequency and Transient Response of Deep Trench Capacitors





- **Frequency dependent Equivalent Series Resistance (ESR) and C_{ideal}**
- **ESR can be made negligible by increasing multiplicity (M)**
- **Transient simulation assumes 500Ω switch resistance in series with the trench cap**

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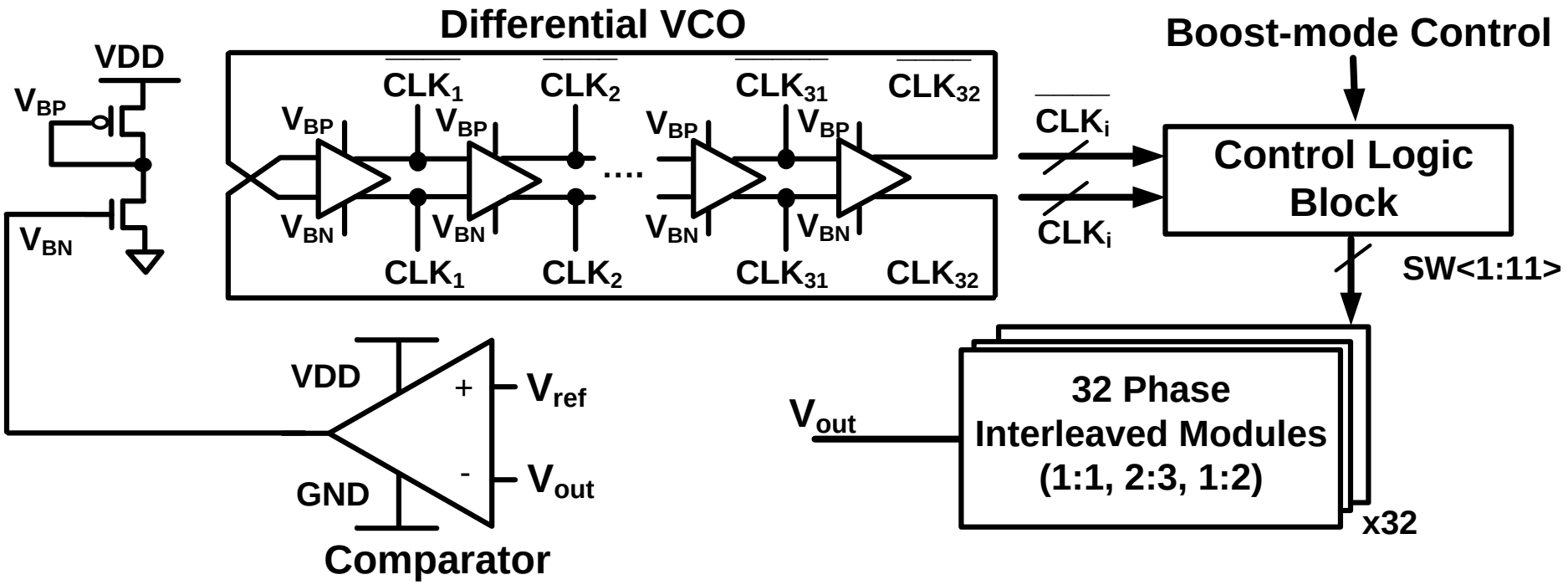
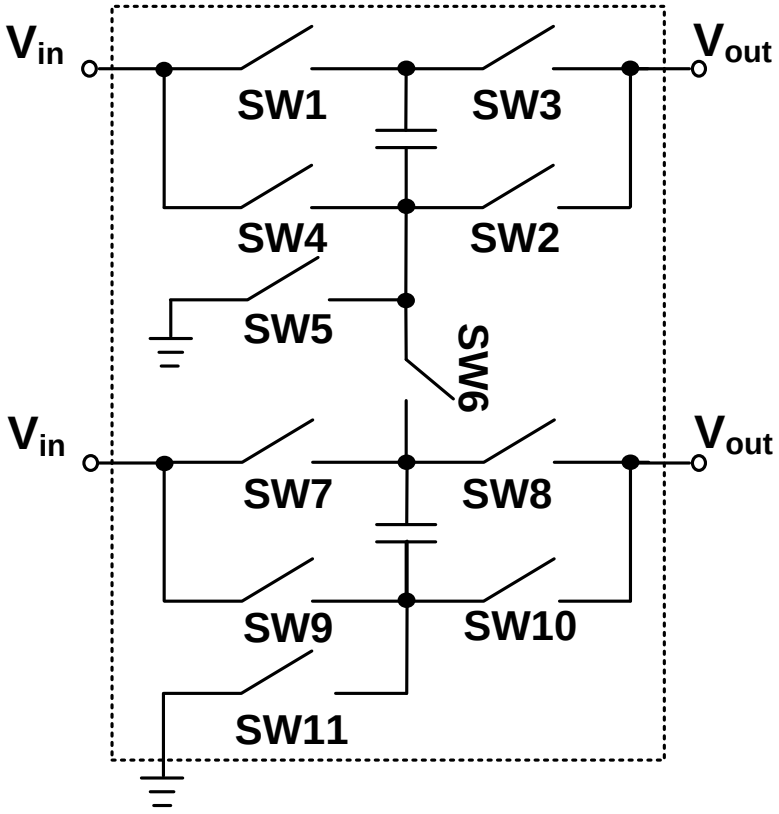
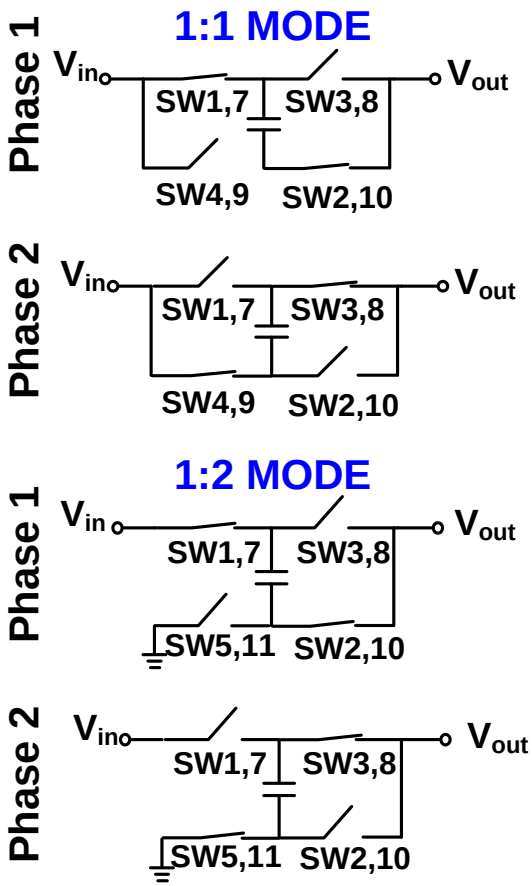
Block Diagram of Step-down Converter in a Feedback Loop

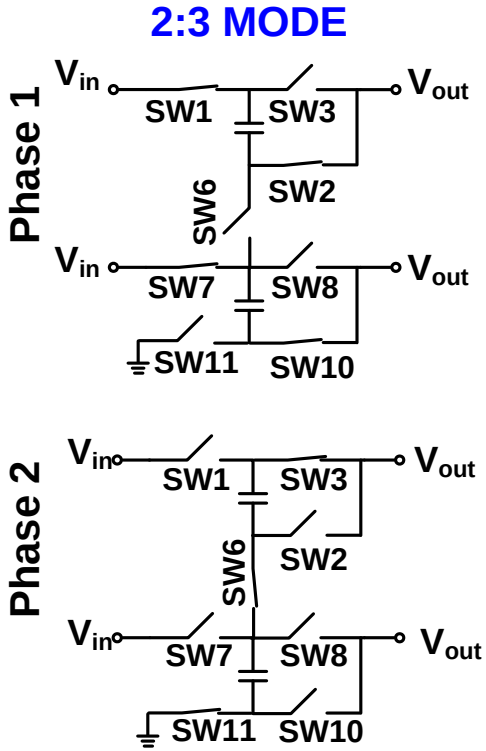


- **Converter modules, comparator, VCO and control units connected in a feedback loop**
- **Time interleaved modules to mitigate output ripple**
- **Boost mode control to enable/disable fast DVFS scheme**

Switch Configuration for Various Conversion Ratios

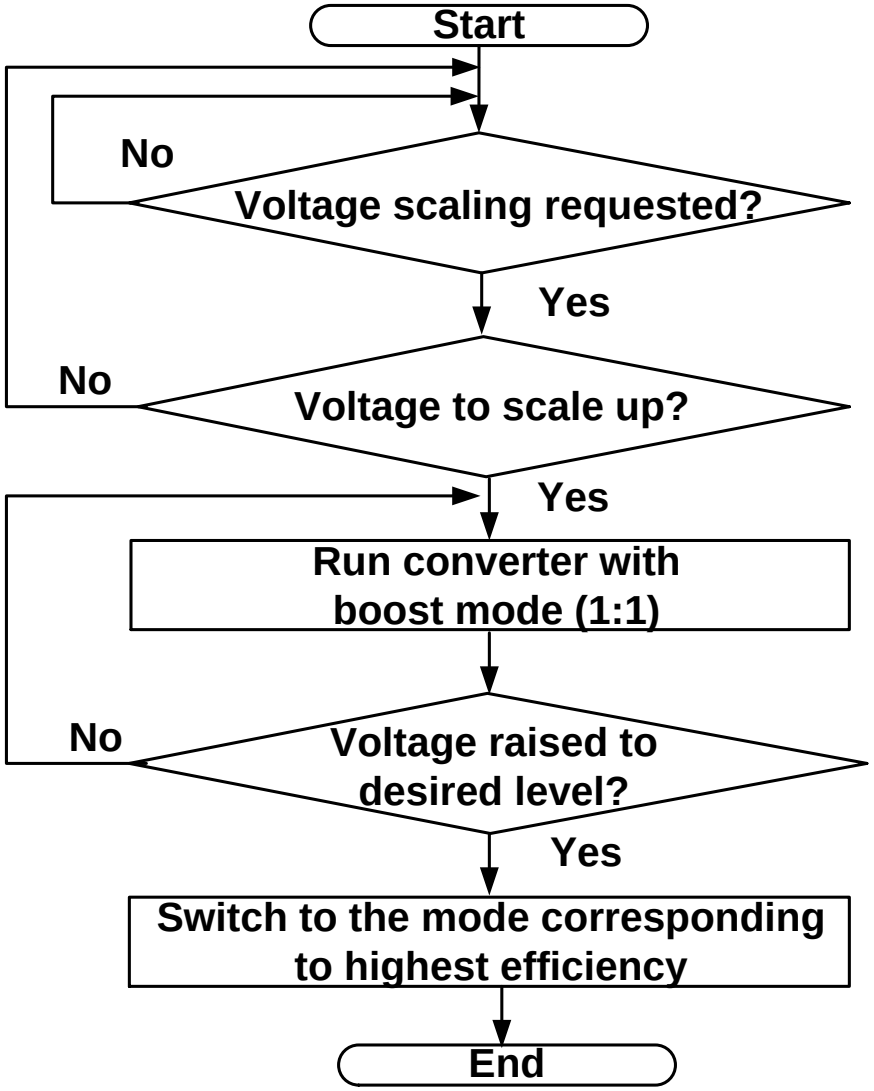






- **Reconfigurable converter module with 11 switches and 2 capacitors**
- **Ratios implemented are 1:1, 2:3 and 1:2**

Fast DVFS Control Scheme



- **Slow DVFS is due to slow charging of supply network**
- **Control logic selects 1:1 ratios for pumping charge at a greater rate**
- **Normal mode is restored to ensure high efficiency**

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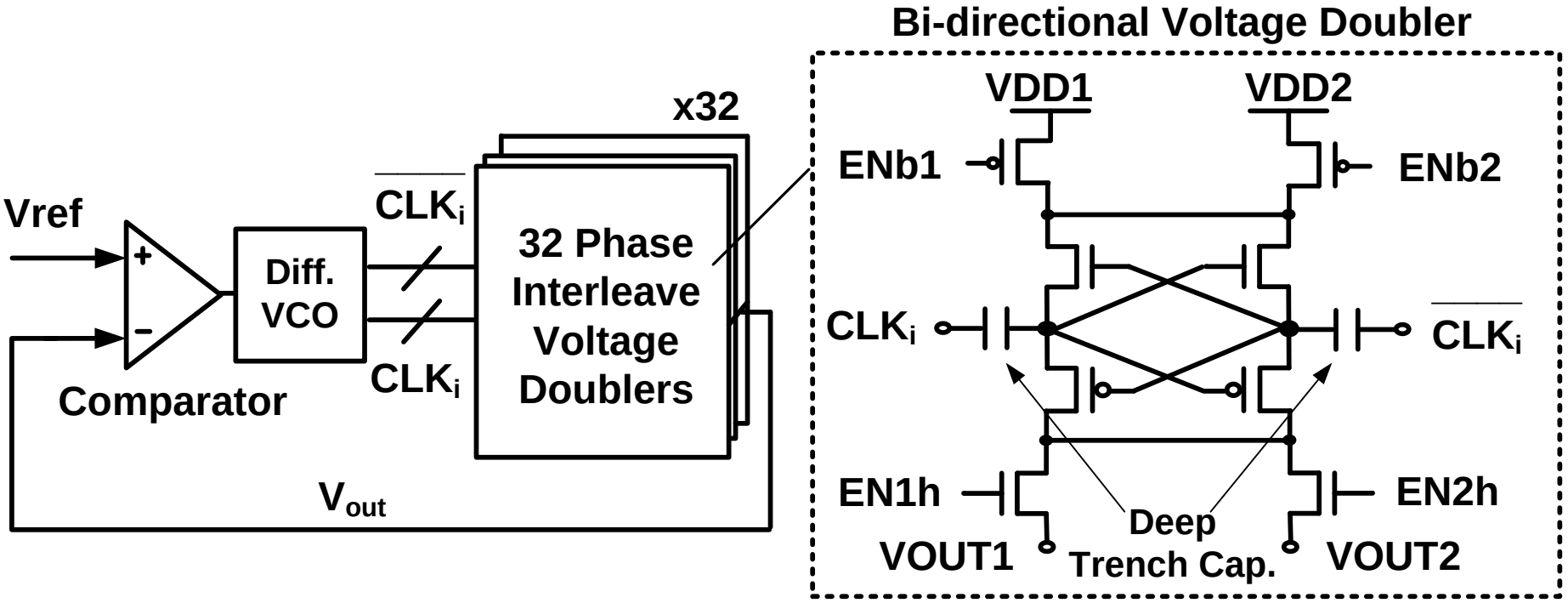
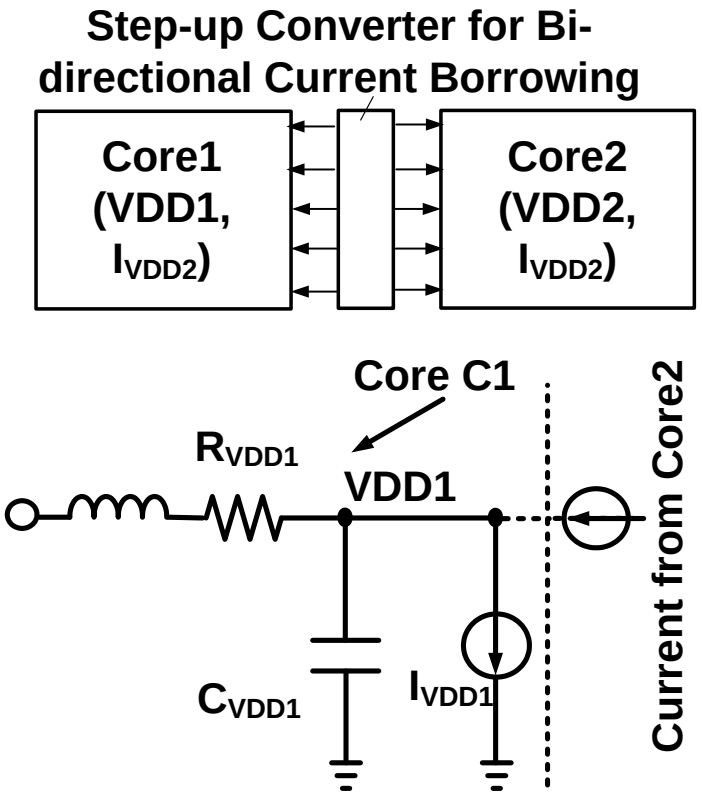
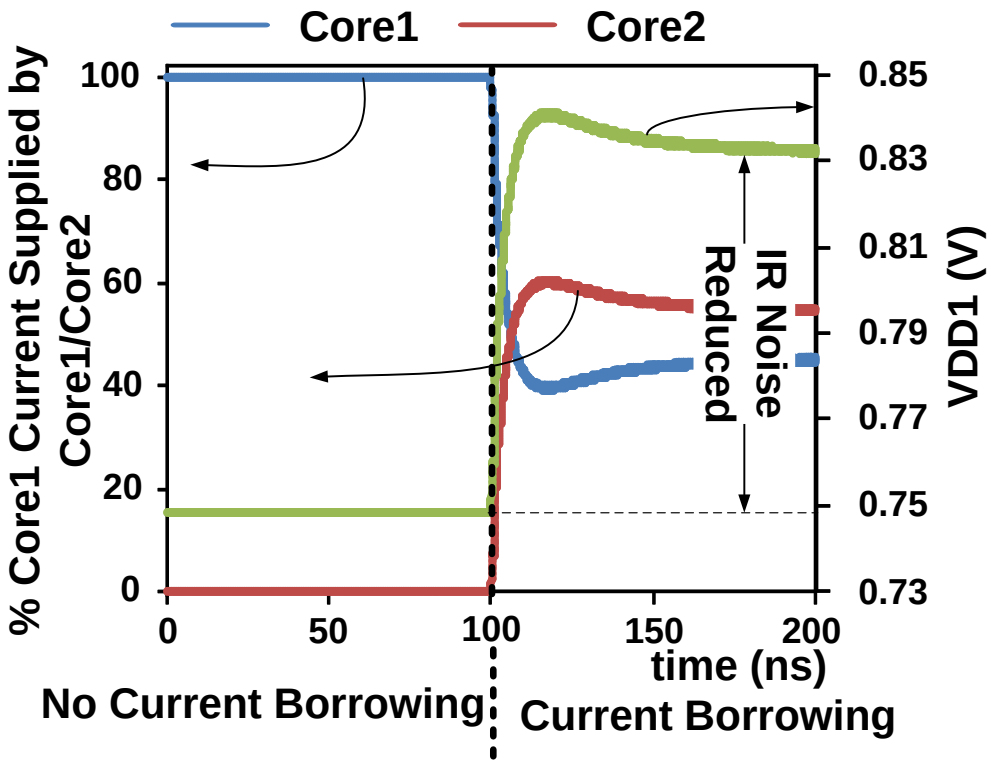
Step-up Converter Block Diagram and Modified Favrat Cell



- **Phase interleaved voltage doublers for ripple mitigation**
- **Modified Favrat cells for bi-directional voltage doubling**

Supply Noise Reduction Using Current Borrowing





- Active core borrows current from adjacent idle core
- Voltage level of idle core boosted by step-up converter

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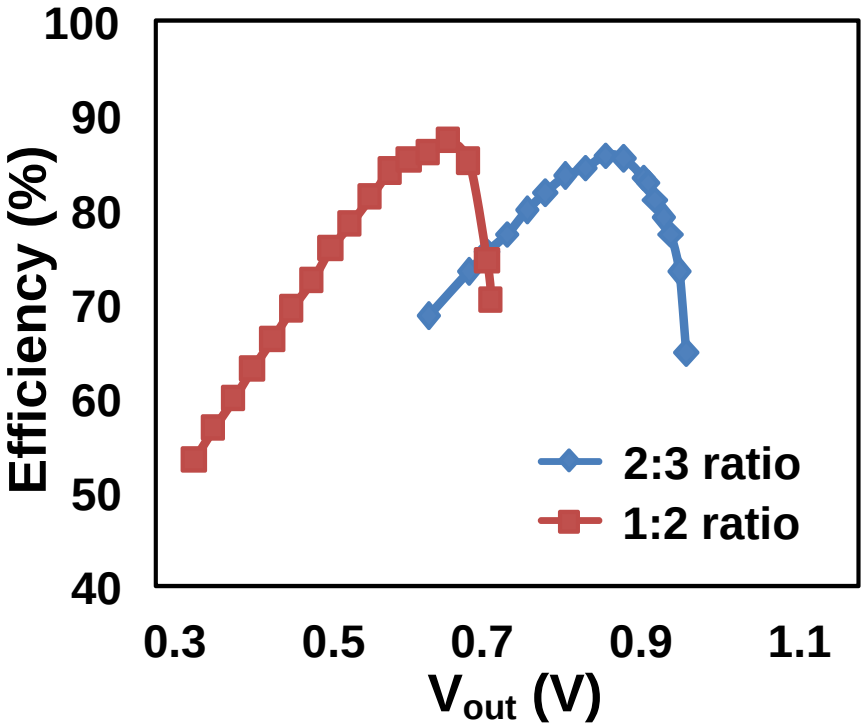
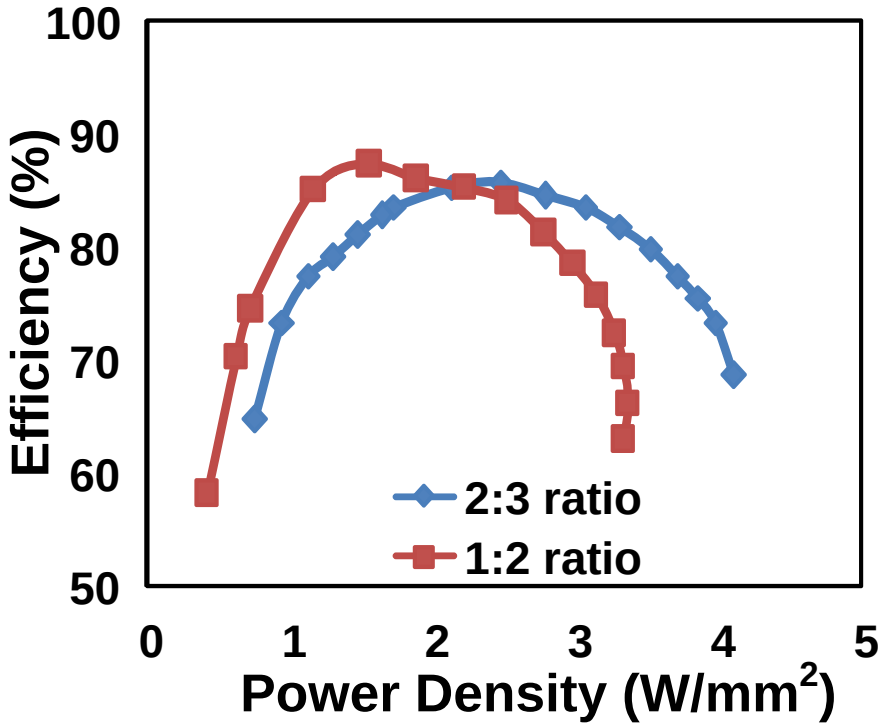
Measured Efficiency of Step-down Converter : Without Feedback Control

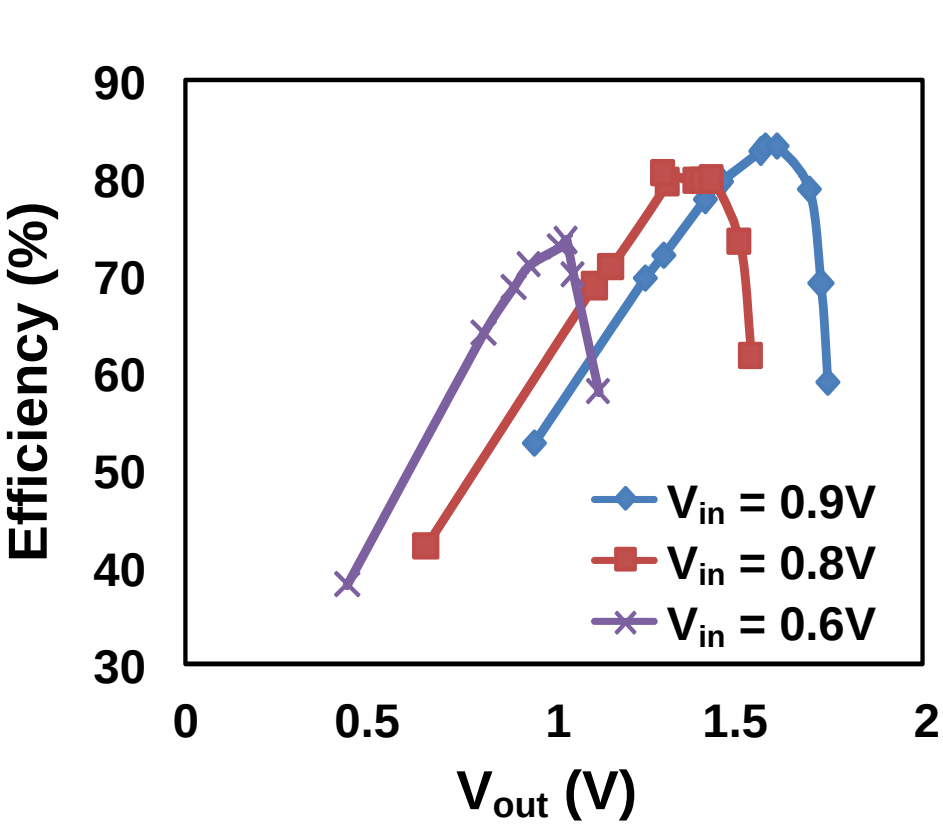
0.9V, 32nm HKMG SOI, 100MHz, V_{in}=1.5V

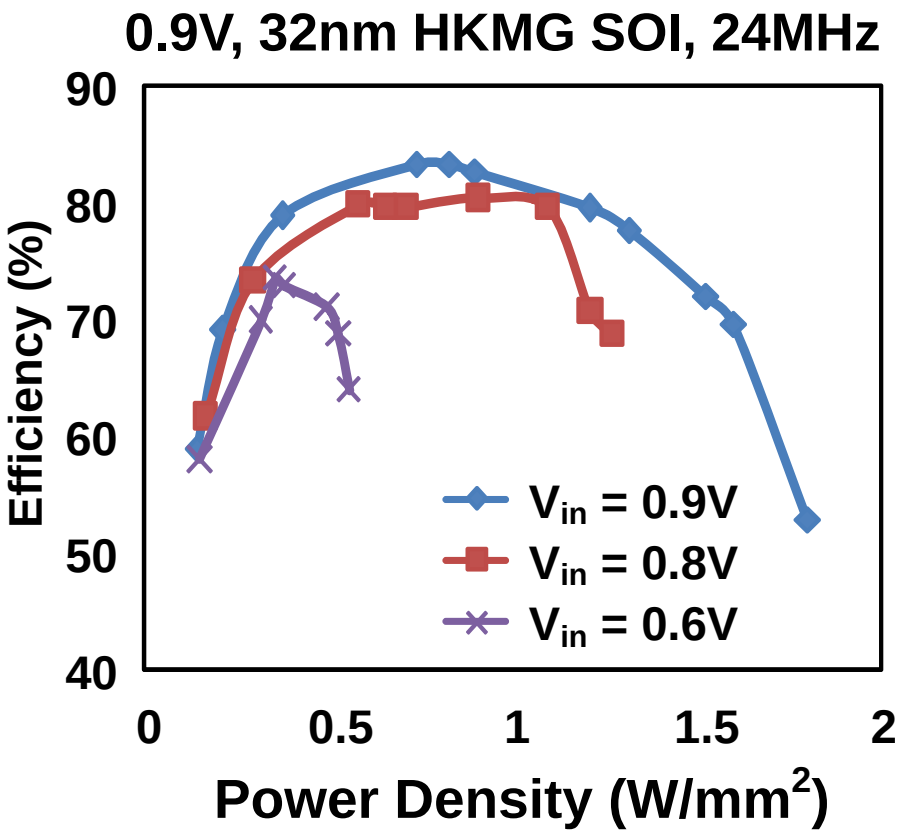




- Capable of delivering 2.78W/mm^2 at 85% efficiency when configured as 2:3 ratio
- Efficiency is over 70% for V_{out} ranging between 0.5V and 0.9V

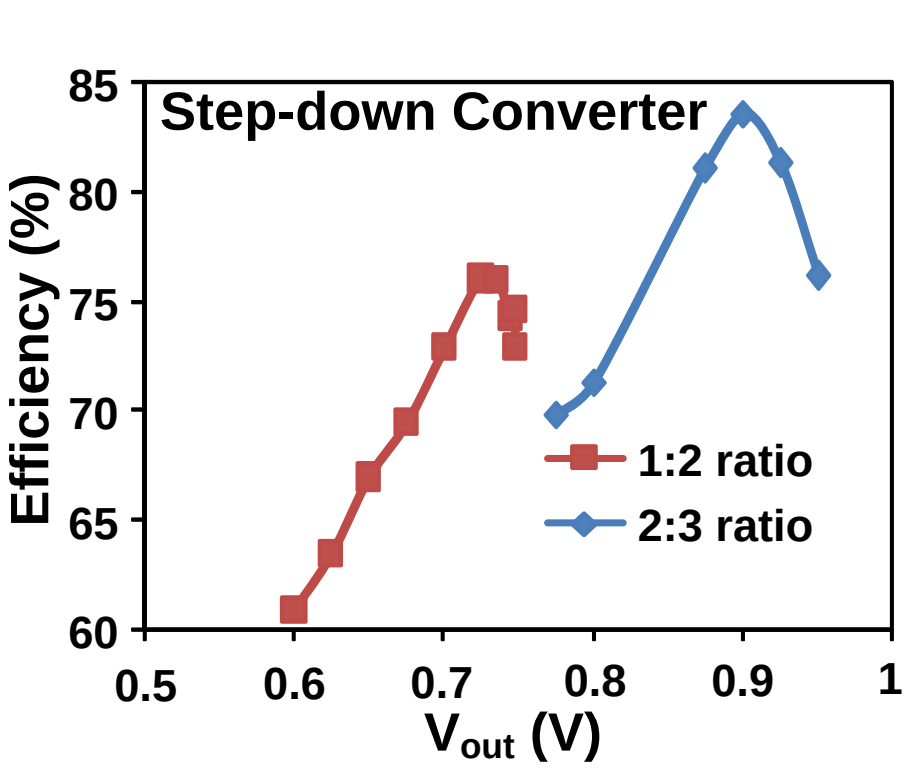
Measured Efficiency of Step-up Converter: Without Feedback Control



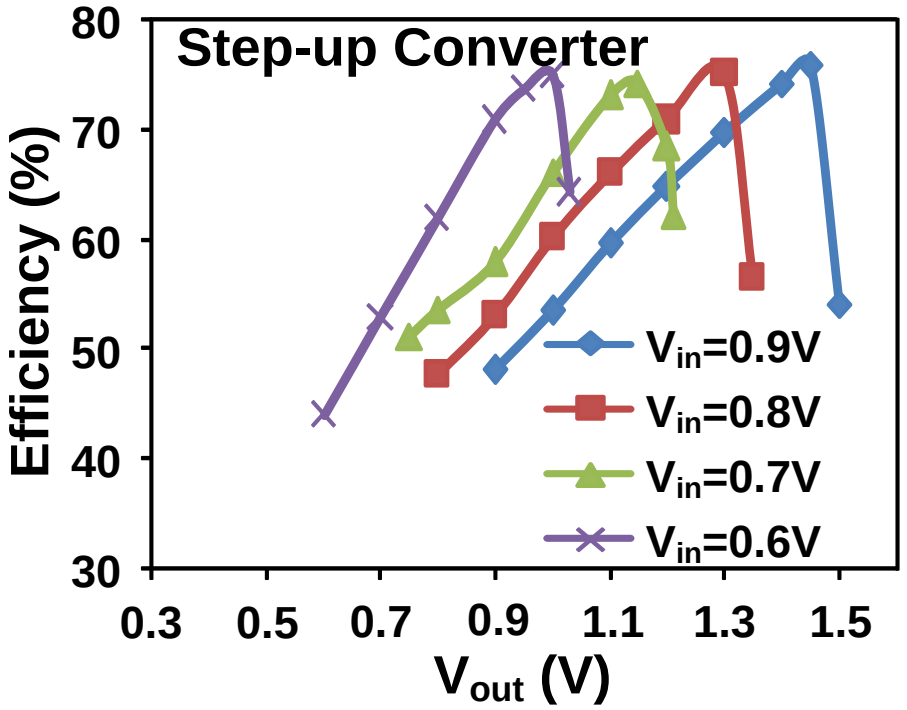


- Capable of delivering a power density of 0.9W/mm^2 at 80% efficiency at V_{in}=0.9V
- For V_{out} =0.9V, efficiency is largest when V_{in}= 0.6V

Measured Efficiency of Step-up and Step-down Converters: With Feedback Control

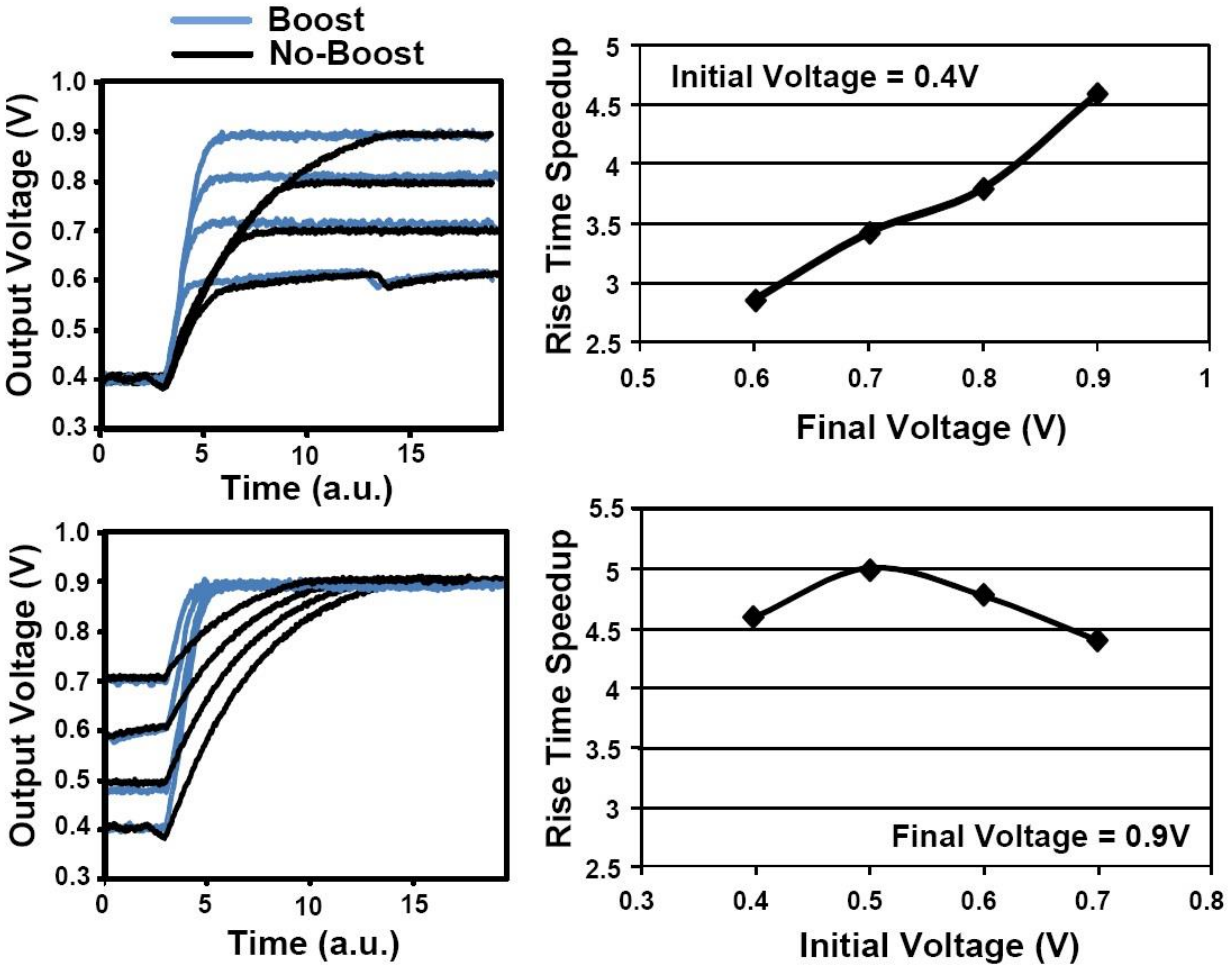


0.9V, 32nm HKMG SOI



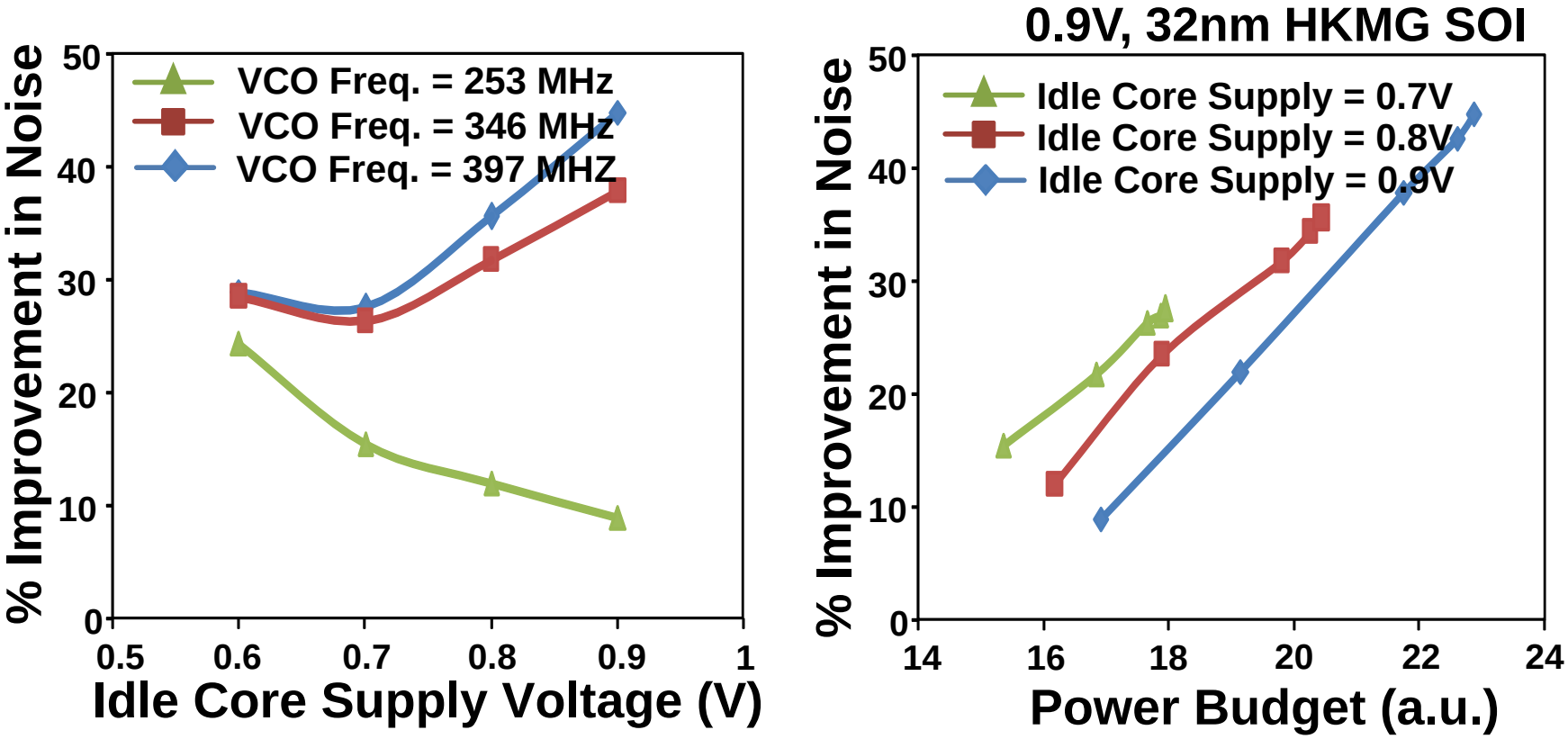
- Closed-loop efficiency vs. V_{out} plots assume ring oscillator load
- Efficiency was measured including power consumption of feedback control circuits

DVFS Speedup Measurement



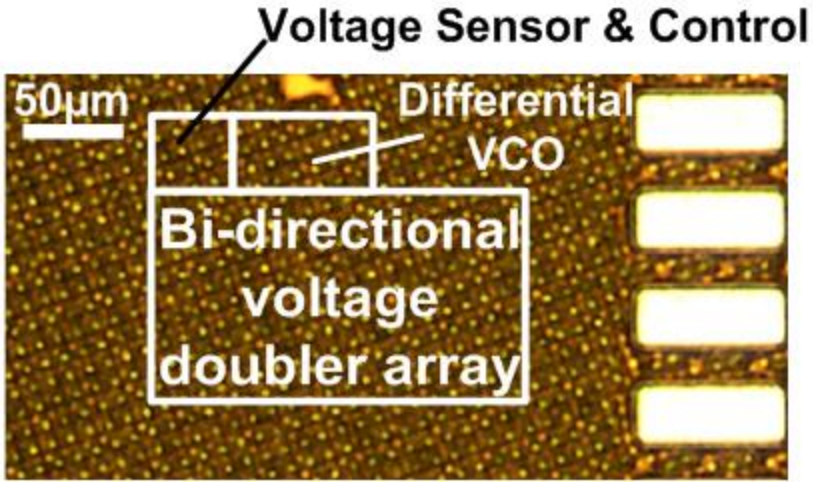
- **Rise time improves by a factor of 5X when V_{out} rises from 0.5V to 0.9V**

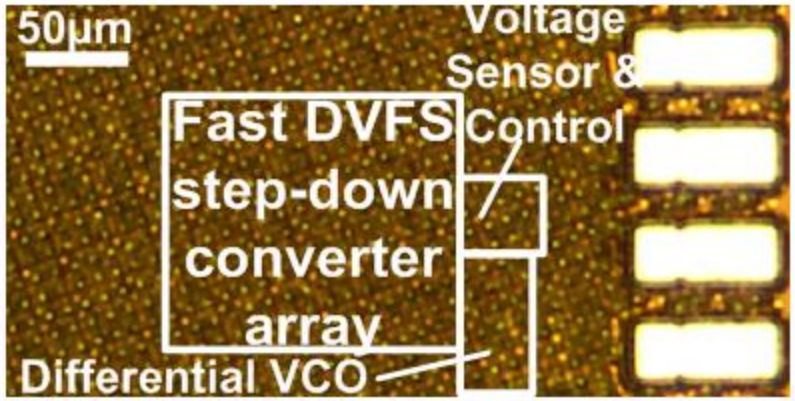
% Improvement in IR Noise



- When VCO frequency↑, charge transfer process faster, IR noise ↓
- When power budget ↓, borrowed current is limited, IR noise ↑

Test Chip Microphotograph and Performance Summary





Tech. Node	Flying Cap.	Operating Modes	Feedback Control Loop	Max. Eff.	Power Density at Max. Eff.	Additional Circuit Feature
32nm SOI	Deep Trench Cap.	2:1 Step-up & 1:2, 2:3, 1:1 Step-down	Yes	85%	2.78W/ mm^2 for 2:3 ratio	Fast DVFS, IR noise reduction

Conclusions

- **Use of deep trench capacitor results in 20x+ higher power density**
- **DVFS rise time can be improved using 1:1 ratio of step-down converter**
  - **5X speed up of DVFS rise transient is observed**
- **IR noise of a core can be reduced by borrowing current opportunistically from adjacent low activity cores**
  - **45% reduction in IR noise for idle core VDD=0.9V**