On-Chip Silicon Odometers and their Potential Use in Medical Electronics

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***Abstract*— The parametric shifts or circuit failures caused by transistor aging have become more severe with shrinking device sizes and voltage margins. Designing circuits that can withstand these aging effects is particularly critical in medical applications where systems must operate flawlessly across a range of conditions for their entire lifetimes. In this work we present several on-chip Silicon Odometers that provide measurement data required to develop transistor degradation models. One such scheme—a beat frequency detection circuit capable of recording oscillator frequency shifts ranging down to a theoretical limit of less than 0.01%—may be suited to trigger real-time adjustments that compensate for lost performance on products in the field. Incorporating this sensing capability may be especially attractive in implantable medical electronics.**

Keywords – Aging; circuit reliability; digital measurements

I. Introduction

The integrated circuits design community is facing unprecedented challenges as CMOS technology approaches several fundamental limitations. Process variability, leakage power and device reliability issues increasingly nullify much of the performance benefit gained by traditional device scaling. In particular, the parametric shifts or circuit failures caused by Bias Temperature Instability (BTI), Hot Carrier Injection (HCI), and Time Dependent Dielectric Breakdown (TDDB) have become more severe with shrinking transistor sizes and voltage margins. We now have chips containing billions of transistors operating at several GHz, with precariously small voltage margins between the supply levels and threshold voltages. More switching activity means more heat density, which accelerates most aging mechanisms. Process improvements such as strained silicon and high-k/metal gate also introduce new degradation concerns, such as BTI in NMOS devices. Finally, technology scaling has led to a massive increase in the number of operating conditions devices find themselves in, so there is a larger variation in their aging processes.

Semiconductor companies generally deal with this aging problem by playing it safe. For example, they build generous guardbands into clock speeds in order to ensure that products will continue to operate over their intended lifetimes. This means that clocks have to be slowed down to well below the limits for fresh circuits in order to account for the inevitable logic slow-down that comes with aging, among other variables. By doing so, manufacturers throw out a portion of the performance benefit that comes with scaling because of problems that arise after long periods of use.

In addition, device dimensions have now been pushed to the atomic scale, and we are approaching physical limitations where transistors no longer act as reliable switches. Manufacturers are facing significant challenges in the fabrication process which could become too costly to surmount. In this environment where we cannot count on continued performance improvements from scaling alone, making conservative estimations about circuit aging will no longer do. In much of the medical devices space, the concerns caused by transistor aging are different. While clock speeds are not as high, and more mature technologies are often used, circuit failure is not an option. Although front end aging is now having a larger impact in modern high performance circuits, it has occurred in all technology nodes to varying degrees. In addition, implantable medical electronics often operate at very low voltages, magnifying even small changes in device performance. Due to the strict reliability standards for medical electronics, a comprehensive approach to dealing with transistor degradation is required.

Research, design, and process development groups are all now devoting significant resources to better understanding and addressing circuit aging. One critical aspect of that work involves developing accurate and efficient means to measure the effects of the different aging mechanisms in order to develop reliability models which are used to design robust circuits. Another option for addressing aging effects is to use on-chip reliability monitors that can trigger real-time adjustments to compensate for lost performance or device failures. This article gives on overview of a new class of test structures that can efficiently collect circuit aging data using on-chip circuits. Circuits-based test structures provide a number of benefits over traditional device probing, such as higher measurement resolution, shorter stress interruptions, reduced test structure area, shorter test times, and simpler test interfaces.

II. Overview of Device Aging Mechanisms

Negative Bias Temperature Instability (NBTI) in PMOS is characterized by a positive shift in the absolute value of the V_{th} (threshold voltage), which occurs when a device is biased in strong inversion with a small, or no lateral electric field (i.e., $V_{DS} \approx 0$ V). The V_{th} shift is generally attributed to hole trapping in the dielectric bulk, and/or to the breaking of Si-H bonds at the gate dielectric interface by holes in the inversion layer, which generates positively charged interface traps. When a stressed device is turned off, it immediately enters the recovery phase, where trapped holes are released, and/or the freed hydrogen species diffuse back towards the substrate/dielectric interface to anneal the broken Si-H bonds, thereby reducing the absolute value of the V_{th}. Measureable recovery has been shown to occur within 1 μs, so fast measurement systems are required to characterize BTI transients [1-2]. Positive Bias Temperature Instability (PBTI)

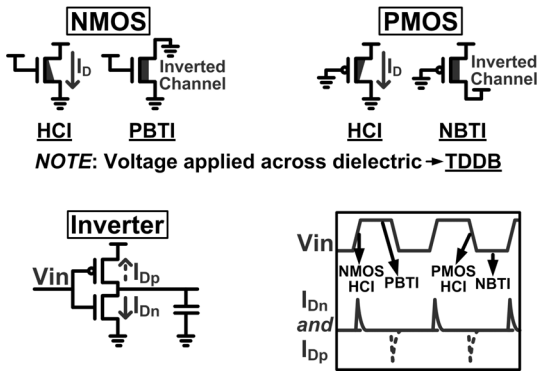


Fig. 1. BTI, HCI, and TDDB stress illustrated for NMOS and PMOS transistors, as well as an inverter during standard operation.

in NMOS transistors was not critical with silicon dioxide dielectrics, but is now contributing to the aging of high-k gate stacks [3].

HCI has become less prominent with the reduction of operating voltages, but remains a serious concern due to the large local electric fields in scaled devices. Hot carriers (i.e., those with high kinetic energy) accelerated toward the drain by a lateral electric field across the channel lead to secondary carriers generated through impact ionization. Either the primary or secondary carriers can gain enough energy to be injected into the gate stack. This creates traps at the silicon substrate/gate dielectric interface, as well as dielectric bulk traps, and hence degrades device characteristics such as V_{th}.

Finally, any voltage drop across the gate stack can cause the creation of traps within the dielectric. These defects may eventually join together and form a conductive path through the stack in a process known as TDDB, or oxide breakdown. Breakdown has been a cause for increasing concern as gate dielectric thicknesses are scaled down to the one nanometer range, because a smaller critical density of traps is needed to form a conducting path through these thin layers, and stronger electric fields are formed across gate insulators when voltages are not reduced as aggressively as device dimensions. The scaling of the physical dimensions of gate stacks can now be slowed or reversed with the introduction of high-k dielectrics, but TDDB remains a critical aging mechanism in those materials [4-5]. As shown in Fig. 1, CMOS devices suffer from BTI, HCI, and TDDB stress under standard digital operating conditions. We will now move on to demonstrate how on-die circuits can be used to measure the effects of those mechanisms.

III. Beat Frequency Detecting Silicon Odometer

The Silicon Odometer beat frequency detection system measures small frequency changes in stressed ROSCs with the concept illustrated in Fig. 2. This figure allows us to visualize the beat frequency between pairs of signals, using low speeds for clarity in this example. The faster signal catches up to the slower one, they overlap, and then the faster one pulls ahead. This repeats, and the time between the overlapping points is the period of the beat frequency. When the 63 Hz signal is superimposed on the 64 Hz signal, the beat period is (64 Hz - 63 Hz) = 1 Hz (*note the 1 second horizontal axis*). With 62 Hz and 64 Hz, the period is (64 Hz - 62 Hz) = 2 Hz.

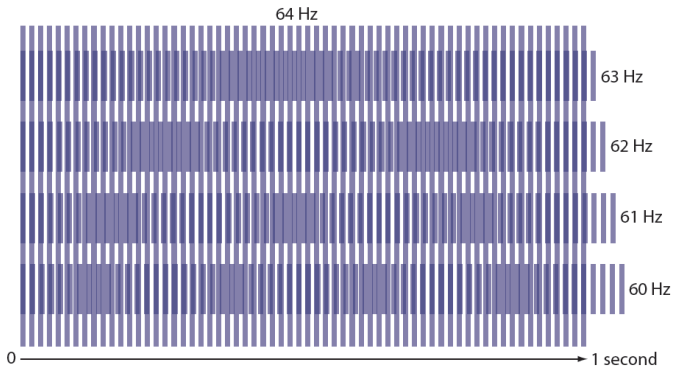


Fig. 2. The beat phenomenon between two ROSCs (ring oscillators) switching at different speeds is illustrated here with low-frequency signals. *(Figure from David Schneider of IEEE Spectrum.)*

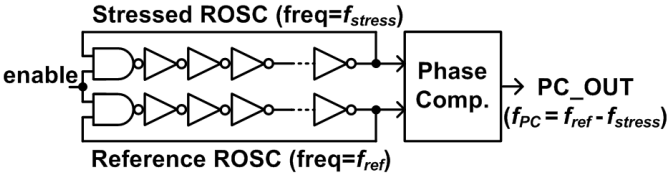


Fig. 3. Beat frequency detection system for measuring small differences in ROSC frequencies [6-8].

Therefore by measuring the beat frequency, we can ascertain the difference between two faster frequencies.

We monitor that beat frequency using the circuit in Fig. 3. During the Odometer measurements, a phase comparator uses a fresh reference ROSC to sample the output of an identical stressed ROSC. The reference, whose supply is set to 0 V during stress periods, allows us to cancel out the effects of temporal voltage or temperature shifts during experiments. The output signal of this phase comparator exhibits the beat frequency: $f_{PC} = f_{ref} - f_{stress}$. A counter is used to measure the beat frequency by counting the number of reference ROSC periods during one period of the phase comparator output signal. Given that simple digital output after each measurement, we can quantify the aging-induced shift in the stressed ROSC as follows.

If the initial frequency of the reference ROSC is called f_{ref}, that of the fresh ROSC to be stressed is f_{stress}, and the initial Odometer output count is N_1, then assuming f_{ref} is higher than f_{stress}, we have:

$$1/f_{ref} \cdot N_1 = 1/f_{stress} \cdot (N_1 - 1) \quad (1)$$

The $(N_1 - 1)$ term arises from the fact that the stressed ROSC with the lower frequency, f_{stress}, will take one less period to cycle back to the same point in the reference ROSC period while both are oscillating. After a stress period ends, f_{ref} will remain unchanged, but f_{stress} will be decreased due to aging, and we call the new frequency f_{stress}'. We also have a new output count (N_2), so the resulting equation is:

$$1/f_{ref} \cdot N_2 = 1/f_{stress}' \cdot (N_2 - 1) \quad (2)$$

Using these two equations, we can calculate the frequency shift during stress as follows:

$$\frac{f_{stress}'}{f_{stress}} - 1 = \frac{N_1 \cdot (N_2 - 1)}{N_2 \cdot (N_1 - 1)} - 1 = \frac{(N_2 - N_1)}{N_2 \cdot (N_1 - 1)} \quad (3)$$

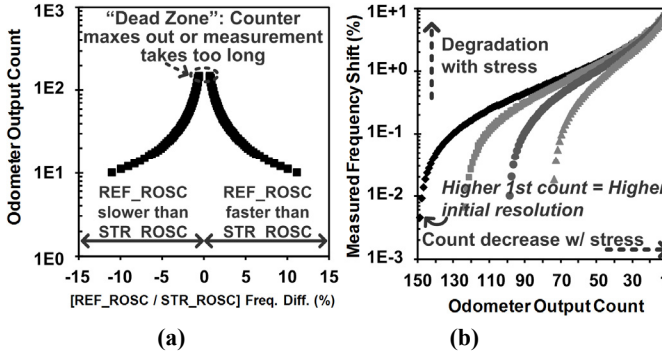


Fig. 4. (a) Silicon Odometer output count vs. the frequency difference between the reference and stressed ROSCs. (b) Frequency shift during a stress experiment vs. output count.

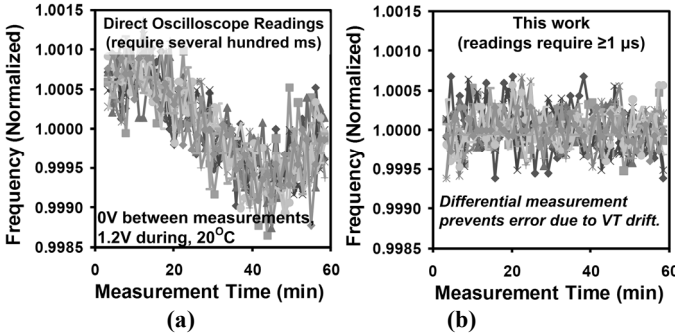


Fig. 5. Error (i.e., deviation from 1.0) in (a) oscilloscope and (b) faster Odometer measurements during no-stress experiments.

The Odometer count relationship with the difference between the ROSC frequencies is illustrated in Fig. 4(a). The Odometer operates correctly with a reference that is either slower or faster than the stressed ROSC. In the former case, the count will increase with stress, while it decreases in the latter. A slower reference is accounted for in equations (1) through (3) by changing the $(N_{\#} - 1)$ terms to $(N_{\#} + 1)$, because the faster stressed ROSC in this case goes through *one more* period than the slow reference during the beat frequency measurement, rather than *one less*. Additionally, it is possible for the reference to transition from being slower than to faster than the stressed ROSC, but this involves moving through a "dead zone" where the count will either equal the counter max value, or if the counter is large enough, the measurement time will become excessively long as the difference between the two ROSC frequencies becomes extremely small.

We chose to start our experiments with a reference frequency that is slightly faster than the stressed ROSC frequency, so that we obtained a monotonic decrease in the output counts with stress. This allowed us to maximize the frequency measurement resolution in the early phases of stress, and to avoid the dead zone. Fig. 4(b) shows measurement result characteristics with monotonic count decreases, and four different initial counts. We achieved maximal starting counts of ~125 in our hardware measurements, which corresponds to initial frequency shift measurements ranging down to 0.0065%. The resolution decreases with time, but we are primarily concerned with the small initial degradation steps that can be obtained with stress that is closer to real operating conditions. It has been shown that stress at excessively high voltages, for example, can lead to unrealistic degradation characteristics that are not useful for predicting device lifetimes under standard operating conditions [9-10].

Although this Odometer is capable of high resolution measurements, noise sources on-chip and in the measurement setup modify this benefit. In order to quantify the impact of noise and to compare the beat frequency system with direct ROSC frequency readings taken by an oscilloscope, we performed no-stress experiments on a test chip implemented in 65nm technology, so ideally there should be no frequency shift. Fig. 5(a) was recorded by a 100 MHz, 1.25 GS/s oscilloscope, after the frequencies of ten ROSCs were divided down by 1024 on-chip. We see a worst case error of 0.18%, and a drift in the measured values due to some slight change in operating conditions. Fig. 5(b) shows a smaller worst case error of 0.07% in the frequency calculated by the Odometer, along with the fact that this differential system eliminates the effects of variations common to both the reference and stressed ROSCs. Similar error floors were found during repeated tests, setting the lower bound on frequency shifts that they can measure. Finally, note that the automated oscilloscope readings required >500 ms, while the Odometer measurements take down to 1 µs in this case [8], or less in other implementations [7]. As stated earlier, fast measurements are required in order to avoid unwanted BTI recovery when stress conditions are removed for measurements.

The ideal minimum Odometer measurement time is set by the output count multiplied by the measured ROSC period, or 125x3 ns = 375 ns in one recent test circuit [7]. However, in this automated scheme, the first two counts are generally smaller than the correct result due to the unpredictable starting location of the measurement at some mid-point in the phase comparator period, so they are discarded. Therefore, the true minimum measurement time is that required to record the first two smaller, erroneous counts plus the correct third result. We verify that the third count is correct during calibration by using an externally controlled longer measurement period in which the initial smaller counts are overwritten by subsequent results in a bank of three eight bit result registers whose contents are scanned out for post-processing. In this case, all counts should be roughly identical, and equal to the third result we record during the shorter automated measurements. We included logic in our system which sends the circuit back into stress immediately after the three results are recorded, in order to achieve measurement times of 1 µs or less [7].

The general testing procedure for beat frequency measurement Odometers begins with a calibration process in which a small initial difference between f_{ref} and f_{stress} is ensured with scan chain-controlled trimming capacitors. After that, a fresh pre-stress measurement is recorded and the counter result described earlier in this section is scanned out. Stress is applied to the ROSCs under test as soon as the count is recorded (*before scan out*) to minimize recovery time. Stress is then interrupted periodically to take new measurements and the calculations described above are used to calculate the aging-induced frequency shift throughout the experiment.

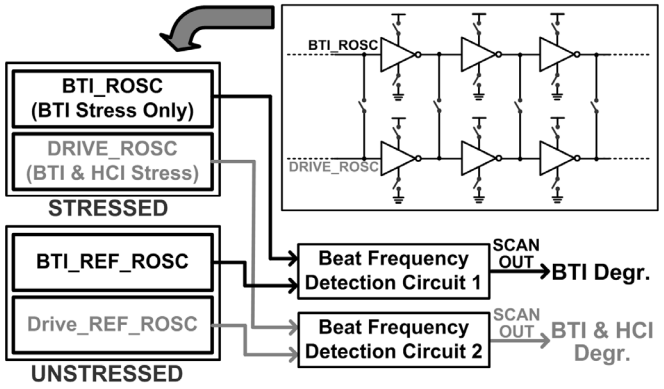


Fig. 6. Proposed system for separately monitoring BTI- and HCI-induced frequency degradation.

IV. Circuit Technique for Separately Monitoring BTI and HCI

In this section we present an implementation of the beat frequency Odometer which discerns between BTI and HCI degradation [7]. Digital logic undergoes both BTI and HCI stress during normal operation as shown in Fig. 1. Therefore the circuits-based HCI/BTI measurement design must focus on isolating the effects of these two mechanisms. We accomplish that task with a pair of ROSCs using a "backdrive" concept in which one ROSC drives the transitions in both structures during stress, such that the driving oscillator ages due to both BTI and HCI, while the other suffers from only BTI.

A block diagram of our proposed design is shown in Fig. 6. This circuit contains four ROSCs in total: two stressed, and two unstressed to maintain fresh reference points. Each of the stressed oscillators is paired with its identical, fresh reference during measurements, and its frequency degradation is monitored with the Silicon Odometer beat frequency detection circuit.

Fig. 7 presents the pair of stressed ROSCs in both (a) stress and (b) measurement modes. During stress, the BTI_ROSC stages are gated off from the power supplies, while the DRIVE_ROSC maintains a standard inverter configuration with the supply set at VSTRESS. Both ROSC loops are opened, and the input of the DRIVE_ROSC is driven by a stress clock generated by an on-chip voltage controlled oscillator (VCO) whose output is level-shifted up to VSTRESS. The switches between these two ROSCS are closed so the DRIVE_ROSC can drive the internal node transitions for both structures.

Simulated waveforms from stress mode are shown in Fig. 7(c). The internal nodes of the BTI_ROSC switch between the supply level (VSTRESS) and 0 V, as would be the case in standard operation. However, the peak drain current though the "on" devices in this structure is only 3-5% of that in the DRIVE_ROSC, since their sources are gated off from the supplies. Note that the sources of these "on" devices in the stressed BTI_ROSC are held at their respective supply levels due to the backdriving action of the DRIVE_ROSC. Therefore, the BTI_ROSC will age due only to BTI stress, while the DRIVE_ROSC suffers both BTI and HCI. We can extract the contribution of HCI to the latter ROSC's frequency degradation with the equation $HCI_{DEG} = DRIVE_{DEG} - BTI_{DEG}$,

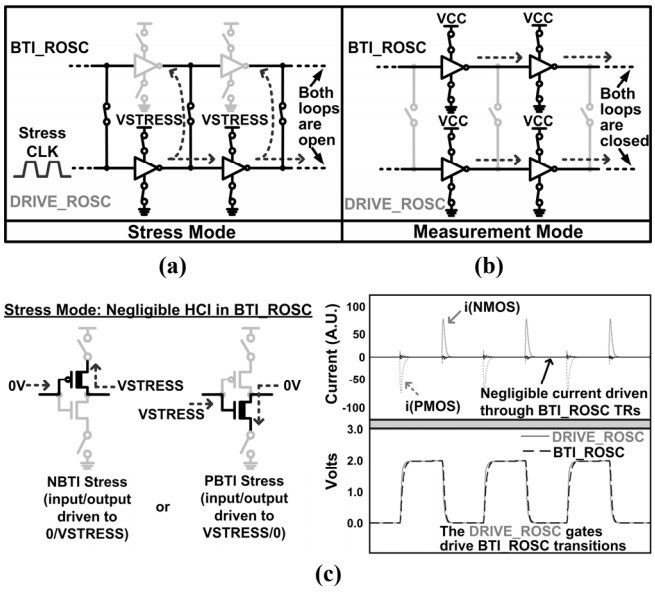


Fig. 7. ROSC configuration during (a) stress and (b) measurement modes. (c) The BTI_ROSC transistors suffer the same amount of BTI as the DRIVE_ROSC transistors during stress, but with negligible HCI degradation.

where DEG stands for degradation. During measurement periods, both ROSCs are connected to the power supply (VCC) and the switches between them are opened, so they each operate in a standard closed-loop configuration.

A test circuit was implemented in a 65 nm bulk CMOS process for concept verification. Fig. 8 presents example results for both ROSCs under 2.4V stress, as well as the calculated degradation due to HCI (HCI_{DEG}). As expected, both BTI and HCI degradation follow a power law behavior, although the latter is seen to saturate at long stress times.

Fig. 9(a) illustrates the impact of frequency on BTI and HCI. These results verify that BTI is at most weakly dependent on frequency, while HCI degrades with increased switching activity. Both aging mechanisms degrade with voltage (Fig. 9(b)), and we observe a decrease in HCI's power law exponent at lower voltages. This has been explained by a possible decreasing contribution of broken Si-O bonds (in comparison to Si-H bonds) at lower voltages, closer to real operating conditions [11-12]. Note the crossover point when HCI begins to dominate the aging is pushed out in time by an order of magnitude at 1.8 V stress compared to 2.4 V. This helps to illustrate the claim that BTI becomes dominant in modern technologies operating at lower supply levels.

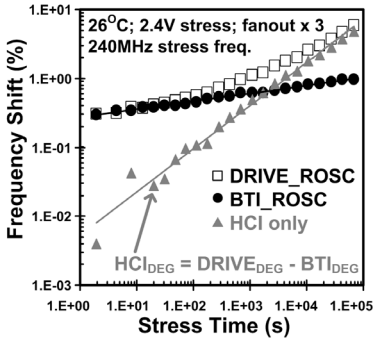
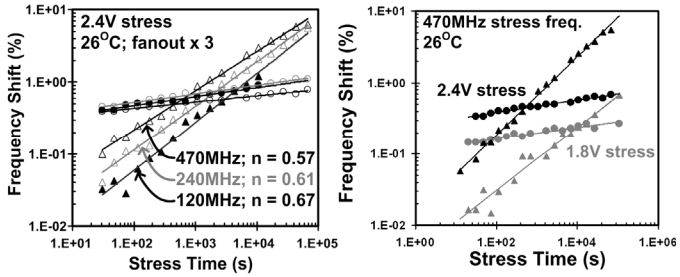


Fig. 8. Example measured results with AC stress conditions.



(a) (b)

Fig. 9. Measured frequency degradation results for (a) three stress frequencies and (b) varied stress voltage.

V. An Array-Based Odometer System for Statistical Circuit Aging Characterization

Variations in the number and characteristics of charges or traps contributing to transistor degradation lead to a distribution of device "ages" at any given time. This issue is well understood in the study of time dependent dielectric breakdown, but is just beginning to be thoroughly addressed under bias temperature instability and hot carrier injection stress. In this section we present a measurement system that facilitates efficient statistical aging measurements involving the latter two mechanisms in an array of ring oscillators. The distribution of frequencies is monitored by three Silicon Odometer beat frequency detection systems working in parallel [8].

A block diagram of the proposed design is shown in Fig. 10. The references are identical to the ROSCs within the array (Fig. 11), and are left unstressed to maintain fresh reference points in the Odometers' differential measurement setup. Ten inverters in each ROSC are 1.2 V thin oxide logic devices. These stages will age during stress experiments, while the rest of the stress and timing control logic is composed of 2.5 V thick oxide I/O transistors, so it is not significantly impacted. Measurements are taken during circuit calibration to calculate the percentage of the fresh full loop delay accounted for by the logic devices under test (DUT). Later, the total frequency shift of each stressed full loop measured by the Odometers is divided by the percentage of the fresh delay taken by the DUTs in order to calculate the degradation in those thin oxide stages. All DUT stages have identical loads and layouts. During stress, the ROSC loops are opened so that their frequencies can be controlled by an on-chip voltage controlled oscillator (VCO). When each oscillator is selected for a measurement, its supply is set to the standard digital level of 1.2 V, the loop is closed, and its frequency shift is measured by the three Odometer systems.

Silicon Odometers provide high-resolution Δf measurements when the frequencies of the ROSC under test and reference are close because this results in a low beat frequency, and hence, a high output count as discussed in Section III. This is ensured with trimming capacitors. However, in the present circuit where many ROSCs are stressed in parallel and selected one-by-one for measurements, controlling the trimming bits in each stressed oscillator would be time and area consuming. Therefore, we instead hardwired nine of fifteen capacitors "on" in each of those ROSCs, while

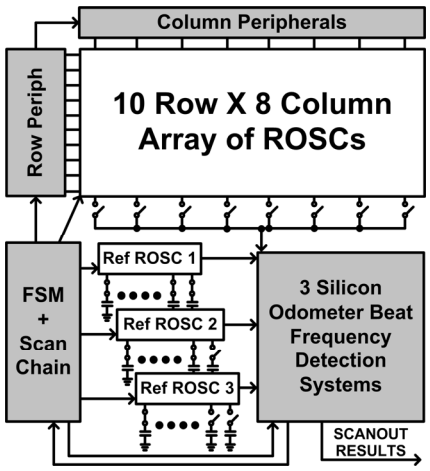


Fig. 10. Reference ROSCs have 15 trimming capacitors controlled by the scan chain. Stressed ROSCs are taken out of stress individually for measurements using the FSM and Peripheral circuits.

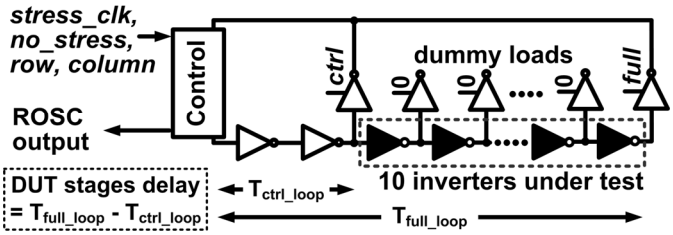


Fig. 11. Basic structure of the ROSC cells. Stages colored black use thin oxide logic devices. All others are 2.5V I/O devices.

individually controlling all fifteen in the three references. The Odometers associated with those references all record output counts corresponding to the beat frequency for each ROSC measurement (Figs. 10 and 12). During post-processing, the highest-resolution degradation characteristic is selected from that set for each ROSC that was stressed.

PDFs of fresh DUT frequencies are shown in Fig. 13 with the resulting distributions after 3.1 hours of DC stress. The primary degradation characteristic at work in these experiments was NBTI, since PBTI is not significant with SiO_2 dielectrics [3], and there was no switching during stress.

In Fig. 14(a) we see that there was no significant correlation between the fresh ROSC frequency and the stress-induced shift. This lines up with previous findings that the stress-induced V_{th} mismatch in PMOS pairs was uncorrelated to the

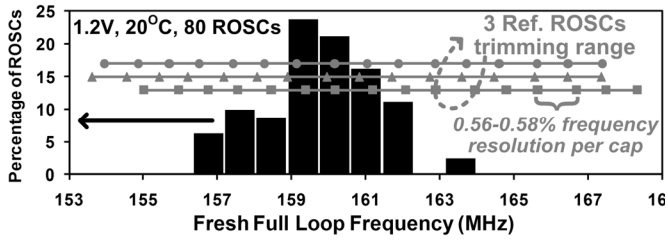


Fig. 12. Fresh full loop frequency distribution with Reference ROSC trimming range. The reference ROSCs are trimmed to positions in the distribution such that we maximize the resolution of the degradation characteristics gathered from each experiment.

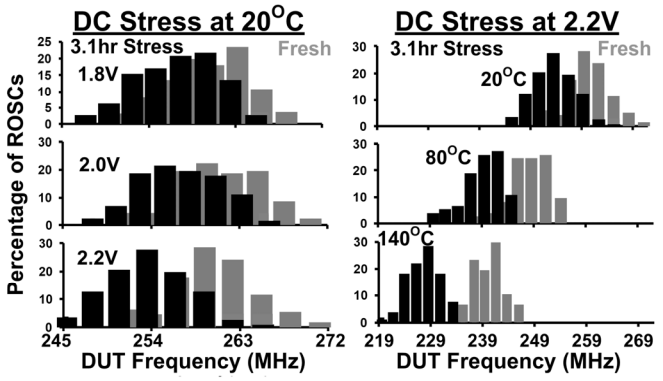


Fig. 13. Shift in frequency distributions after 3.1 hour stress. Each 20°C distribution was gathered from 120 ROSCs, while those at higher temperatures came from 80 due to a limited number of dies.

initial mismatch [13], and that the initial spread in the V_{th} is not correlated to that caused by aging [3]. Fig. 7(b) shows the μ (mean) frequency shifts and the σ (standard deviation) of the shifts vs. stress time. The σ increases with stress, roughly following a power law with an exponent (n) of just under 1/2 that of the μ shift. Therefore, this σ(Δf)/μ(Δf) ratio decreases with stress time.

VI. Test Circuit for Automated Gate Dielectric Breakdown Characterization

In this section we give a brief overview of a circuits-based method for cost and time effective TDDB characterization. Most of the previously published TDDB measurement results were gathered from individual device probing experiments. The equipment used in those tests can be expensive, and each device may have to be tested serially. Given the need for up to thousands of samples to correctly define the Weibull slope of the T_{BD} distribution [10], [14], that serial testing process quickly becomes cumbersome.

Therefore, in the circuit presented here, DUTs are stressed in parallel and we continuously loop through the array, temporarily removing stress conditions in one cell at a time and measuring each DUT's gate current. In addition, the array format is a convenient method to study any spatial correlation of TDDB without requiring elaborate test setups. Test array structures like this are gaining popularity as an efficient way to gather process technology information, since individual device probing is not convenient when large numbers of readings are required [15-16].

Fig. 15 shows our TDDB characterization system consisting of a 32x32 array of structures we call "stress cells" that contain the DUTs, whose gate currents (I_G) are periodically measured using an Analog-to-Digital (A/D) current monitor and on-chip control logic [17]. Note that our first implementation of that cell, as seen in Fig. 16, only applies inversion mode stress. After an initialization sequence, cells are cycled through automatically without the need to send or decode cell addresses, in order to simplify the logic and attain faster measurement times. The stress cell was implemented to facilitate the accelerated stressing of the DUTs by using thick oxide I/O transistors in the supporting circuitry to avoid excessive aging or breakdown in these other devices. A switch drives the DUT gate to the stress voltage if the cell has been turned on for a stress test.

Automatic measurements were completed with LabVIEW™ software and a National Instruments data acquisition board connected to a laptop. During a pre-stress calibration procedure, the current monitor is run normally, as it would during stress measurements, but with a range of known off-chip resistance values. This step allows us to map DUT gate resistance values to the circuit's digital outputs, and hence would enable the tracking of any progressive gate breakdown. However, we observed hard (i.e., abrupt and total) breakdowns exclusively in our automated array measurement as well as individual device probing experiments on the 130 nm bulk technology used here.

Cumulative distribution functions (CDF) of the time to breakdown, both on a standard percentage scale as well as the Weibull scale, are displayed in Figs. 17(a) and 9(b),

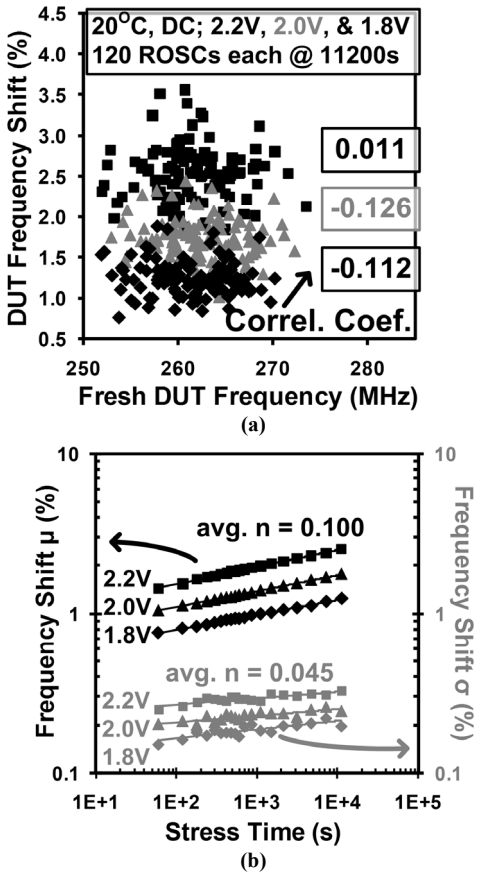


Fig. 14. (a) No significant correlation was found between the stress-induced Δf and the fresh frequencies. Pae *et al.* found that the initial spread in the threshold voltage is not correlated to the shift caused by aging [3]. (b) The mean and standard deviation of Δf both increase with stress time.

respectively. The Weibull slope values are in good agreement with other published data [10], [18].

Test arrays such as ours, where a large number of devices are closely spaced, facilitate investigations of any spatial correlation in the process or characteristics being studied. For example, spatial correlation of gate oxide thicknesses could lead to a correspondingly correlated breakdown process [19]. The spatial distribution of T_{BD} in a 20x20 portion of a test

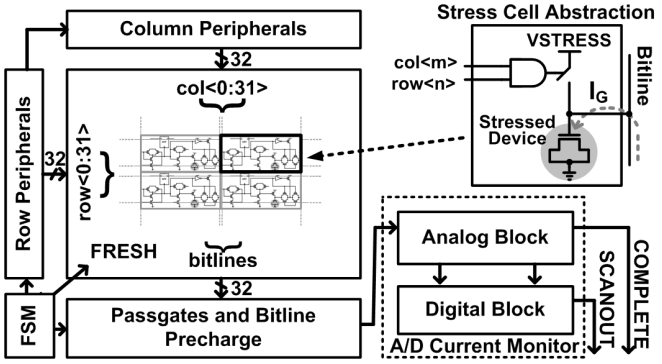


Fig. 15. 32x32 array for automated gate dielectric breakdown characterization.

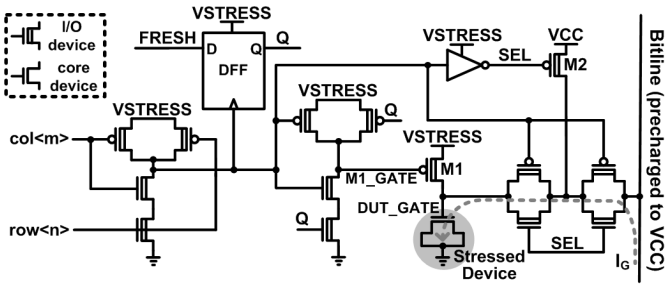


Fig. 16. Inversion mode stress cell with bitline leakage compensation and stress/no-stress capability.

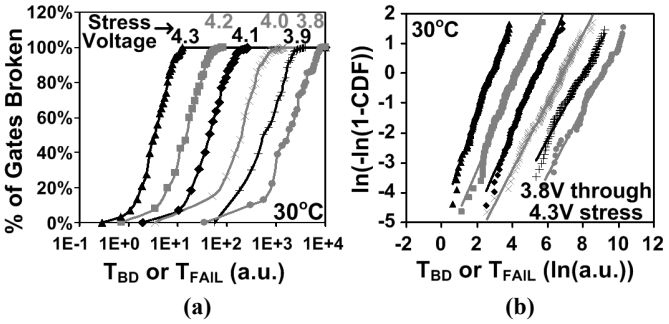


Fig. 17. Measured T_{BD} CDFs on (a) a percentage scale and (b) a Weibull scale.

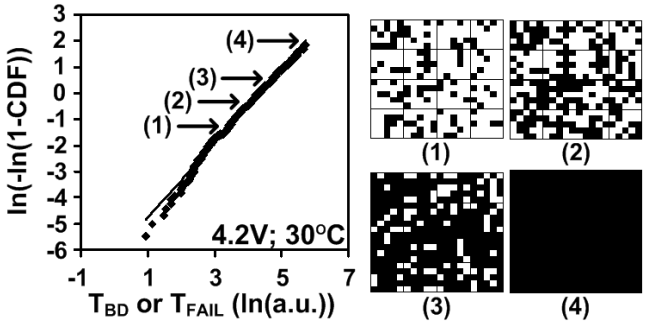


Fig. 18. Spatial T_{BD} distribution in a stress cell array at four time points on the Weibull scale CDF.

array stressed at 4.2 V is plotted along with the corresponding Weibull distribution in Fig. 18. The four spatial diagrams correspond to the four divisions of the Weibull plot representing 25% of the cells each. No spatial correlation is apparent from these plots, and this was quantified with a Moran's I analysis of the data [17].

While time dependent dielectric breakdown (TDDB) in transistor gates has traditionally been studied under inversion-mode stress conditions, ultra-thin dielectrics can also suffer breakdowns in the off-state when the channel is not inverted [9], [20], [21]. This off-state stress becomes particularly problematic under excessively high drain biases, such as those occurring during burn-in screening, or in certain I/O circuits where a transition is made into a higher voltage domain. In another test circuit we implemented two new stress cell designs that facilitate inversion mode as well as several off-state tests, showing that the framework discussed in this section can be readily expanded upon [22].

VII. The Role of On-Die Aging Monitors in Medical Electronics Reliability Management

As is the case in other fields of electronics, there is a push for smaller form factors, more memory, and increased processing bandwidth in medical devices. This has led manufacturers to move to newer scaled CMOS technologies when possible. However, the reliability standards for these devices remain stringent, which poses a particularly arduous set of challenges. As stated earlier, the shrinking device sizes and voltage margins in advanced technologies makes circuits more susceptible to suffering both soft and hard failure due to aging. Therefore, medical technology firms, even more so than manufacturers of other consumer electronics, require time- and cost-efficient methods to characterize reliability mechanisms on their own custom test vehicles. They are also prime candidates to consider in-situ monitors that are embedded in products in the field.

The focus of our work has been on implementing and demonstrating the utility of on-die aging characterization circuits geared towards test vehicles rather than the in-situ space. The precision and timing resolution of our beat frequency detection Odometer makes it well suited to record aging data at low stress conditions that do not distort aging characteristics like some high stress tests. In addition, most implantable medical electronics use high V_{th} devices and run at low voltages, so small changes in the margin between those values can have a significant impact on performance, making measurement precision critical. It also may facilitate studies of gradual aging in the subthreshold regime, which is a topic that remains largely unexplored. The array-based measurement systems for ROSC aging and TDDB facilitate high volume testing without invasive probing. Using these on-die tools, medical technology manufacturers can more easily gather reliability data that may not be readily available from the fab.

In order to account for failure distribution tails due to specific use and environmental conditions, or to dynamically adjust voltage and frequency based on real-time data in a closed loop sensor system, reliability engineers are naturally interested in the in-situ solution as well. Any such new designs would complement existing on-product failure analysis tools, as design for failure analysis is already a crucial concept in medical devices [23]. These circuits must be compact and very low power, particularly in applications such as implantable medical electronics. Ring oscillators and digital delay lines have already been used as embedded process variation or environmental condition monitors both on

test vehicles and products in the field [24-28]. Our beat frequency detection system fits in to that design space and can be used to improve the timing and measurement resolution of ROSC frequency readings. Other published work has focused more specifically on the practicality and design of compact embedded device aging monitors [29-31].

VIII. Conclusions

In this review paper we have discussed a number of unique circuits that demonstrate the benefits of utilizing on-chip logic and a simple test interface to automate transistor aging characterization. In addition to avoiding the use of expensive probing equipment, implementing on-chip logic to control the measurements enables a better combination of measurement and timing resolutions. This is critical when interrupting stress to record BTI measurements, as that mechanism is known to recover within microseconds or less. The high frequency resolution of the beat frequency detection Odometer allows us to obtain aging data at low stress conditions, close to or matching those of normal operation. Next, the silicon area needed to collect statistical data is significantly reduced compared with traditional device probing, as multiple test structures can share the same read-out circuitry and I/O pads. Finally, the compact all-digital circuit structures could enable circuit prognostics in real product designs, and eventually lead us down the path to enhanced real time adaptation.

In conclusion, recent developments on-chip degradation monitors indicate that these systems can play a critical role in understanding the circuit-level aging behavior in nanoscale devices. This capability will allow chip manufacturers to develop techniques to avoid wasteful overdesign and frequency guard banding based on pessimistic degradation projections, and hence more fully realize the benefits of CMOS scaling while ensuring that products remain fully operational for their intended lifetimes.

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