# Impact of Interconnect Length on BTI and HCI Induced Frequency Degradation

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# Purpose

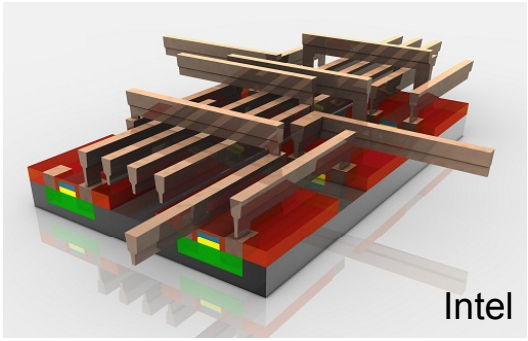
- Explore the dependence of BTI and HCI induced aging on interconnect length
- Design a dedicated on-chip aging monitor for interconnect paths
- Develop BTI and HCI aging models applicable to interconnects

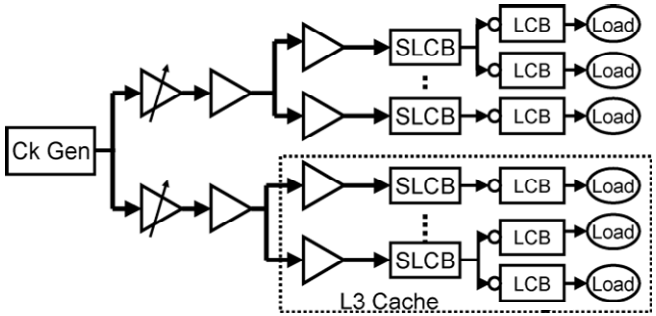
# Outline

- **Interconnect Driver Aging**
- ***All-in-one* Silicon Odometer**
- **Test Chip Design and Results**
- **Aging Models for Interconnect Drivers**
- **Summary**

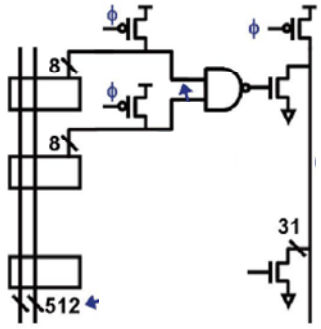
# Interconnect Driver Aging

- **Global interconnects**
  - **Clock networks**
  - **Memory wordlines and bitlines**
  - **Signal buses, etc**
- **Aging mechanisms**
  - **Front-end: BTI, HCI, TDDB**
  - **Back-end: EM, ILD breakdown**
- **Aging impact on interconnect fabrics**
  - **Clock skew worsens**
  - **Slew rate degrades**
  - **$f_{max}$ degrades**
  - **Duty cycle modified**



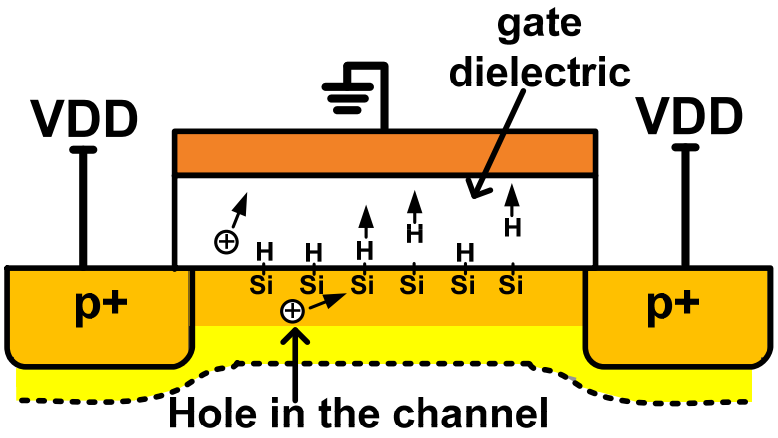




S .Tam, et al., JSSC 2004

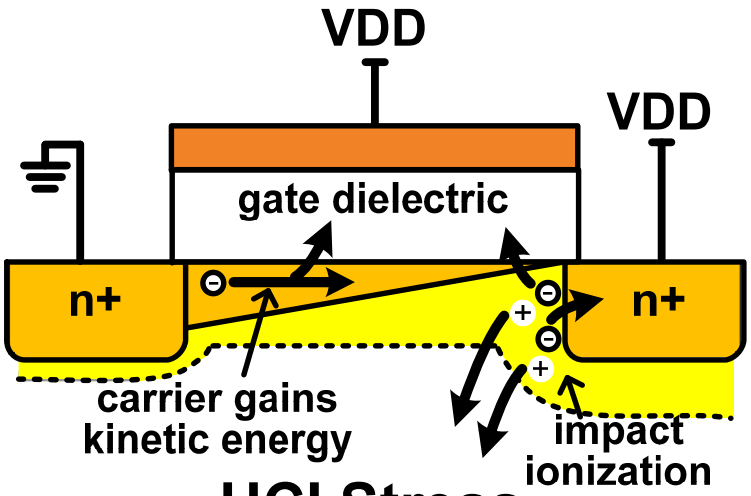



L. Chang, et al., VLSI Sym. 2007

# BTI and HCI Mechanisms



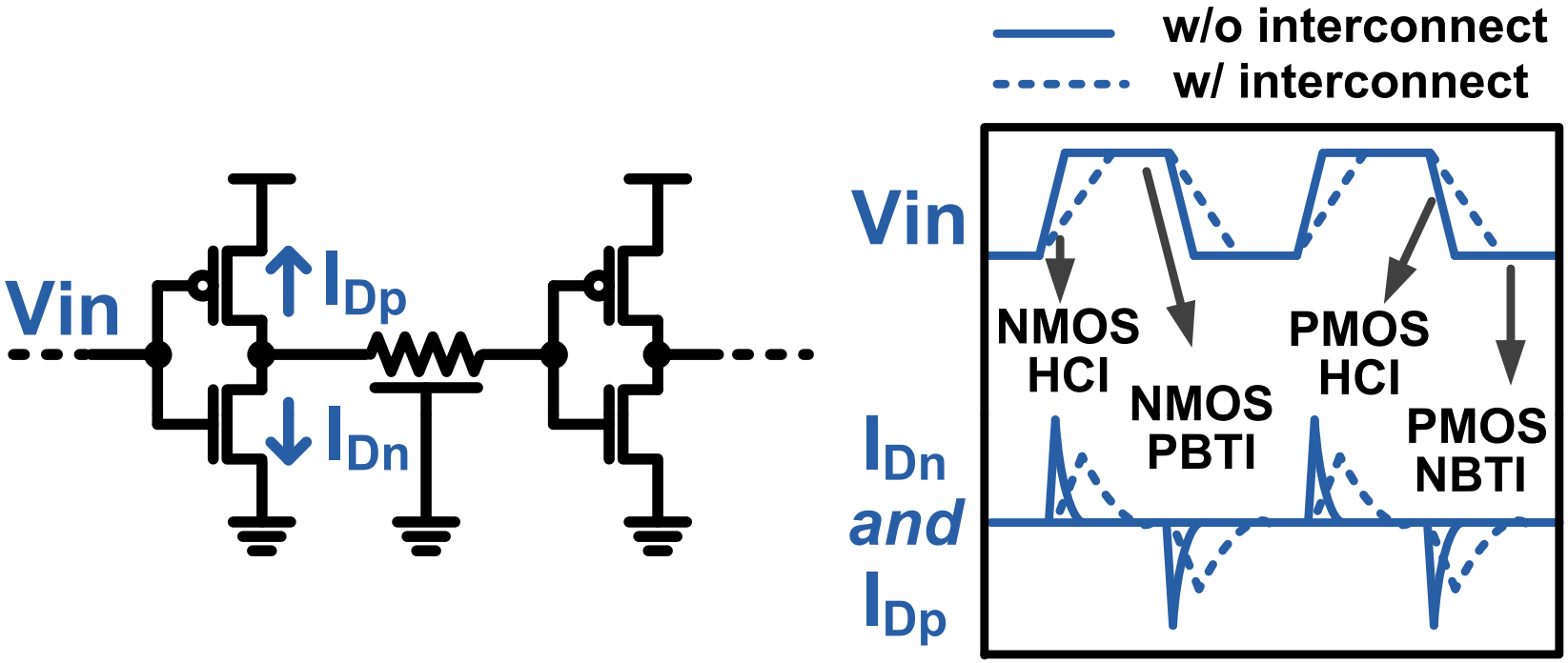

NBTI Stress




HCI Stress

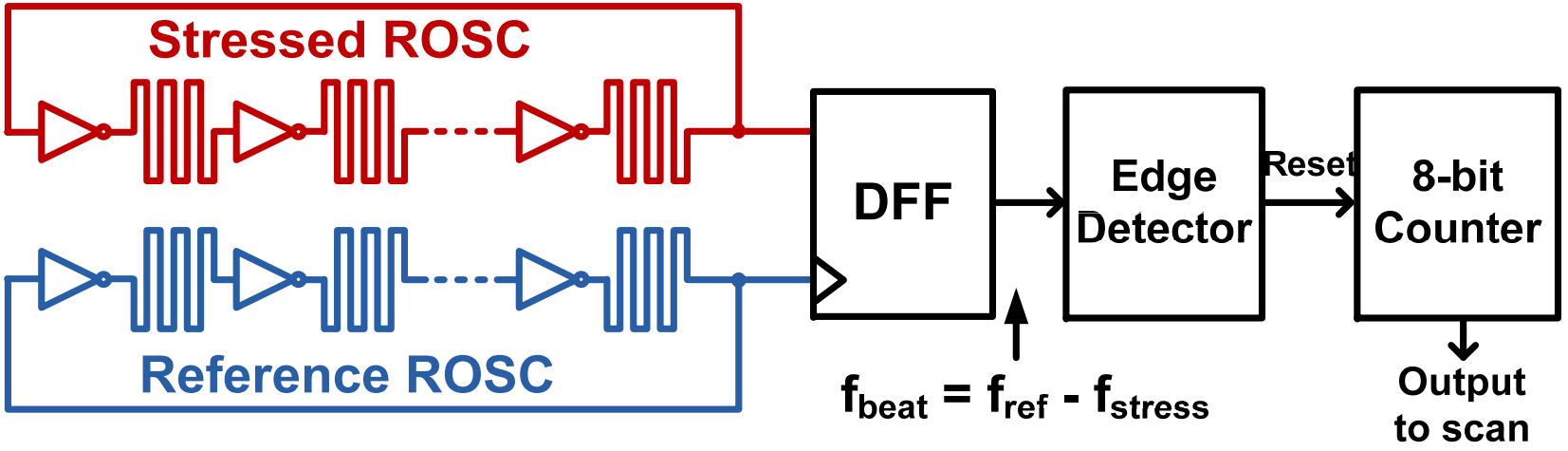
- NBTI: Holes in the channel facilitate the breaking of Si-H bonds, traps generated at the oxide interface
  - Occurs when the channel is in strong inversion mode
  - Fast recovery (<10μs) when the device is turned off
- HCI: Energetic carriers causes dielectric degradation
  - Occurs when current is passing through the channel

# Motivation for Studying Interconnect Aging




- Interconnect affects the voltage and current shapes
  - Increased transition time (decreased slew rate)
  - Increased current pulse; decreased current peak value
- BTI and HCI have different sensitivities to bias conditions

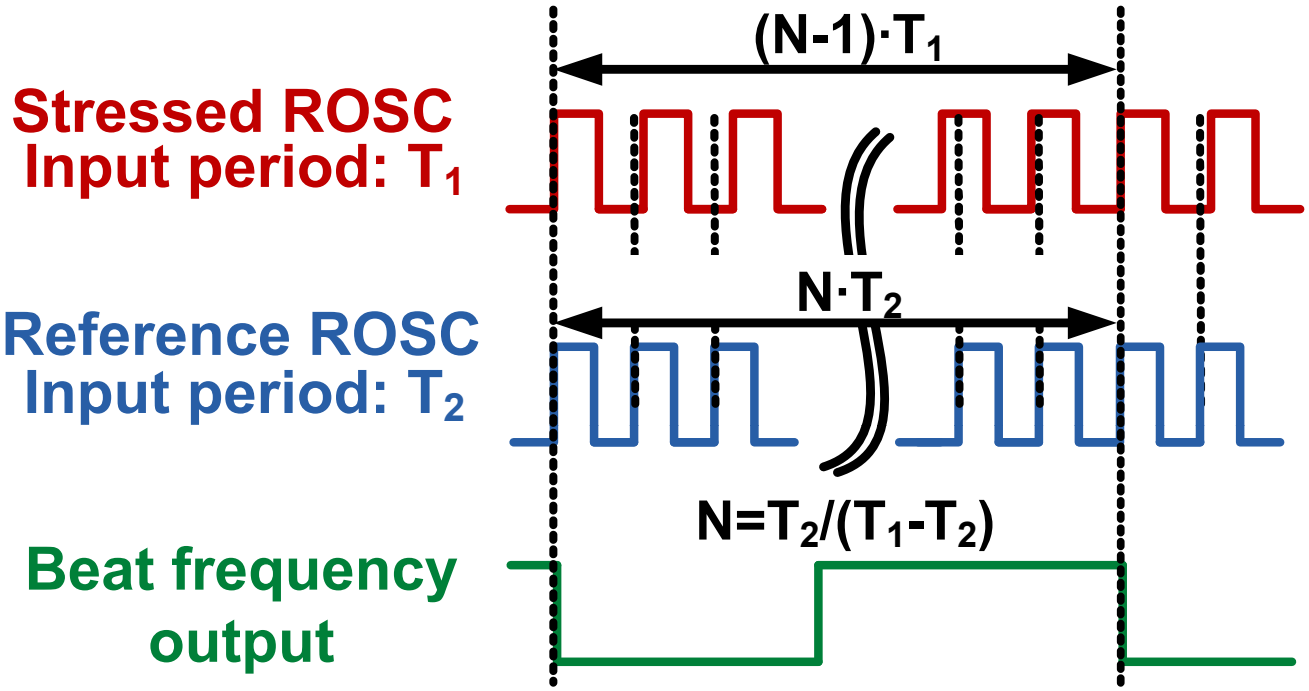
# Silicon Odometer Beat Frequency Scheme




T. Kim, *et al.*, JSSC, 2008

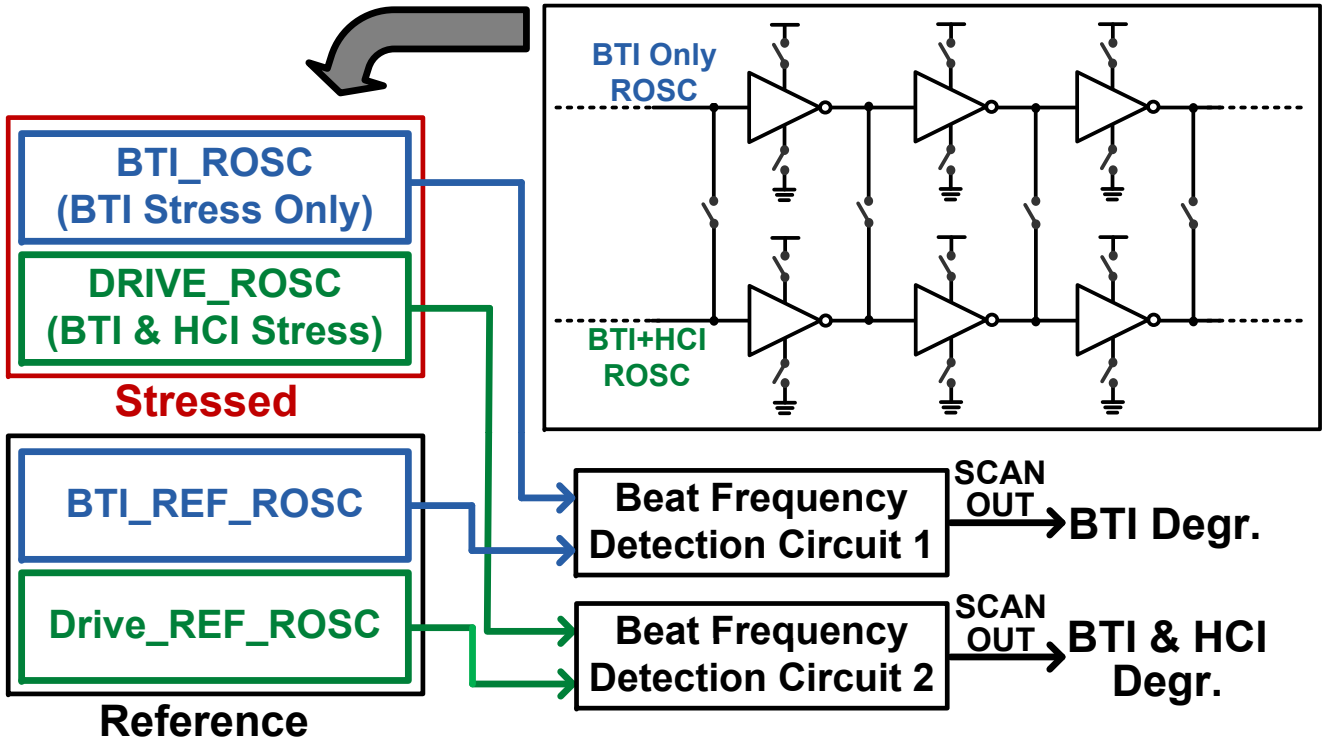
- Beat frequency of two free running ROSCs measured by DFF and edge detector
- Benefits of beat frequency detection system
  - Achieve ps resolution with μs measurement interrupt
  - Insensitive to common mode noise such as temperature drifts
  - Fully digital, scan based interface, easy to implement

# Beat Frequency Detection Concept




- Sample stressed ROSC output with reference ROSC
  - 1% delay different before stress → N=100
  - 1.01% delay different after stress → N=99
  - Minimum $\Delta f$ sensing resolution is 0.01%

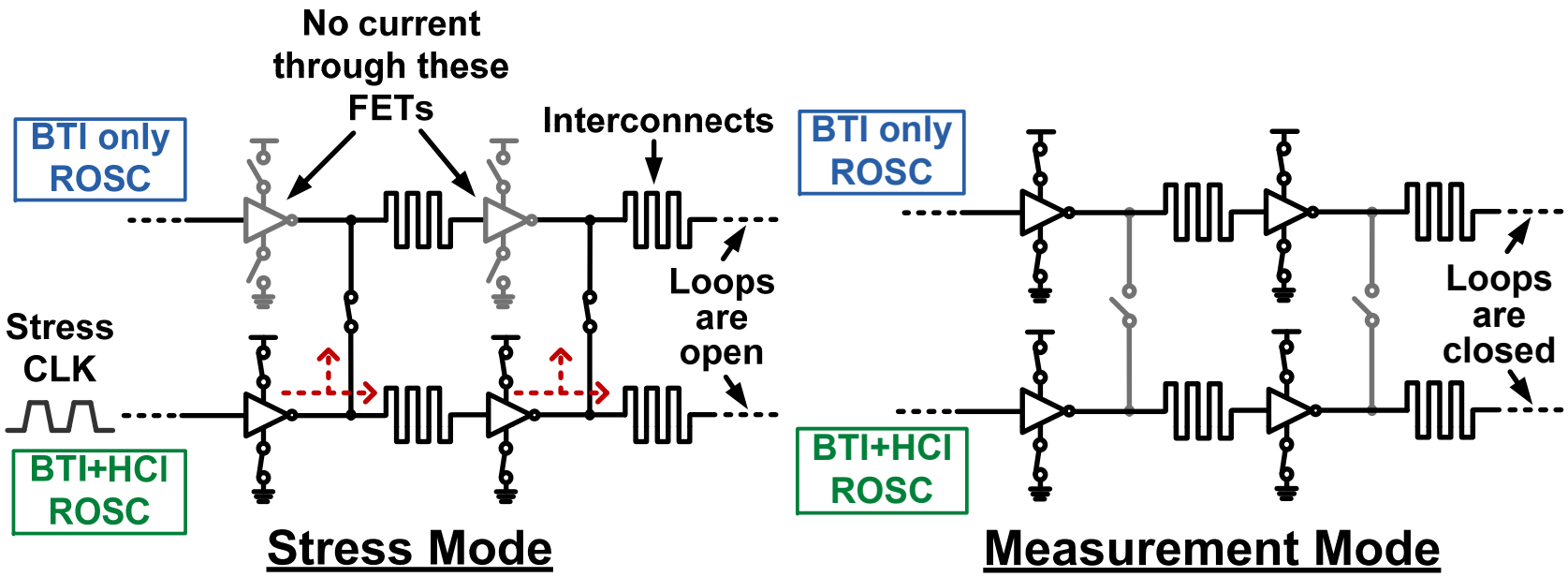
# All-In-One Silicon Odometer




J. Keane, *et al.*, VLSI Symp. 2009, JSSC 2010

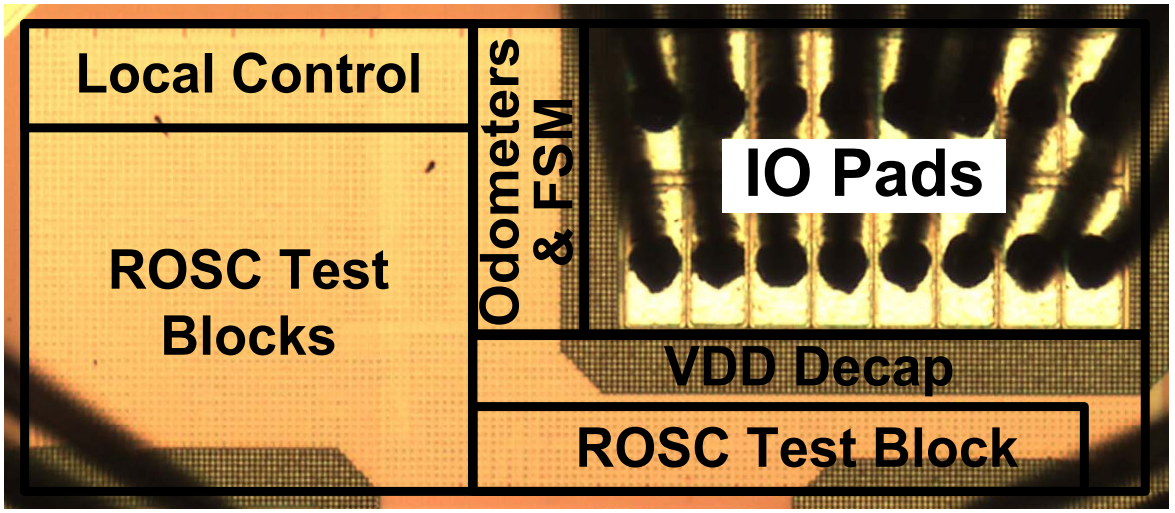
- 2 pairs of ROSCs: stressed pair and unstressed pair
- For the stressed pair, one ROSC suffers from BTI only; the other undergoes both BTI & HCI
- Two beat frequency detection systems

# Separating BTI and HCI



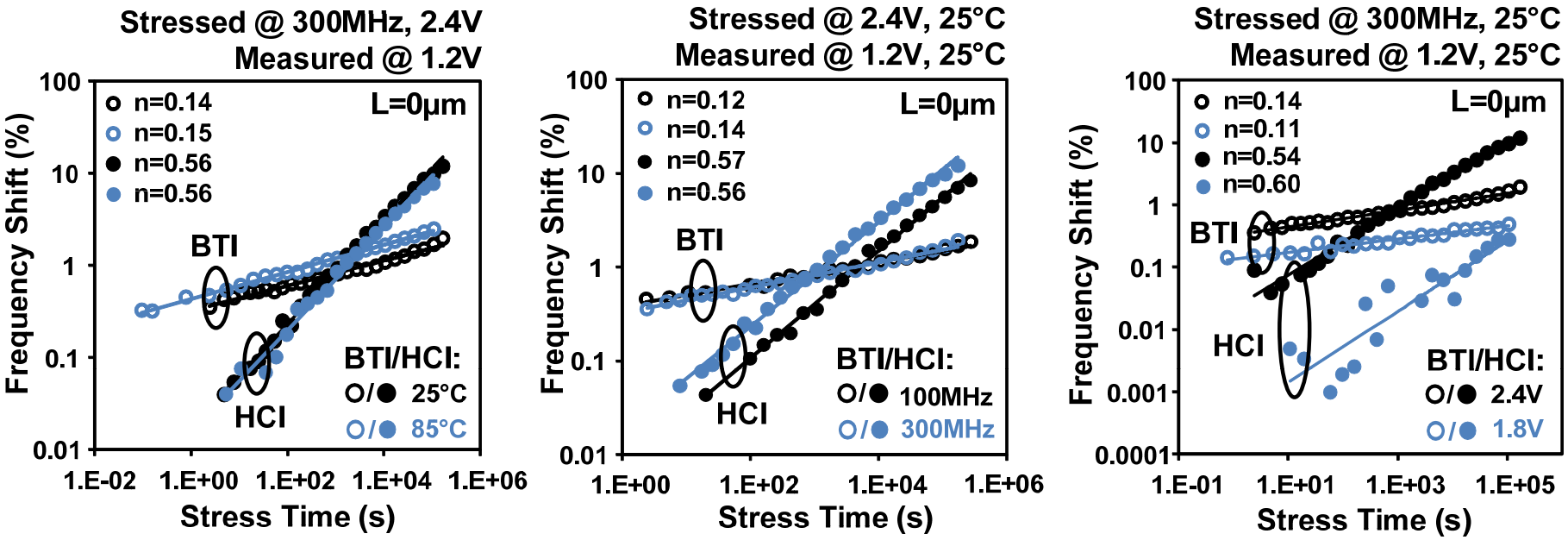

- **Stress mode: ROSC loops open**
  - **Top ROSC gated off from supply, no HCI stress**
  - **Bottom ROSC drives transitions**
- **Measurement mode: ROSC loops close**
  - **Both ROSCs are free running**
  - **Switches between them are open**

# 65nm Test Chip Die Photo and Features



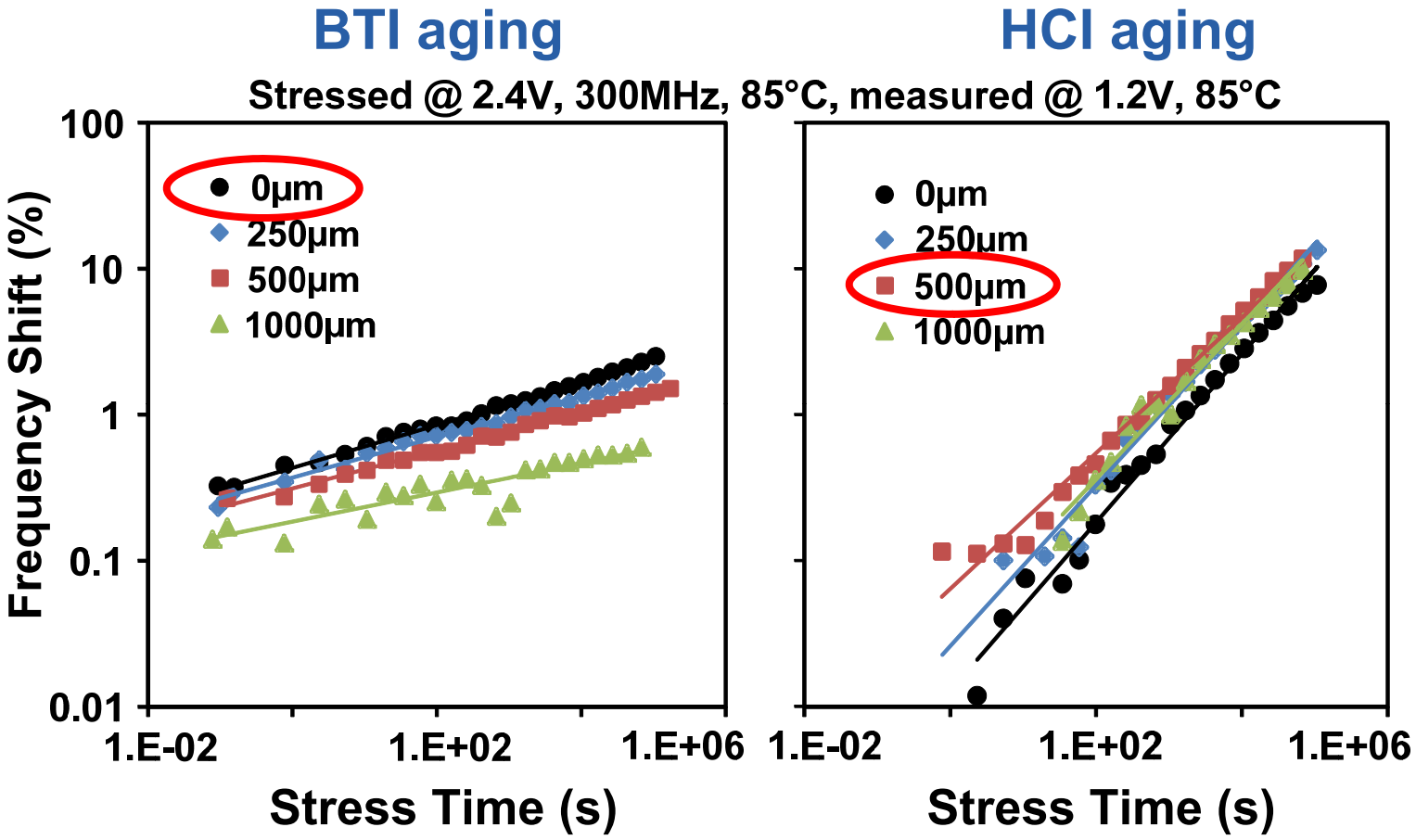

| | |
|---|---|
| Process | 65nm LP CMOS |
| Core / IO Supplies | 1.2V / 2.5V |
| Interconnect Length | 0µm, 250µm, 500µm, 1000µm |
| Interconnect Layer | M2, W=100nm |
| Interconnect RC | R=1.4Ω/µm, C=0.09fF/µm |
| Active Area | 0.182mm$^2$ |
| Δf Resolution | 0.016% |
| Meas. Interrupt | 3µs |

# BTI and HCI Aging: Without Interconnect



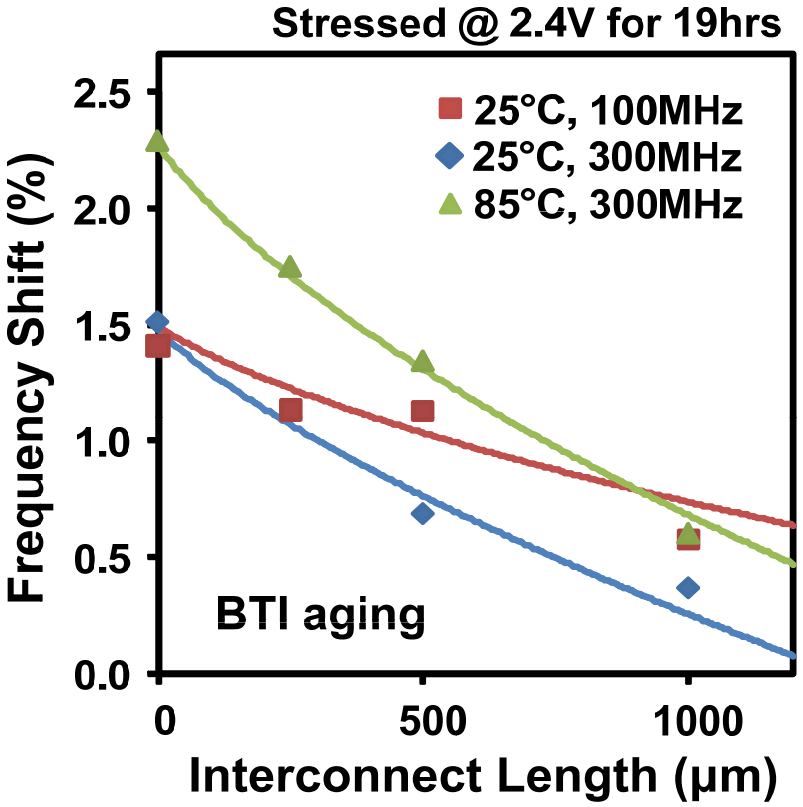

- **BTI is positively correlated with temperature; HCI is negatively correlated**
- **BTI is at best weakly dependent on frequency; HCI degrades with increased frequency**
- **BTI is less sensitive to stress voltage than HCI**

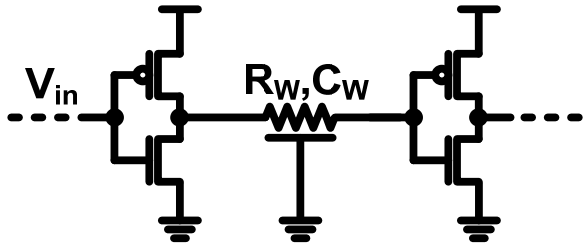
# BTI and HCI Aging: With Interconnect

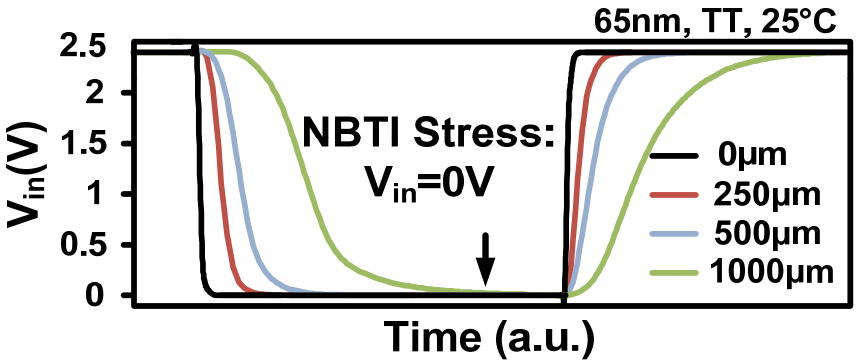



- BTI aging decreases with interconnect length
- HCI degradation peaks at L=500µm

# BTI Aging vs. Interconnect Length

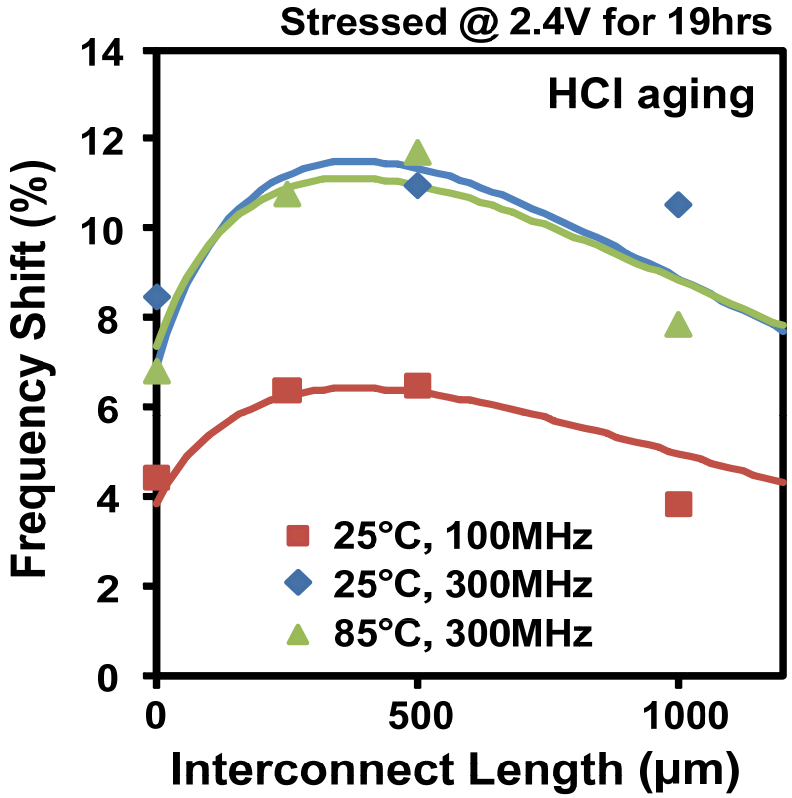


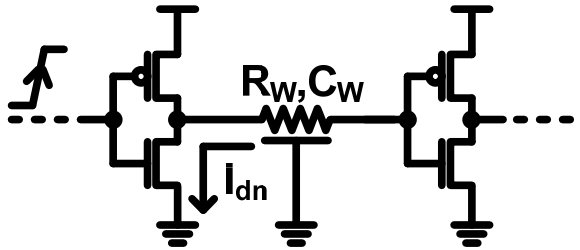



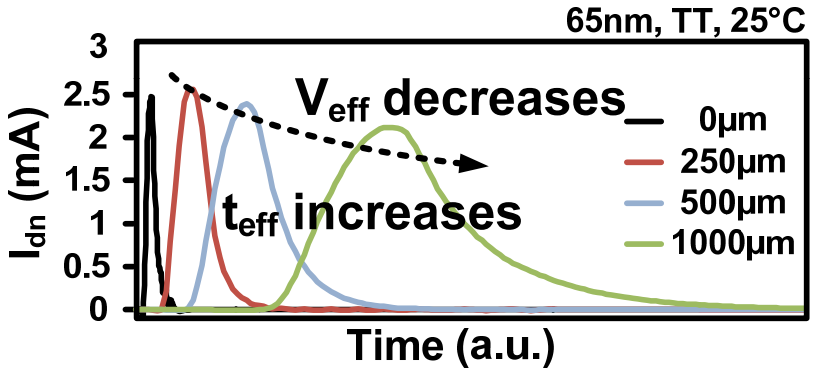




- BTI induced frequency degradation decreases with longer interconnect
- Longer transition time → shorter PMOS stress duration → Less BTI aging

# HCI Aging vs. Interconnect Length

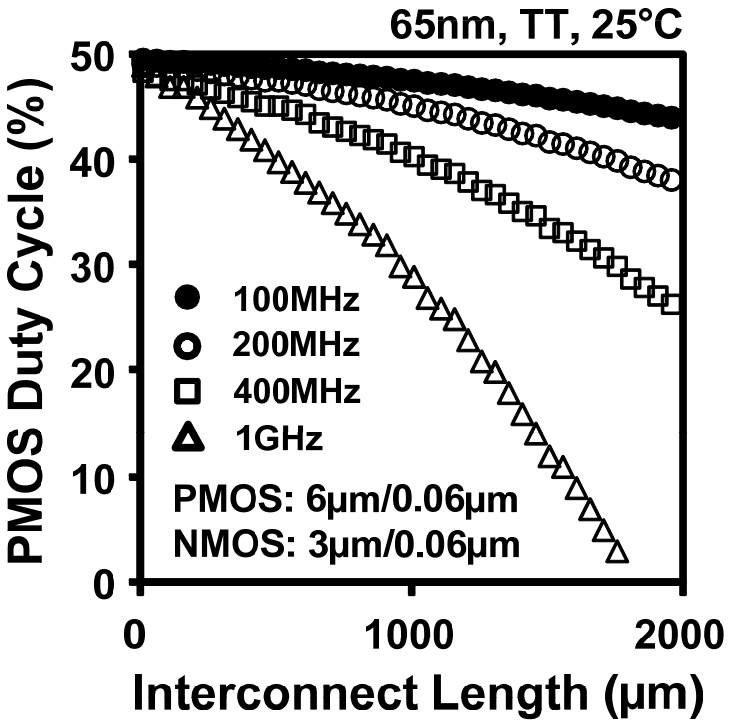


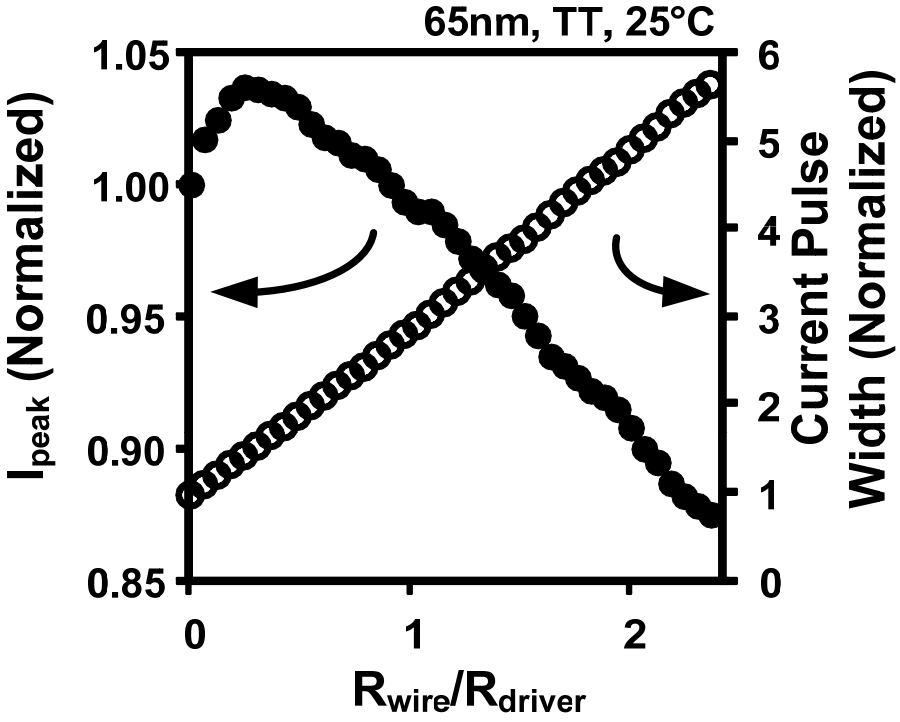




- HCI aging exhibits a non-monotonic behavior with respect to interconnect length
  - Current pulse width increases
  - Current peak decreases

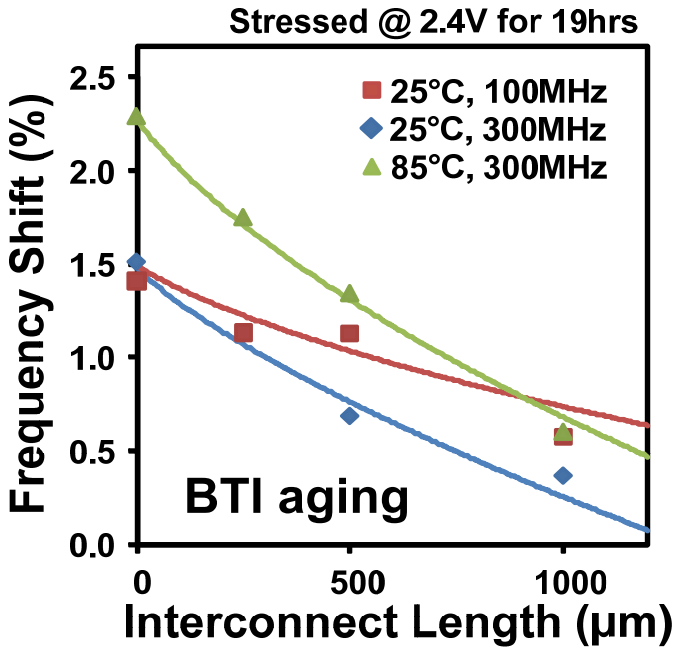
# Simulation Results

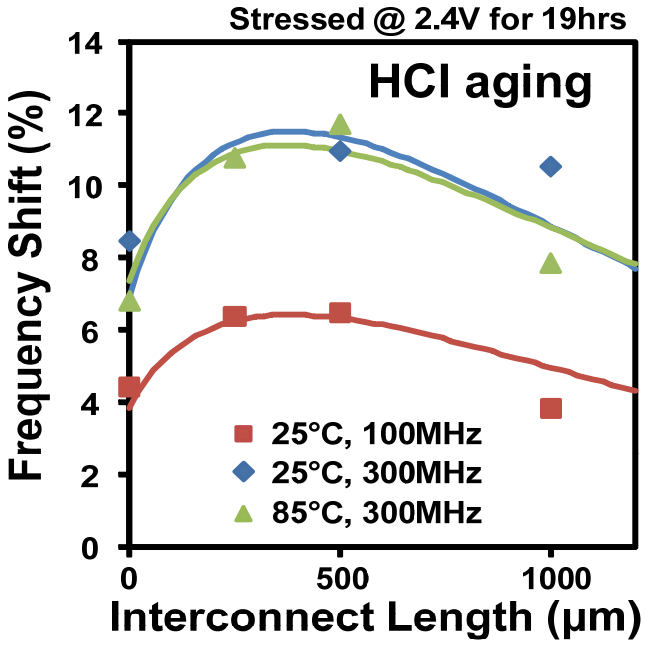



- **Left: Reduced BTI stress duty cycle**
- **Right: Lower $I_{peak}$ → decreased HCI stress voltage**
- **Right: Increased current pulse width → increased HCI stress time**

# Aging Models for Interconnect Drivers




$$(\Delta f/f)_{BTI} = \alpha[A\exp(\gamma V_{str})t^{n} - B(2t_T/T)^{k}]$$

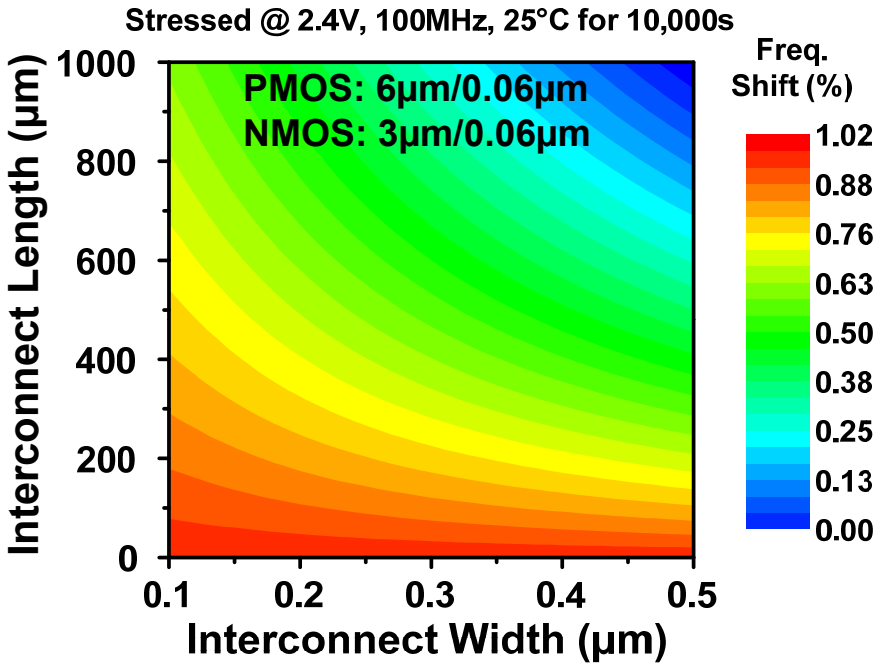
- $t_T$: transition time
  - $\approx R_{eq}(C_W+C_L)+R_W(C_W/2+C_L)$
- $\alpha$: wire delay sensitivity factor
  - $= \dfrac{R_{eq}(C_L+C_W)}{R_{eq}(C_W+C_L)+R_W(C_W/2+C_L)}$
- A: temperature related
- γ, B, k: empirical parameters
- n: BTI time exponent
- T: stress clock period
- t: BTI stress time

$$(\Delta f/f)_{HCI} = \alpha C\exp(-D/V_{eff})t_{eff}^{m}$$

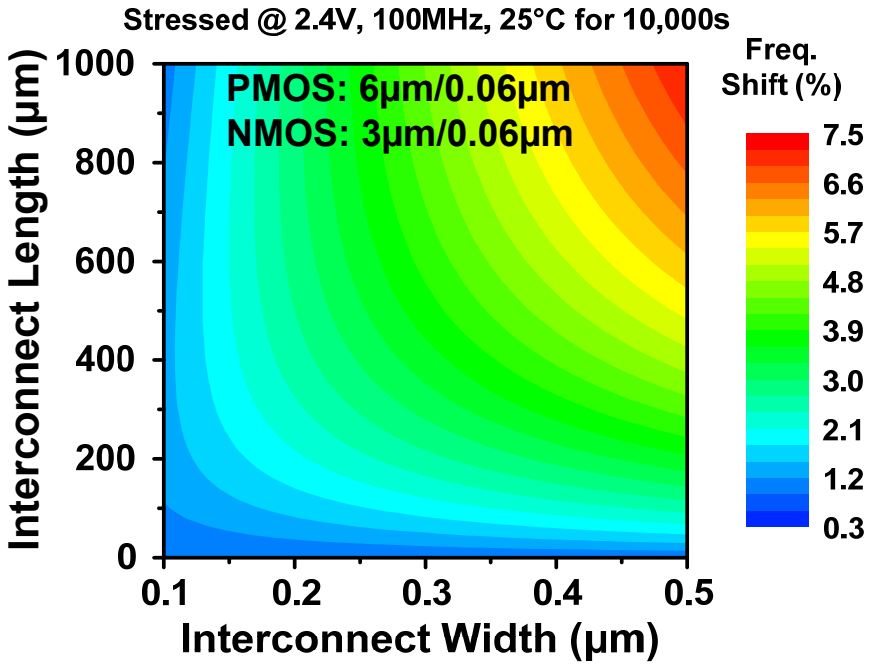
- $V_{eff}$: effective NMOS stress voltage
  - $= \dfrac{R_{eq}}{R_{eq}+R_W} V_{str}$
- $t_{eff}$: effective stress time
  - $= \dfrac{R_{eq}(C_W+C_L)+R_W(C_W/2+C_L)}{R_{eq}C_L}\, t$
- C, D: empirical parameters
- m: HCI time exponent
- t: HCI stress time
- α: sensitivity factor used in BTI case

# Interconnect Width and Length Dependency

## BTI




## HCI




- BTI reduced for larger interconnect L and W
- HCI generally worse for larger L and W
- Non-monotonic HCI dependence on L for small W

# Summary

- An odometer circuit designed to separately monitor BTI and HCI in long interconnects
  - 0.016% resolution with μs order measurement time
  - Insensitive to voltage and temperature drifts
- The dependence of BTI and HCI degradation on interconnect length explored for the first time
  - BTI decreases with longer interconnect
  - HCI shows non-monotonic dependence on interconnect length
- Proposed BTI and HCI models for interconnect drivers agree well with silicon data