An Array-Based Chip Lifetime Predictor Macro for Gate Dielectric Failures in Core and IO FETs

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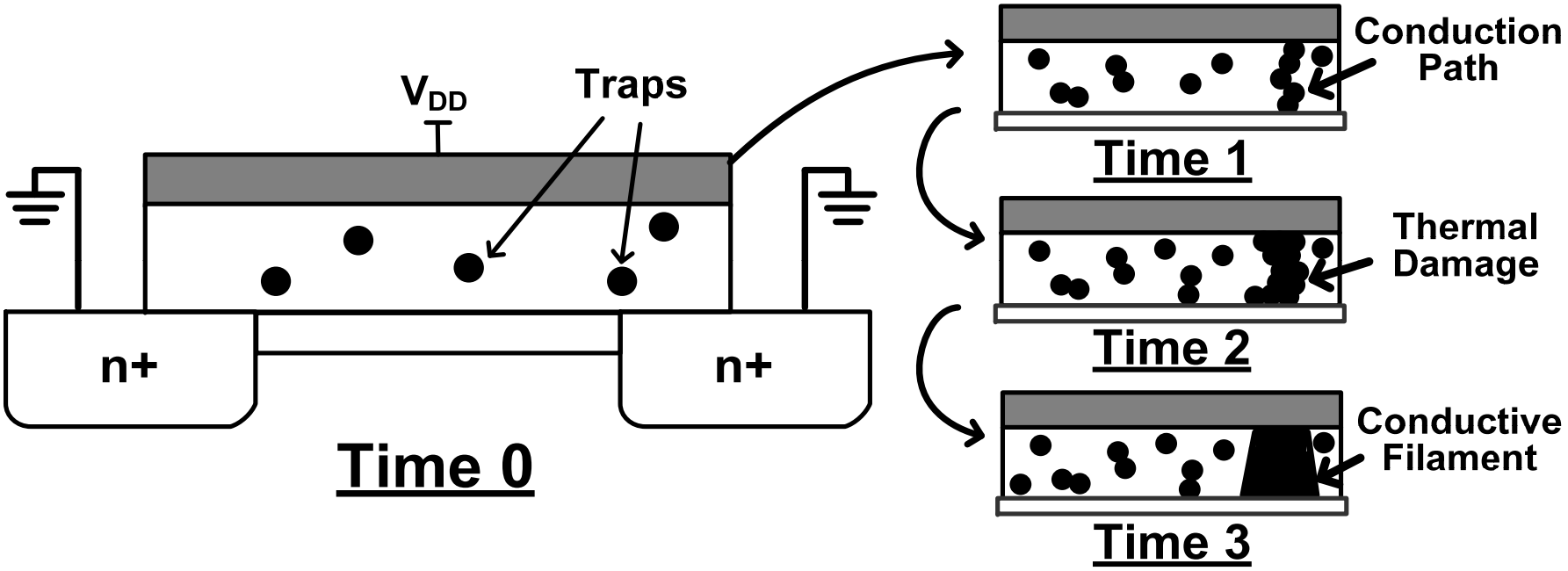
Presentation Agenda

- Introduction to TDDB Lifetime Prediction
- Proposed TDDB Test Macro Description
  - Flexible Stress Cell Design
  - IO Stress Cell Design
- TDDB Measurement Results
- Conclusion

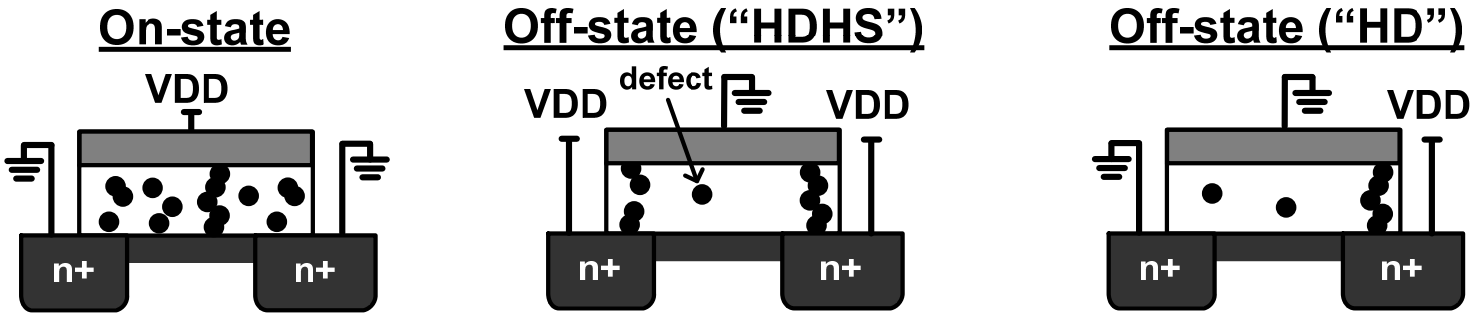
Introduction to TDDB

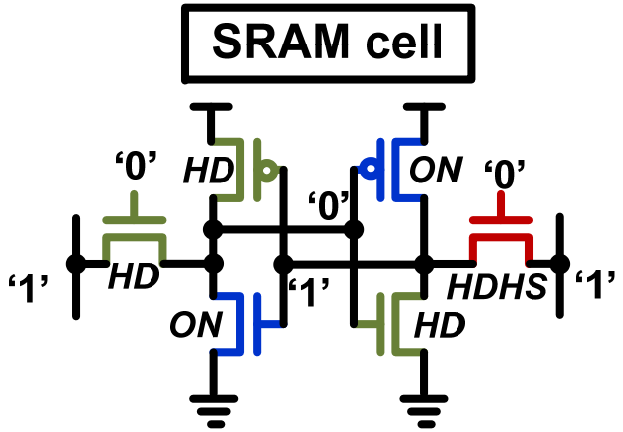
"Time Dependent Dielectric Breakdown"

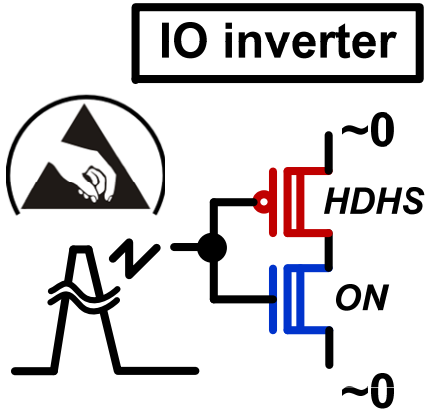


- Traps: Defects in dielectric, increase under electric field
- Traps overlap forming conductive path
- Gate dielectric no longer a reliable insulator
  - Parametric or functional failures

Different TDDB Manifestation

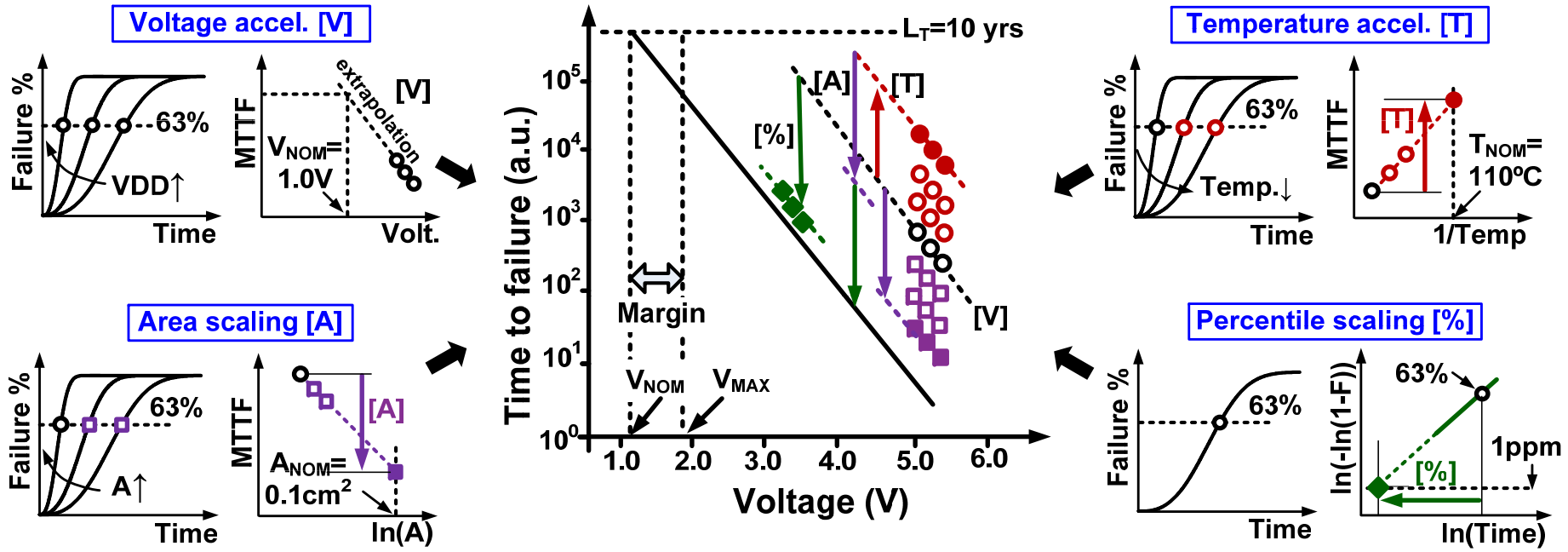






- Different modes of TDDB: on-state, off-state (HDHS, HD)
- Other modes important for structures like SRAM cells and IO inverters especially during burn-in/RF applications

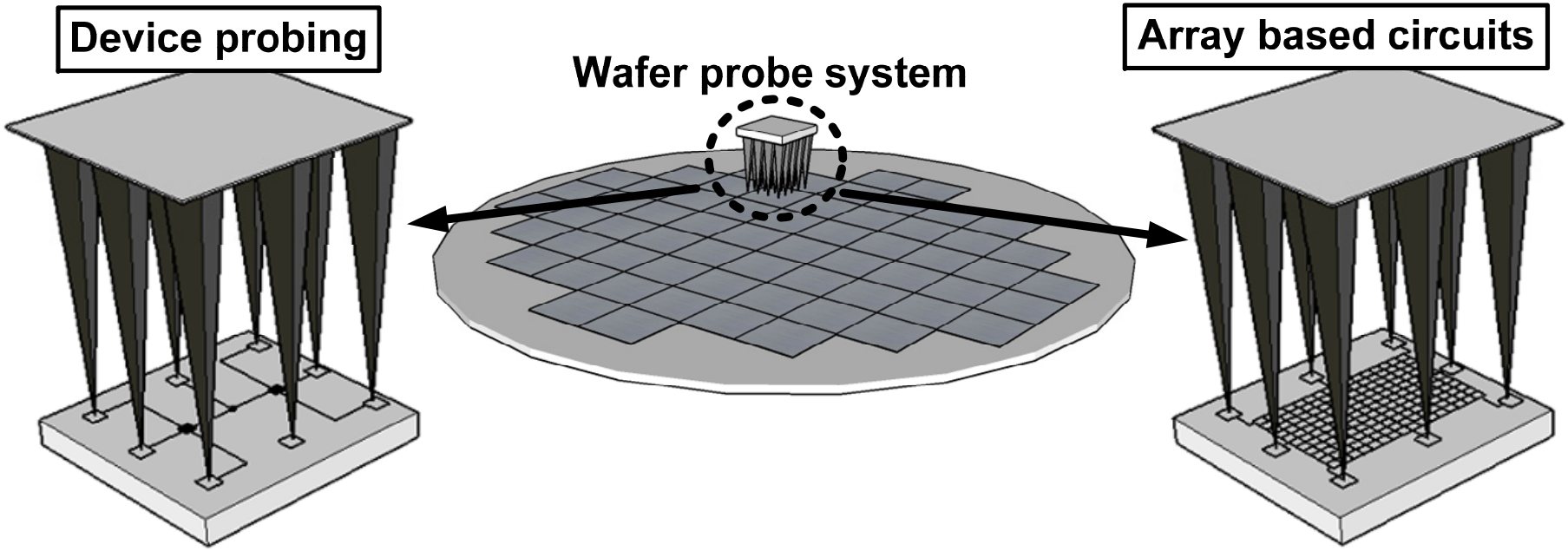
Chip Lifetime Prediction Methodology



- **Extrapolate stress results with respect to:**
  - **Op. conditions based on acceleration models**
  - **Larger chip areas (e.g., Poisson scaling for TDDB)**
  - **Lower percentiles based on chosen distribution**

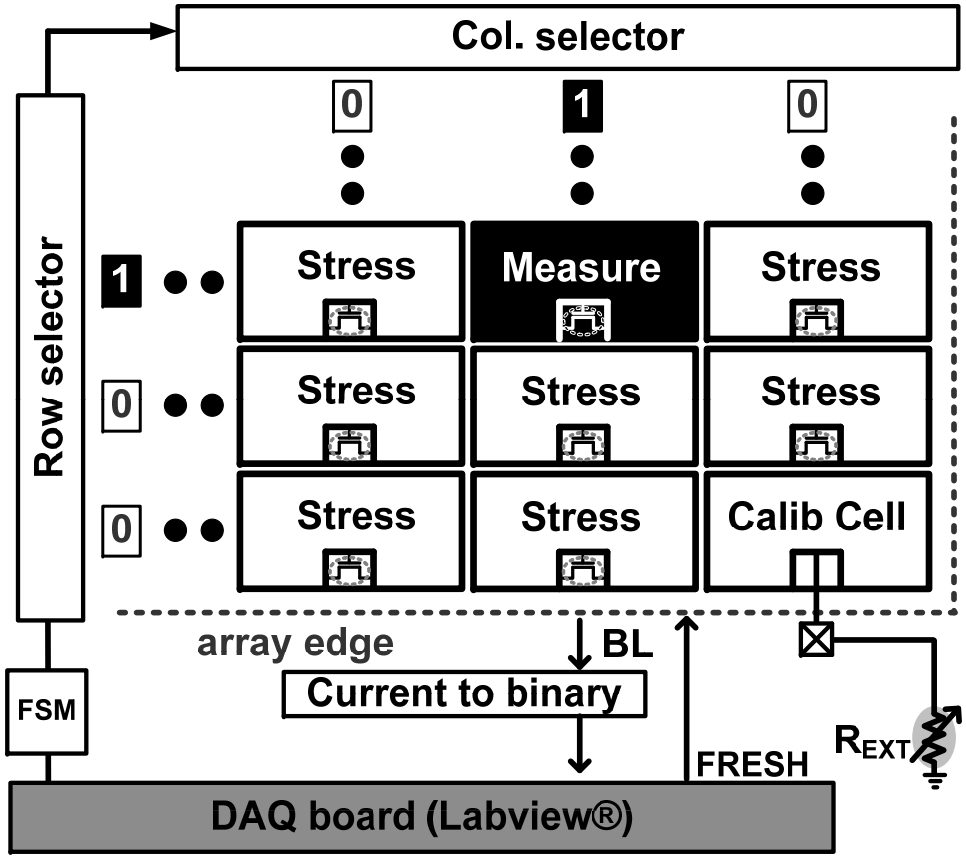
TDDB Characterization Methods

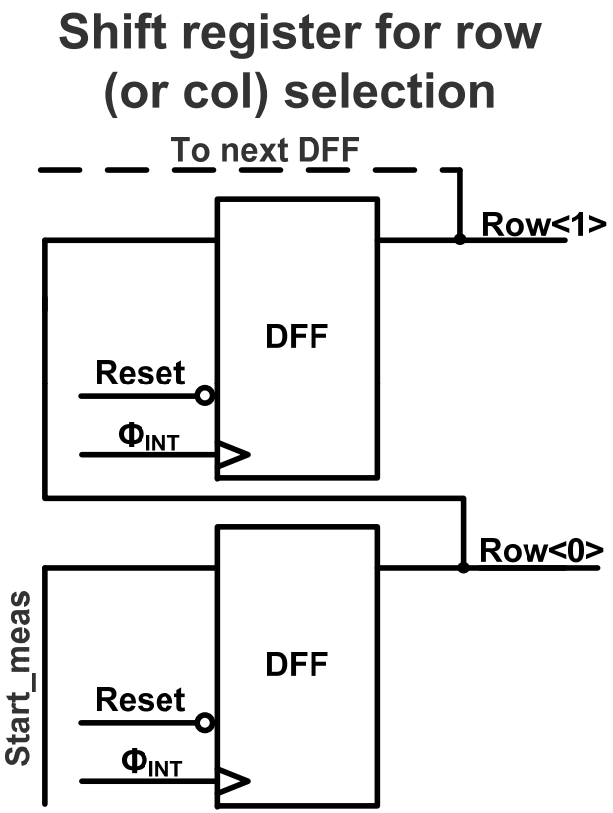
Device Probing vs. Array Based Circuits



- Device probing: simplicity and legacy
- Advantages of an array based circuit approach
  - Parallel stress, short test time, small test area, high resolution, representativeness and accuracy

Proposed TDDB Test Macro

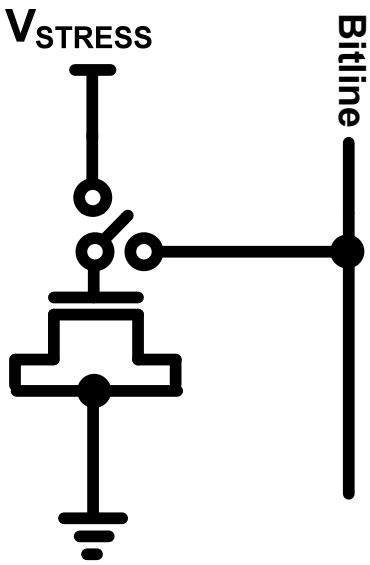




- Two new stress cells: flexible stress cell, IO stress cell
- Current to binary converter for fast evaluation
- Embedded calibration cells

Stress Cell Abstractions

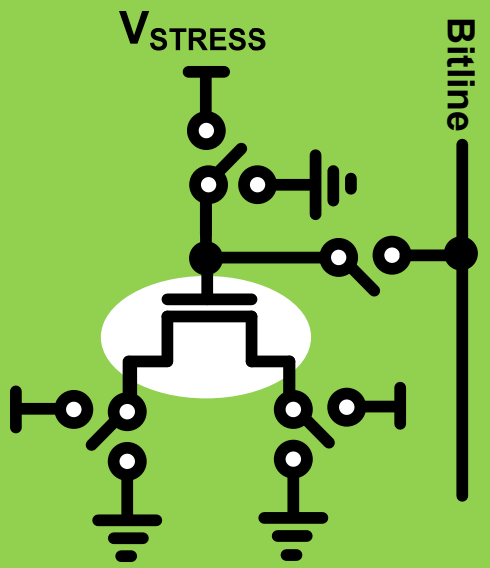
On-state, Core FET



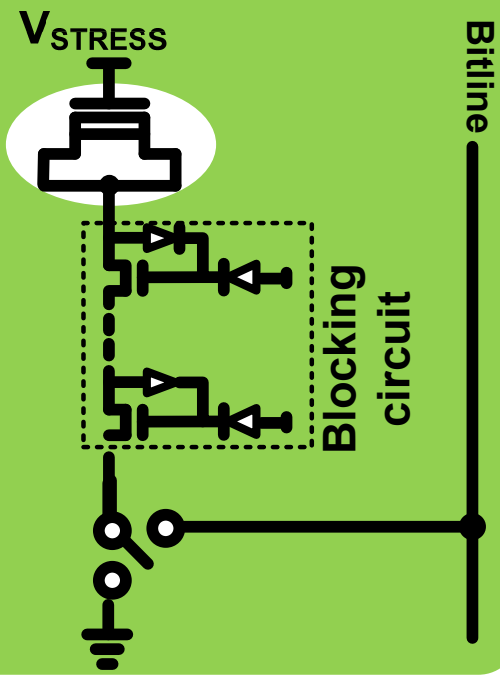
J. Keane, CICC08

Proposed stress cells

Off-state, Core FET

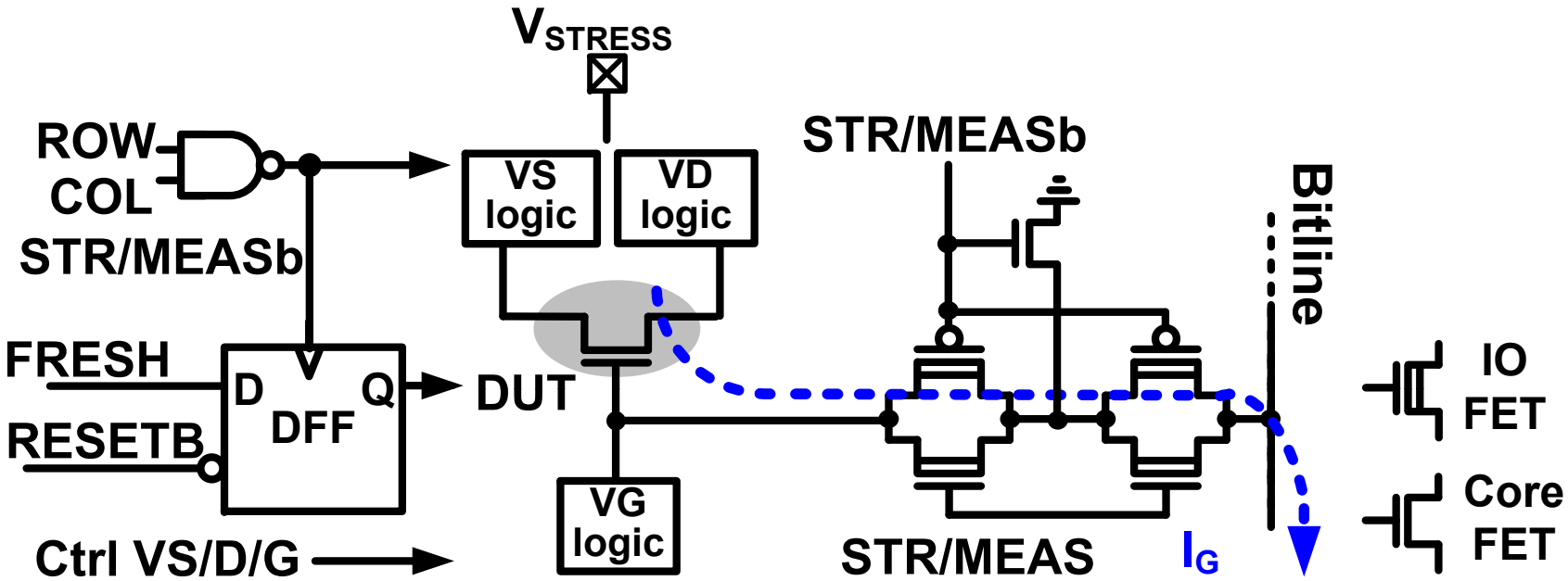


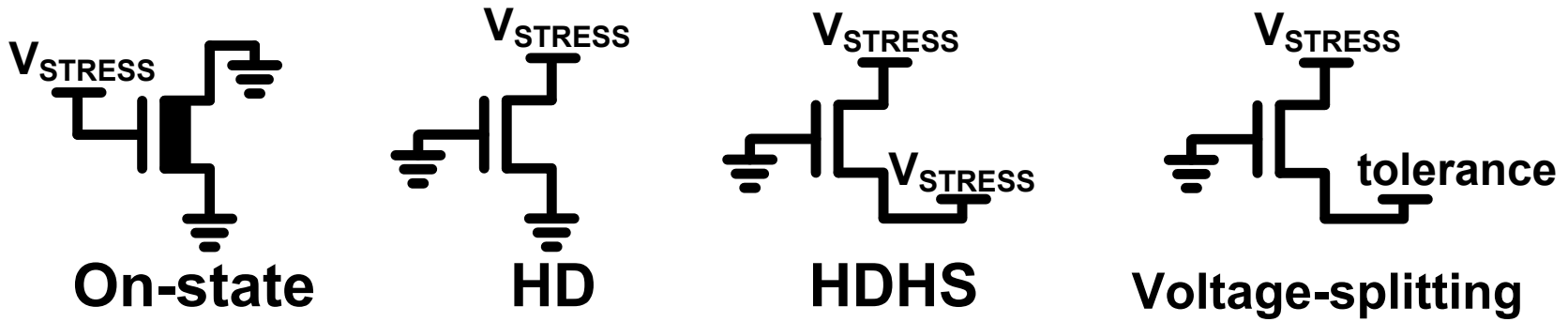
On-state, IO FET



- Prior art only tackled <u>core</u> device on-state TDDB statistics
- Challenge for IO cell: How to provide high V_{STRESS} (~9V) to the DUT in isolation when we are employing thickest available t_{ox}

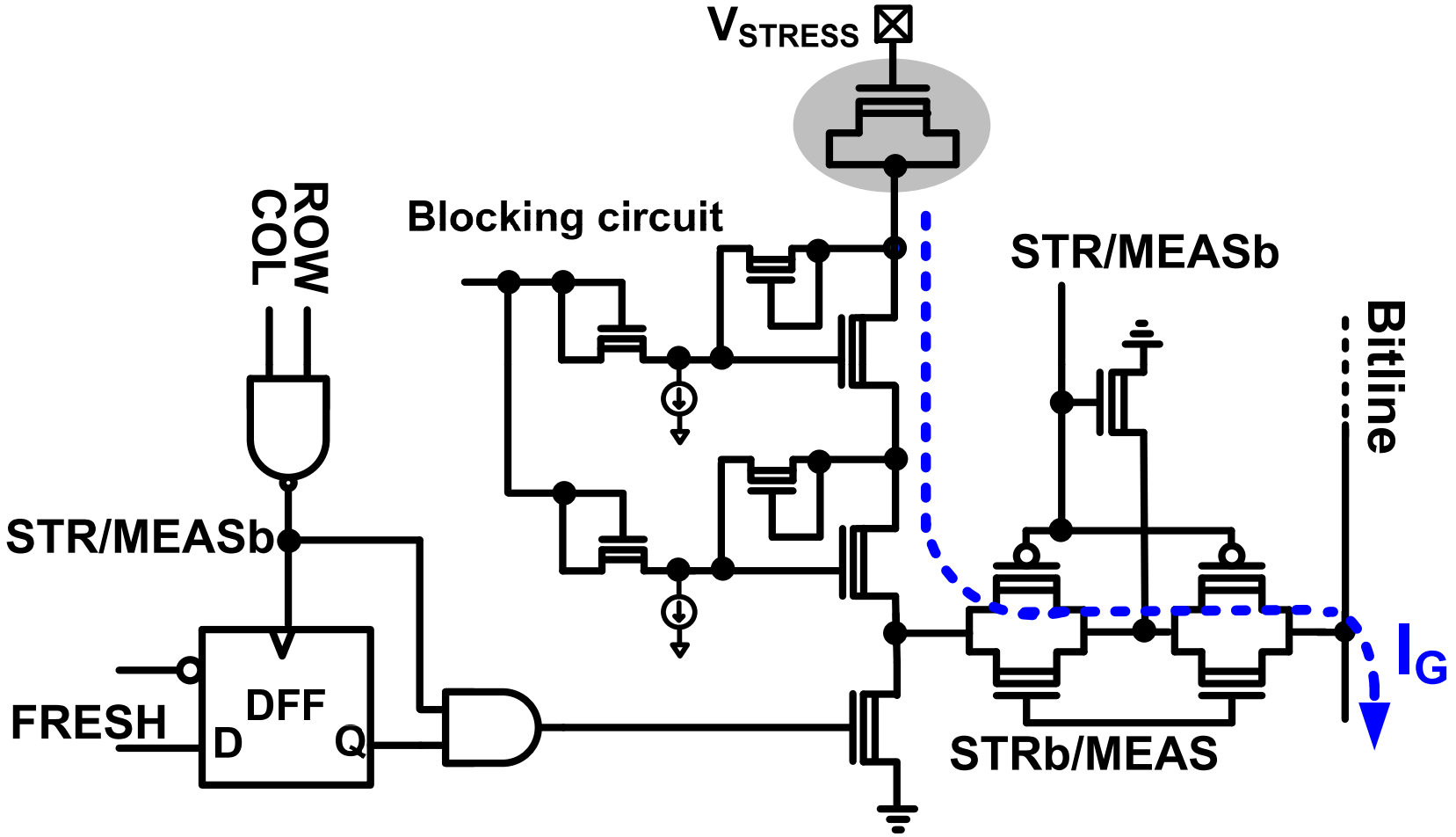
Flexible Stress Cell Design





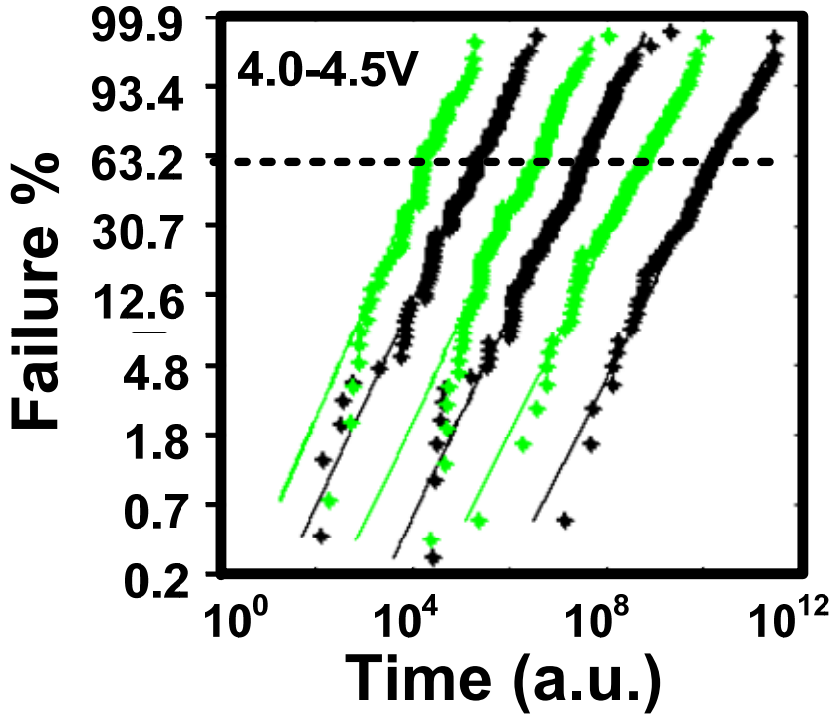
- Control on VS/D/G voltages for flexible modes

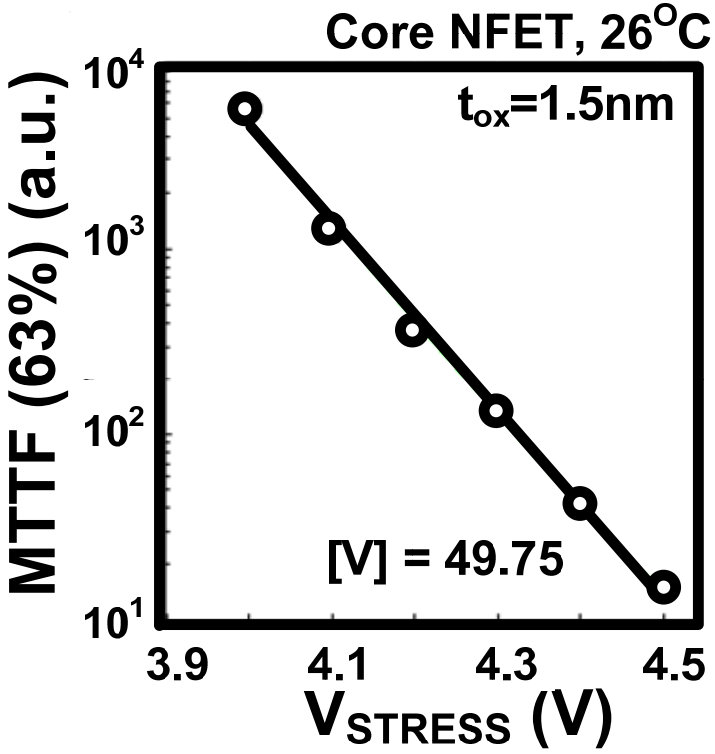
IO Stress Cell Design



- Pre-breakdown: Full V_{STRESS} appears across DUT
- Post-breakdown: $2V_{GS}+2V_T$ drop blocks V_{STRESS}

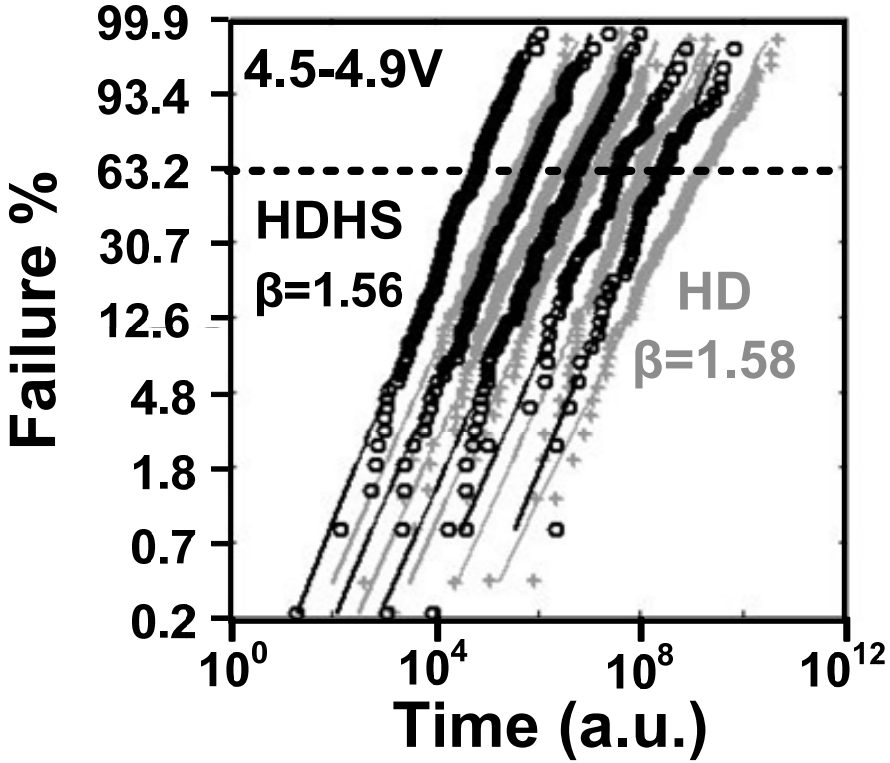
Measured Data: On-state, Core FET

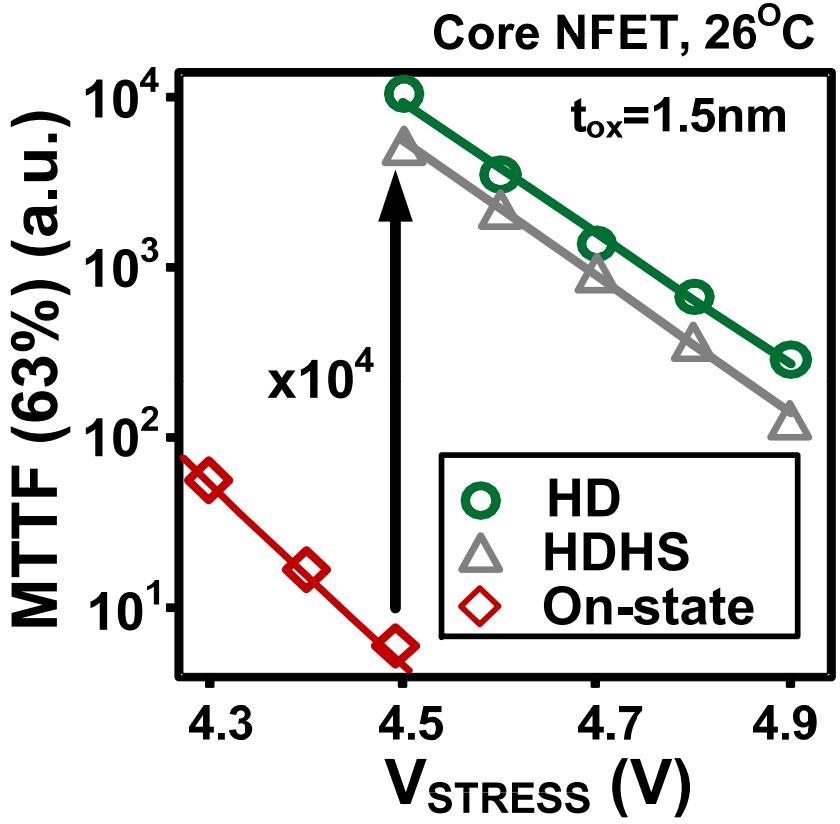




- Compared to previous on-state characterization in the same process (J. Keane , CICC'08)
  - Similar β value (=1.44)
  - Almost same [V] (=49.75) close to prev. work (=51.0)

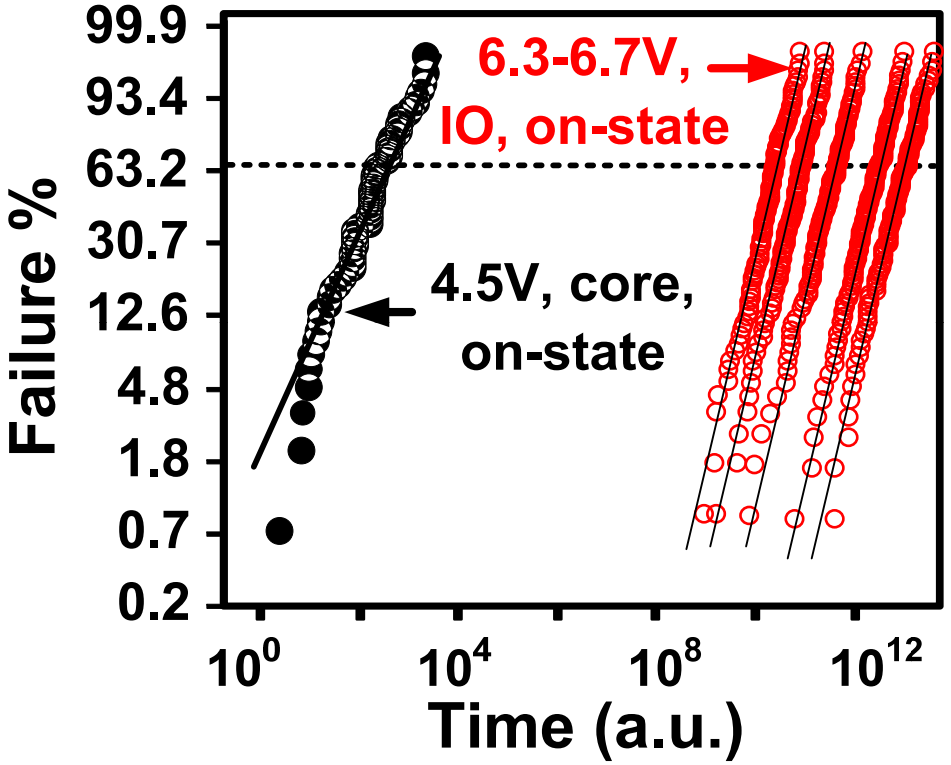
Measured Data: Off-state, Core FET

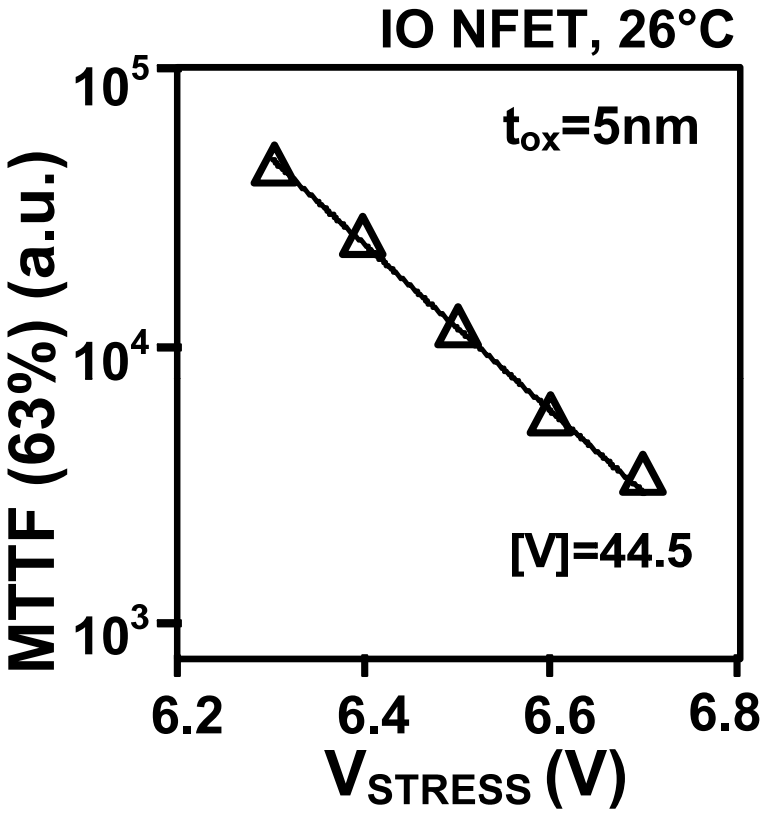




- Compared to core on-state, off-state yields
  - Smaller spread or relatively large β (=1.56)
  - Smaller [V] (=43.5) compared to core case

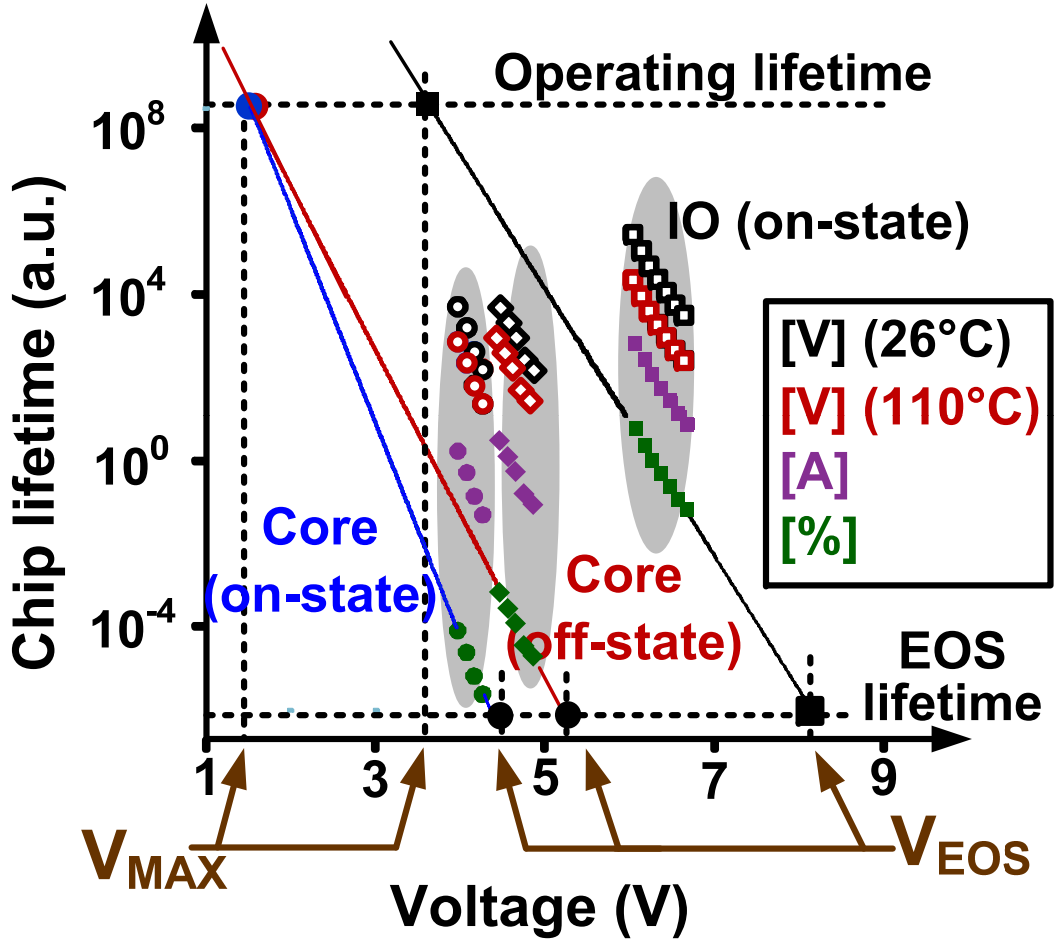
Measured Data: On-state, IO FET





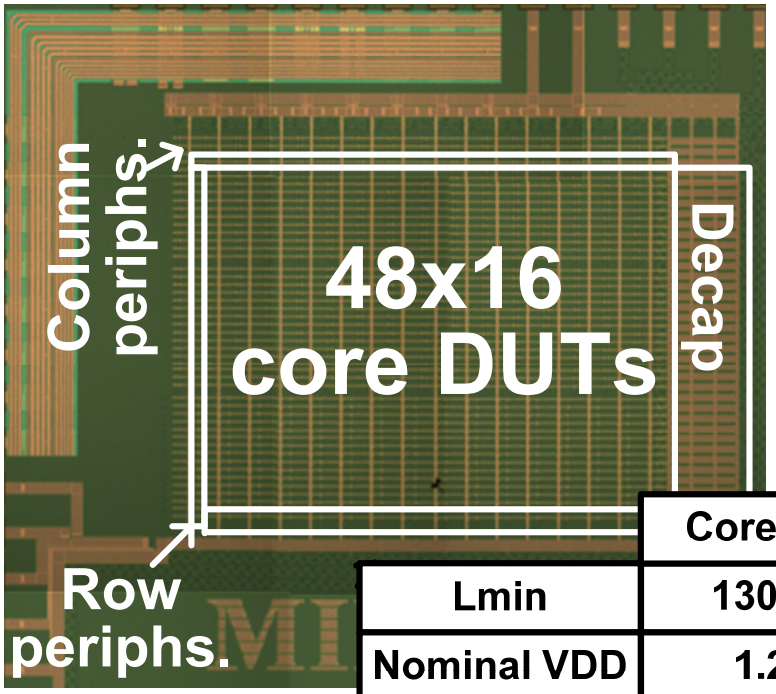
- Compared to core devices, IO devices have:
  - Smaller spread or large β (=2.71)
  - Smaller [V] (=44.5) compared to core case

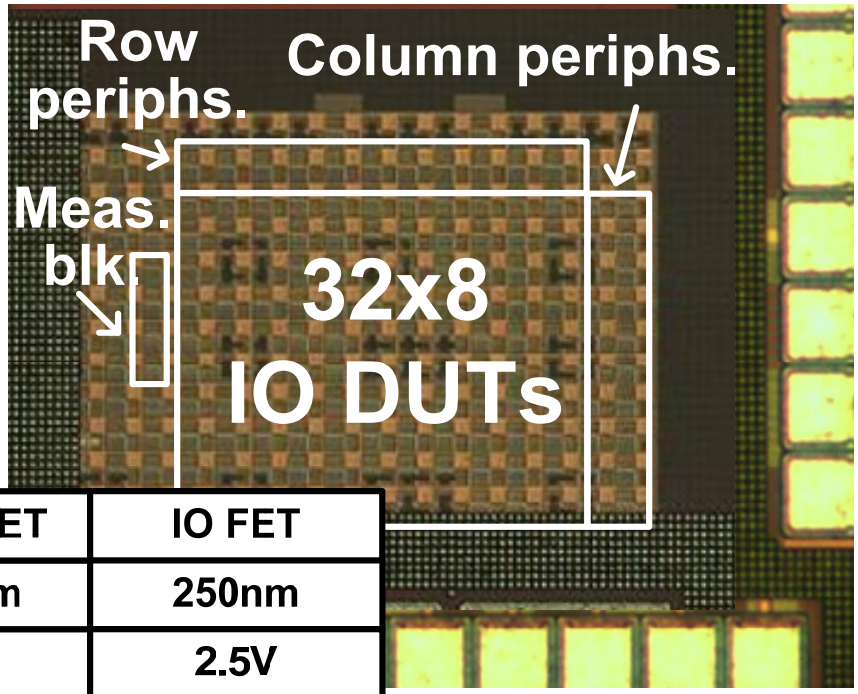
Putting It All Together



- Proposed macro can <u>efficiently</u> collect large fail statistics under various stress modes

Test Chip Micro-photographs





	Core FET	IO FET
Lmin	130nm	250nm
Nominal VDD	1.2V	2.5V
Array dim.	1.33x0.9mm^2	0.34x0.24mm^2
DUT dim.	2µm x 2µm	2µm x 2µm

- Two arrays for core and IO DUTs separately implemented

Conclusion

- Proposed TDDB macro reduces stress time and silicon area in proportion to number of DUTs
- Two stress cells were proposed:
  - A flexible DUT for both off and on-state stress
  - IO DUT for stressing up to $4xV_{DD}$ without thicker t_{ox} devices
- Two stress arrays were fabricated
  - L_{MIN} of 130nm for core devices and 250nm for IO devices
  - In tandem lifetime projections were made for comprehensive TDDB evaluation

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