A Programmable Adaptive Phase-Shifting PLL for Enhancing Clock Data Compensation under Resonant Supply Noise

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Agenda

- Resonant supply noise and clock data compensation effect
- Clock modulation and adaptive clocking technique
- Proposed phase-shifting PLL
- 65nm test chip results
- Conclusions
Resonant Supply Noise

- IR and Ldi/dt noise: 10-15% of nominal $V_{dd}$
- Resonance between package/bonding inductance and die capacitance
- Typical resonant frequency: 40-300MHz
- Large magnitude, affects the entire chip
Clock Data Compensation

• Both clock and data are affected by resonant supply noise
• Modulated clock can partially compensate for the datapath delay increase
Existing Clock Modulation Schemes

- Clock distribution with RC-filtered supply
- Clock buffers with built-in RC filters
- Noise sensitive PLL generating adaptive clock

[1] Intel Pentium 4, N. Kurd, et al., JSSC’01
[3] Intel Nehalem, N. Kurd, et al., JSSC’09
Adaptive Clocking Technique

- Point A coincides with E for best compensation
- Adjust both phase shift & supply noise sensitivity for optimal compensation
Proposed Phase-Shifting PLL

\[ C_{eq} = (C_u + C_d) || C_f \]
\[ S_v = \frac{C_u}{C_d} \]

Supply Tracking Modulator

AVDD: PLL VDD
DVDD: Digital VDD
Noise Sensitivity & Phase Shift Control

65nm, 1.2V, room temp., simulation results

- $S_v (= \frac{C_u}{C_d})$ controls supply noise sensitivity
- $C_{eq} (= \frac{C_f}{C_d+C_u})$ controls phase shift and noise sensitivity
- Both $S_v$ and $C_{eq}$ are digitally programmable
Test Chip Organization

<table>
<thead>
<tr>
<th>Clock tree</th>
<th>Buffer style</th>
<th>Interconnect</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>Inverter</td>
<td>None</td>
</tr>
<tr>
<td>#2</td>
<td>Inverter</td>
<td>Short</td>
</tr>
<tr>
<td>#3</td>
<td>Inverter</td>
<td>Medium</td>
</tr>
<tr>
<td>#4</td>
<td>Inverter</td>
<td>Long</td>
</tr>
<tr>
<td>#5</td>
<td>Differential</td>
<td>Short</td>
</tr>
<tr>
<td>#6</td>
<td>Differential</td>
<td>Long</td>
</tr>
<tr>
<td>#7</td>
<td>Differential</td>
<td>Short</td>
</tr>
<tr>
<td>#8</td>
<td>RC buffer [5]</td>
<td>Long</td>
</tr>
</tbody>
</table>

Local supply noise monitor

Supply noise generation blocks

VCO & clock pattern control

Switches for colored noise

LFSRs for random noise

% of timing errors = \( \frac{T_{CLK}}{T_{BER}} \times 2^{n+1} \)
The table below summarizes the performance of the PLLs:

<table>
<thead>
<tr>
<th>Modulation</th>
<th>Sensitivity</th>
<th>Phase shift</th>
<th>Programmable</th>
<th>1st droop</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conv.</td>
<td>None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[1][2]</td>
<td>Clock path</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>[3] PLL</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

- **Technology**: 65nm LP CMOS
- **Total area**: 350 x 250 µm²
- **Regulation frequency**: 40MHz-300MHz
- **VDD**: 1.2V
- **PLL area**: 120 x 100 µm²
- **F_{max} improvement**: 3.4%-7.3%
• BER increases quickly at higher $f_{\text{clk}}$
• Define $F_{\text{max}}$ as clock frequency when BER=$10^{-6}$
$F_{\text{max}}$ vs. Noise Sensitivity & Phase Shift

- Chip tested at different $V_{\text{dd}}$ and $f_{\text{noise}}$
- Optimal configuration varies significantly on operating condition
F\textsubscript{\text{max}} vs. Noise Frequency

- Tested under different Vdd & noise waveform
- 3-7% improvement on F\textsubscript{\text{max}} for typical resonant band (40-300MHz) at 1.2V and 1.0V
F_{max} \text{ vs. Different Clock Trees}

Tested under different V_{dd}, f_{noise} and noise patt.

3-7% improvement on F_{max} with various clock distribution designs under 1.2V and 1.0V
Conclusions

• Resonant noise is an important concern in power supply network designs

• Inherent timing compensation between clock and data improves $F_{\text{max}}$

• A 65nm phase-shifting PLL demonstrated
  – Enhances clock data compensation effect
  – Programmable supply noise sensitivity and phase shift for optimal compensation
  – 3-7% $F_{\text{max}}$ improvement for typical resonant noise frequencies (40-300MHz)