A 1V Printed Organic DRAM Cell Based on Ion-Gel Gated Transistors with a Sub-10nW-per-Cell Refresh Power

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Agenda

• Motivation
• Previous Organic Memory Research
• Electrolyte Gated Organic TFT with an Unusually High Gate Capacitance
• Proposed 3T DRAM Array Design
• 1V 8x8 Printed DRAM Measurements
• Conclusions
Organic Electronics

- Flexible, large area low temperature processing, low cost, printable
- Emerging applications: Active display matrix, e-paper, RFID, solar cell, etc
- Memory: Key component in flexible applications
Previous Organic Memory Research

- **Non-volatile memory**
  - Floating-gate structure
  - Ferroelectric materials
  - Fuse-based

- **Volatile memory**
  - Write-only SRAM (JSSC07)
    - Braille sheet display
    - Static power problem
  - No previous work on general purpose DRAM

*T. Sekitani, Science 2009*

*M. Takamiya, JSSC 2007*
Electrolyte Gated OTFT with an Unusually High Gate Capacitance

- Polarized ions enable $C_{gate} = 10 \sim 100 \mu F/cm^2$
  - High gate capacitance ideal for DRAM cells
  - 65nm LP CMOS: $C_{gate} \sim 1.4 \mu F/cm^2$

Aerosol Jet Printing Method

- Ultrasonic atomizer: aerosol generation
- Output nozzle produces small droplets (1-5 µm)
  - Sub-5 µm line width printing capability
P-type Only 3T DRAM Gain Cell

- Ideal memory cell for electrolyte gated OTFTs
  - Long retention time (> 1 minute), compared to 65nm CMOS (~100µs [4])
  - P-type only implementation possible, no static power

DRAM Cell Measurement

- Verified full read and write functionality
  - Required WL pulse width: 20 ms (write), 12 ms (read)
  - Operating voltage range: 0.8V – 1.2V
8x8 Printed Organic DRAM Array

- Custom IC design flow adopted for OTFTs

<table>
<thead>
<tr>
<th>Process</th>
<th>Ion-gel organic TFT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel</td>
<td>Poly(3-Hexylthiophene)</td>
</tr>
<tr>
<td>TR dim.</td>
<td>W/L = 500µm / 25µm</td>
</tr>
<tr>
<td>Array dim</td>
<td>24 x 25 mm²</td>
</tr>
<tr>
<td>Array size</td>
<td>64 bits (8 WLs, 8 BLs)</td>
</tr>
<tr>
<td>Read delay</td>
<td>&lt; 12 msec</td>
</tr>
<tr>
<td>Write delay</td>
<td>&lt; 20 msec</td>
</tr>
<tr>
<td>Supply</td>
<td>0.8V - 1.2V</td>
</tr>
<tr>
<td>T_RETENTION</td>
<td>&gt; 60sec @ 1.30V WWL</td>
</tr>
<tr>
<td>P_ACTIVE</td>
<td>8 µW/bit</td>
</tr>
<tr>
<td>P_STANDBY</td>
<td>5.5 nW/bit</td>
</tr>
</tbody>
</table>

Photograph of Printed Organic DRAM Array

24 mm
Array Retention Time Measurements

- Worst case retention time: 30 sec for WWL=1.25V
- Retention time over 1 minute for WWL=1.30V
Power Consumption Comparison

- 12X+ power savings in active mode
- < 10nW/bit refresh power in retention mode

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Proposed General Purpose DRAM Array for Display/Sensor Applications

- Low voltage, low power
- Random access
- Compatible with existing OTFT logic circuits [3]

Conclusions

• An 8x8 printed organic DRAM array demonstrated for the first time
  – Retention time > 1min, refresh power < 10nW/b
  – 12X power reduction over SRAM in active mode
  – Cell operation: 50Hz
  – VDD down to 0.8V

• Future work
  – Periphery circuit design
  – Integration with displays or sensors