

18.3 A 1V Printed Organic DRAM Cell Based on Ion-Gel Gated Transistors with a Sub-10nW-per-Cell Refresh Power

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Organic thin-film-transistors (OTFTs) are drawing much attention as they have attributes such as structural flexibility, low-temperature processing, large area coverage, and low cost, which make them attractive for large-area electronics. Various forms of OTFTs can enable applications that were not achievable using traditional inorganic transistors and/or surpass them in terms of performance and cost. OTFTs cannot match the performance of silicon-based transistors, but can complement them by enabling electronic flexible systems, which don't have to operate at high-speed. Recently, inkjet printing has become a popular method for low-cost manufacturing of OTFTs making product level implementations feasible. Despite these encouraging developments, the relatively high voltage needed to power up traditional OTFT devices and the lack of a good n-type device presents major circuit design challenges for OTFT-based systems.

Memory is a key component in many OTFT applications but only few attempts have been made on designing memory circuits suitable for OTFTs [1]. SRAM, which is the mainstream embedded memory in silicon chips, suffers from large power consumption in today's OTFT technologies, which only allow p-type devices to be fabricated. Although research on n-type OTFTs is currently underway [2], introduction of a viable n-type material has been delayed as existing materials have unstable characteristics, no good contact, and significantly lower mobility than their p-type counterpart. Since only p-type organic transistors are currently available for most designs, resistors or diode-connected transistors are required to achieve SRAM functionality, introducing large static power consumption. Moreover, unless the read operation can be sacrificed, the load resistor must be strong enough to avoid a destructive read, which prevents any further power-saving opportunities in SRAM. In this paper, we report a DRAM array in a printable, flexible and low-voltage ion-gel gated OTFT technology [3], which has no DC static power and achieves considerable performance improvement at operating voltages below 1V, overcoming the fundamental limitations of OTFT-based SRAMs.

DRAM cells can be implemented using three transistors, or even two transistors, in a standard logic process without a dedicated storage capacitor process [4]. Despite using a single type of device for the cell, this circuit (commonly referred to as "gain-cells") has no DC static current, making it an ideal memory candidate for OTFT technologies where only p-type devices are available. The main challenge for gain-cells is the short retention time, typically less than 100 μ s in silicon due to the small gate capacitance used for data storage [4]. Ion-gel gated OTFTs used in this work serve as an ideal device platform for DRAMs as their gate capacitances can exceed 100 μ F/cm², roughly 70 \times higher compared to that in 65nm CMOS [3]. This unusually high capacitance is derived from the ultra-thin electrical double layers formed upon electrical polarization as shown in Fig. 18.3.1 and can be used to enhance DRAM retention time and simultaneously achieve a much higher drive current at low supply voltages compared to other OTFT devices.

An 8 \times 8 DRAM array was fabricated using an aerosol jet printer to demonstrate the feasibility of gain-cell DRAMs in a p-type-only OTFT technology. This printing method can accommodate functional inks with a variety of viscosities and has a patterning precision of 10 μ m. Our underlying design philosophy was to implement a general-purpose memory array with full read and write capability that can be utilized for a range of applications including electrochromic displays and/or sensor sheet arrays as shown in Fig. 18.3.2 (left). The basic read and write operations of the 3T OTFT memory cell are illustrated in Fig. 18.3.2 (right). Each transistor has a channel width of 500 μ m and a channel length of 25 μ m.

The leakage components during hold mode are illustrated in Fig. 18.3.2: namely the gate currents of the storage and write devices and the subthreshold leakage of the write device. A boosted WWL is preferred to suppress the subthreshold leakage as is the case in all practical DRAM designs. This boosted voltage can be efficiently generated using a single-stage charge pump consisting of a p-type gate capacitor and a diode-connected transistor. Note that the retention time of data '0' is more critical than data '1' for p-type cells as the storage node is surrounded by high voltages resulting in all leakage currents in the pull up direction. Moreover, the read current for driving the RBL is determined by the data '0' voltage, as it determines the gate overdrive of the p-type read device. Measurements were automated with LabVIEW™ software to collect reliable retention-time statistics. When read is enabled, a cell storing data '0' will have a large pull-up current and drive the RBL high. A pull-down resistor attached to the RBL resets the RBL signal after the read is completed. Measured waveforms in Fig. 18.3.3 verify full read and write functionality at 1V. WWL is kept high after the write access to test for the worst-case data '0' retention condition. The steady-state RBL voltage level is used to calculate the voltage stored in the cell at the time of access. We define retention time as the time it takes for the data '0' voltage inside the cell to increase to 0.5 \times V_{DD}, and the resistor load is therefore selected so that a 0.5 \times V_{DD} voltage in the storage node translates into a RBL level of (V_{DD}-0.1V).

The retention-time statistics of the DRAM array at 1V are shown in Fig. 18.3.4. With a boosted WWL of 1.25V, the worst-case cell has a retention time of 30s while 72% of the cells have retention times longer than 1 minute. With a slightly higher boosted WWL of 1.30V, every cell in the array can have a retention time exceeding 1 minute. This translates into a retention time that is 5 orders of magnitude longer than recent gain-cell designs in 65nm CMOS [4], which is sufficiently long even for the slow OTFT circuits to perform a periodic refresh operation. Figure 18.3.5 (left) shows the impact of WWL pulse width on retention time indicating that a 20ms write pulse is needed to achieve a retention time greater than 1 minute. This can be further improved if a negative WWL voltage is available. The read delay, defined as the 50% rise time of the RBL signal when reading from a data '0' cell, was 12ms or less. The memory cells show robust read and write operation down to 0.8V.

Our printed DRAM array also demonstrates significant reduction in power consumption during active and standby modes. Due to the extremely long retention time, the refresh power of the proposed memory cell is in the nano-watt order. Figure 18.3.6 compares the measured power consumption of an SRAM and a gain-cell DRAM implemented using the same kind of ion-gel OTFT devices. Individual SRAM cell structures were fabricated and tested for this comparison. Results show that the overall power consumption of an OTFT DRAM (including active, static, and refresh power) is 12 \times lower than the static power consumption of an OTFT SRAM for a 50Hz operating frequency. In standby mode where all RBLs are left floating except for when the cells are refreshed, the DRAM power consumption per cell is reduced to below 10nW. Figure 18.3.7 shows the chip microphotograph and performance summary of the organic DRAM array chip.

Acknowledgements:

This work was funded by the National Science Foundation.

References:

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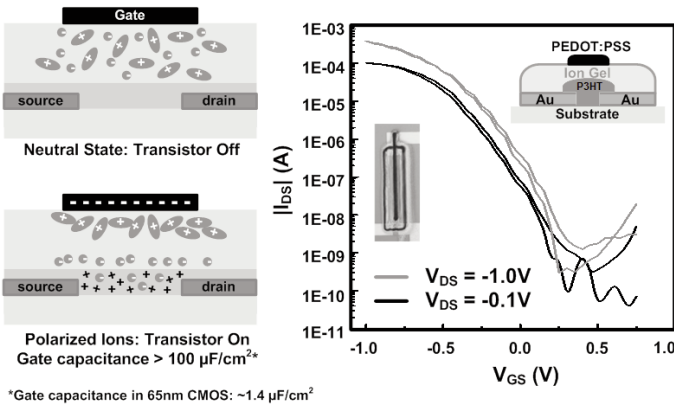


Figure 18.3.1: Basic operation of an ion-gel gated OTFT. I_{DS} - V_{GS} curve shows a 0.4mA drive current at a 1 V voltage ($W=500\mu\text{m}$, $L=25\mu\text{m}$).

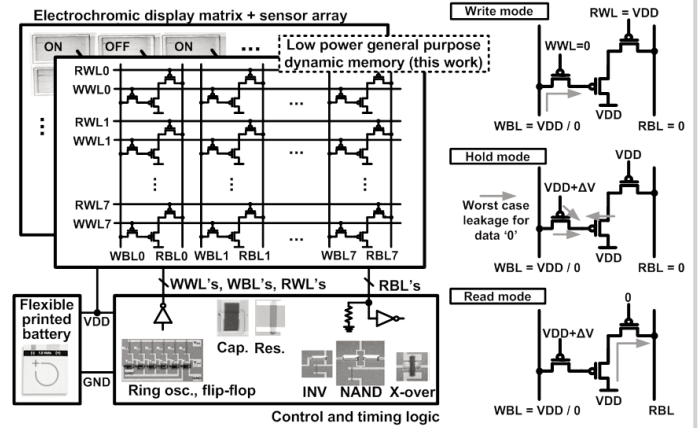


Figure 18.3.2: Conceptual diagram of a flexible display and sensor array system and detailed illustration of cell schematic and operations.

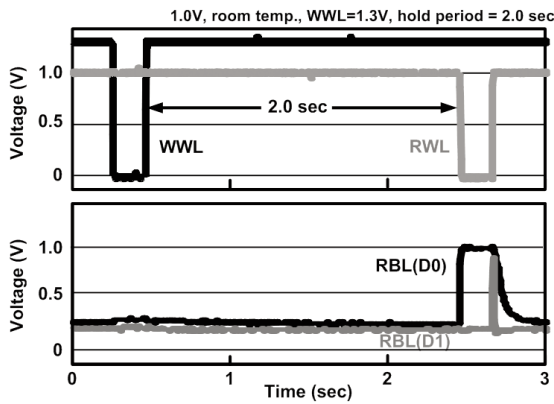


Figure 18.3.3: Measured waveforms of the 8x8 DRAM test chip for a 2.0s hold period.

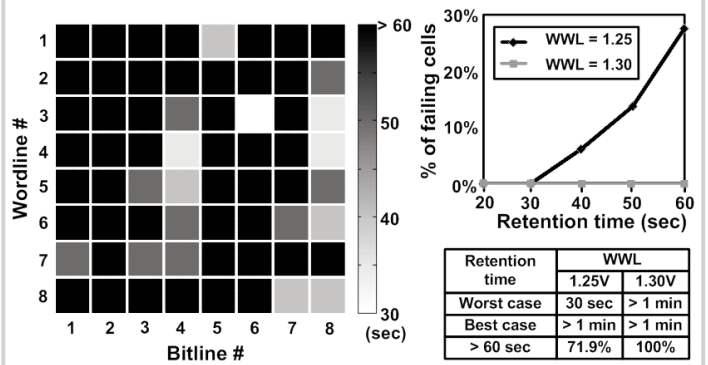


Figure 18.3.4: Measured retention time map for WWL=1.25V (left). Percentage of failures vs. retention time at different WWL voltages (right).

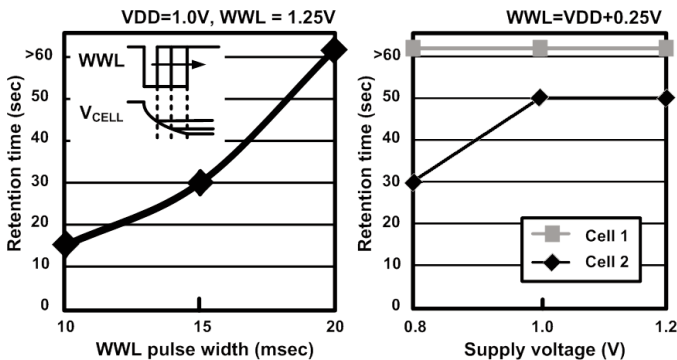


Figure 18.3.5: Retention time vs. WWL pulse width and retention time vs. supply voltage.

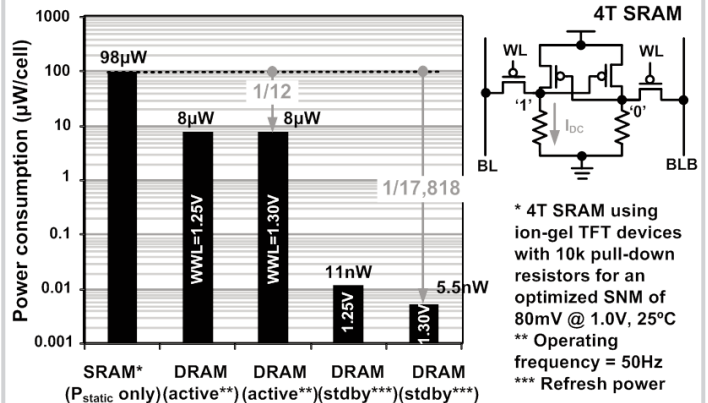
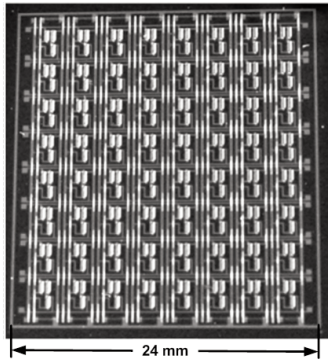


Figure 18.3.6: Measured power consumption of an OTFT SRAM (static power only) and DRAM for different WWL voltages and operation modes.



Process	Ion-gel organic TFT
Channel material	Poly(3-Hexylthiophene)
Array dimension	24 x 25 mm ²
Array size	64 bits (8 WLs, 8 BLs)
Read delay	< 12 msec
Write delay	< 20 msec
Supply	0.8V - 1.2V
*Retention time	30sec @ 1.25V WWL > 60sec @ 1.30V WWL
**Active power	8 μW/cell @ 1.25V WWL 8 μW/cell @ 1.30V WWL
**Standby power	11 nW/cell @ 1.25V WWL <5.5 nW/cell @ 1.30V WWL

* Measured @ 1.0V, 25 °C
 ** Measured @ 1.0V, 25 °C, refresh period of 30 sec (WWL=1.25V) and 60 sec (WWL=1.30V)

Figure 18.3.7: Chip photograph of the 8x8 printed organic DRAM and performance summary.