28.10 A 700MHz 2T1C Embedded DRAM Macro in a Generic Logic Process with No Boosted Supplies

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6T SRAMs have been the embedded memory of choice for modern microprocessors due to their logic compatibility, high speed, and refresh-free operation. The relatively large cell size and conflicting requirements for read and write at low operating voltages make aggressive scaling of 6T SRAMs challenging in sub-22nm. Recently, 1T1C embedded DRAMs (eDRAMs) have replaced SRAMs in several server applications reducing the cache area and improving performance [1]. Difficulties in scaling the trench capacitor and the additional process steps involved in manufacturing the thick oxide access devices are currently limiting the wide spread adoption of 1T1C technology. Gain cells have features such as decoupled read and write paths, a nondestructive read, and a 2X higher bit-cell density than a 6T SRAM, making them a strong contender for future embedded memories [2-4]. However, the boosted supplies needed for robust operation necessitates thick oxide devices to prevent gate reliability issues in gain cells. Although this would lead to a larger bit-cell size and decreased macro performance, these limitations have been overlooked in the past. In this paper, we present the following circuit techniques for realizing a truly logic compatible (i.e. thin oxide only implementation) gain cell eDRAM with no boosted supplies; (i) a 2T1C gain cell featuring a beneficial couple-up read and a preferential couple-down write, (ii) a single-ended 7T SRAM to repair weak gain cells, and (iii) a storage voltage monitor capable of tracking PVT and cell retention time for adaptive refresh control. The 64kb test macro in Fig. 28.10.1 achieves a random cycle frequency of 700MHz and a retention time of 500µsec.

DRAMs typically require two boosted supplies: a boosted high voltage to suppress the subthreshold leakage (consider a PMOS write device) and a boosted low voltage to prevent V_{TH} drop during write. The proposed 2T1C gain cell shown in Fig. 28.10.2 can operate reliably with no boosted supplies allowing the gain cell to be implemented using regular thin oxide devices. The new cell structure consists of an asymmetric 2T cell [4] and a coupling MOS capacitor controlled by the PCOU signal. PCOU is pre-discharged to 0V during hold mode introducing only a small amount of gate-overlap leakage through the coupling device (PC). At the beginning of the read access when the Read Word-Line (RWL) is activated, PCOU is also switched to VDD. This couples up both data '1' and '0' storage voltages. The higher voltage levels increase the drive current for the NMOS read access device (PS) enhancing the read performance. After the Sense Amplifier (S/A) samples the Read Bit-Line (RBL) data, a write-back operation follows which drives the Write Word-Line (WWL) to 0V instead of the usual negative boosted supply. Using a data '1' Write Bit-Line (WBL) voltage that is slightly lower than VDD (i.e. VDD-α in Fig. 28.10.2), the sub-threshold leakage in the unselected cell can be effectively cut off without using a boosted high supply for WWL [3]. Data '1' can be easily written back to the cell with a PMOS write device (PW). However, without a boosted low supply, data '0' will not be fully restored due to the V_{TH} drop in PW. To resolve this issue, PCOU is switched to 0V immediately after write back. This couples down the data '0' voltage but not the data '1' voltage since PW remains on when WBL is high. Finally, WWL is switched back to its precharge level of VDD and this couples up both data '1' and '0' voltages using the gate-overlap capacitance, fully restoring the cell storage levels.

Outlier cells with poor retention times can be replaced using 7T SRAM cells with decoupled read and write paths implemented as part of the array (Fig. 28.10.3). The single-ended read and differential write of the 7T SRAM share the same control signals with the main 2T1C array minimizing the circuit overhead. Gain cells have a very small storage capacitance and therefore the probability of having a failing cell in a redundant row or column is high compared to 1T1C DRAMs. In fact, measured results in Fig. 28.10.3 show that this probability is 3.13% when a target retention time is longer than 200µsec and repair cells are identical to normal cells. In order to guarantee that all repair cells work with negligible array overhead (1.23% in case of a single-WL repair per 128 WL's), a redundancy scheme utilizing the 7T SRAM repair cells is proposed. The redundancy scheme was implemented for replacing weak word-lines to evaluate the stability of 7T SRAMs under dummy cell and BL-S/A variations. Measured retention bitmap of a 1kb 2T1C sub-array shows weak bit-lines as well as randomly located weak cells. The 128b 7T SRAM shows very stable operation under variation and mismatches. The proposed redundancy scheme can be easily adopted to replace weak bit-lines which improves the retention time from 200µsec to 500µsec.

Retention time of commodity DRAMs varies exponentially with temperature since it is highly sensitive to junction leakage and subthreshold leakage. Therefore, DRAM products have on-chip temperature sensors to adaptively control the refresh period according to the chip operating temperature [5]. Similarly, retention time of gain cells is also highly dependent on operating temperature as shown in Fig. 28.10.4 where there is a 5X difference in the measured retention time between 25°C and 85°C. This means that the refresh power can be reduced at low operating temperatures without sacrificing read performance. However, retention time of an asymmetric 2T gain cell is highly dependent on the gate leakage that has a weaker dependency on temperature [4]. Moreover, the various coupling effects illustrated in Fig. 28.10.2 makes a simple temperature sensor based refresh control ineffective for our gain cell. To overcome this problem, we propose a gain cell based temperature sensor that directly measures the storage node voltage at different temperatures using a cell access pattern generator. The VCO-1 output indicates the current retention time setting and the VCO-2 output provides the average storage node voltage for the 256 cells. To remove any systematic error that may have been introduced while merging the 256 cells, a calibration step is needed to obtain the relationship between the measured storage voltage and the actual retention characteristic. Measured storage voltages including the coupling effects at different temperatures and retention times are shown in Fig. 28.10.4.

A 128kb test macro implemented in a 1.2V, 65nm low-leakage logic CMOS process contains a conventional 3T array and the proposed 2T1C array for performance comparison. Figure 28.10.5 shows the cumulative retention time distribution while varying the boosted low supply of the 3T array. Our design achieves a 1.4nsec (714MHz) random cycle and a 500µsec retention time (after a single-BL repair scheme) without using a boosted supply. Figure 28.10.6 shows the measured VDD shmoo of retention time and random cycle time. Static current consumption of the proposed gain cell including the refresh operation is 147.1µA/Mb at 1.1V while a 6T SRAM consumes 307.5µA/Mb at a power-down data retention voltage of 0.6V. The chip microphotograph and key features of the 65nm eDRAM test chip are shown in Fig. 28.10.7.

Acknowledgements:
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References:

[1] J. Barth, D. Plass, E. Nelson, C. Hwang, et al., "A 45nm SOI Embedded DRAM Macro for POWER7™ 32MB On-Chip L3 Cache," *International Solid-State Circuits Conference*, pp. 342-343, Feb. 2010.

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[3] K. Chun, P. Jain, J. Lee, and C. H. Kim, "A Sub-0.9V Logic-compatible Embedded DRAM with Boosted 3T Gain Cell, Regulated Bit-line Write Scheme and PVT-tracking Read Reference Bias," *Symposium on VLSI Circuits*, pp. 134-135, June 2009.

[4] K. Chun, P. Jain, T. Kim, and C. H. Kim, "A 1.1V, 667MHz Random Cycle, Asymmetric 2T Gain Cell Embedded DRAM with a 99.9 Percentile Retention Time of 110µsec," *Symposium on VLSI Circuits*, pp. 191-192, June 2010.

[5] J. Sim, H. Yoon, K. Chun, H. Lee, et al., "Double Boosting Pump, Hybrid Current Sense Amplifier, and Binary Weighted Temperature Sensor Adjustment Schemes for 1.8V 128Mb Mobile DRAMs", *Symposium on VLSI Circuits*, pp. 294-297, June 2002.

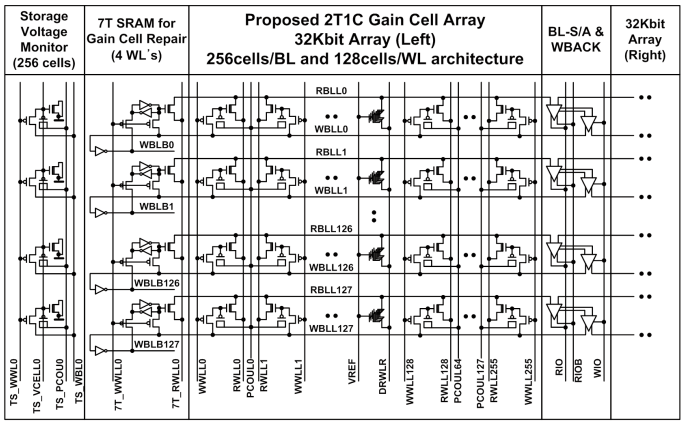


Figure 28.10.1: A 64kb gain cell eDRAM macro with no boosted supplies.

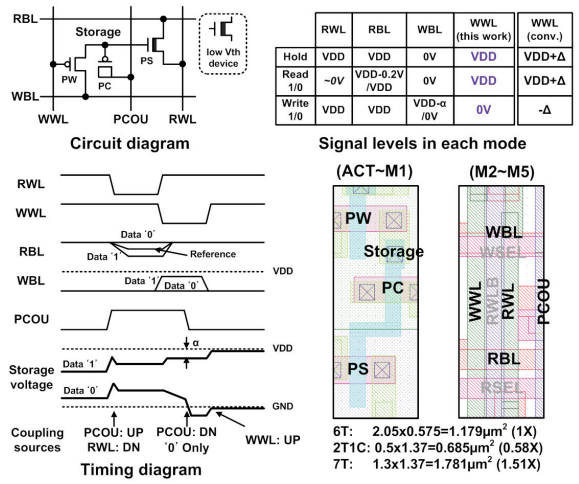
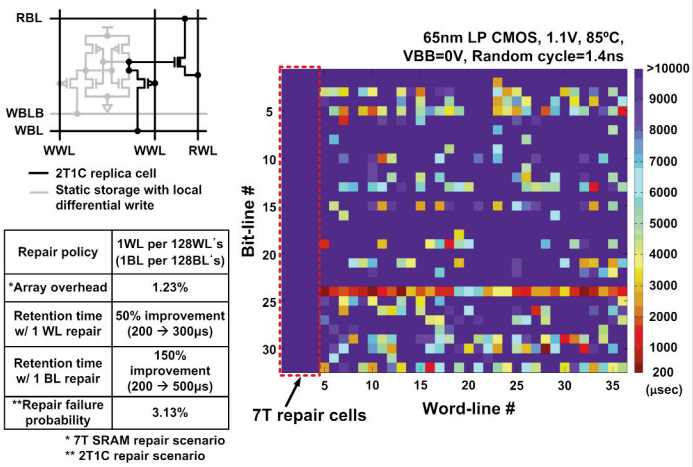


Figure 28.10.2: Proposed 2T1C cell featuring a beneficial couple-up read and a preferential couple-down write.



Repair policy	1WL per 128WL's (1BL per 128BL's)
*Array overhead	1.23%
Retention time w/ 1 WL repair	50% improvement (200 → 300μs)
Retention time w/ 1 BL repair	150% improvement (200 → 500μs)
**Repair failure probability	3.13%

* 7T SRAM repair scenario
** 2T1C repair scenario

Figure 28.10.3: Proposed 7T SRAM repair cell and redundancy scheme (left). Measured retention statistics map (right).

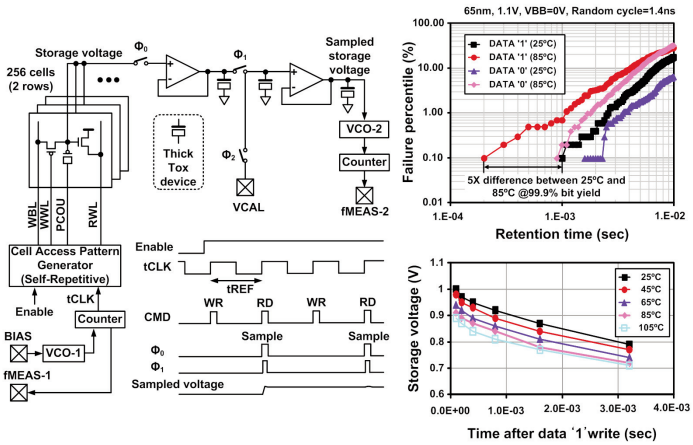


Figure 28.10.4: Proposed storage voltage monitor (left). Measured retention statistics of 2T1C array and storage voltage (right).

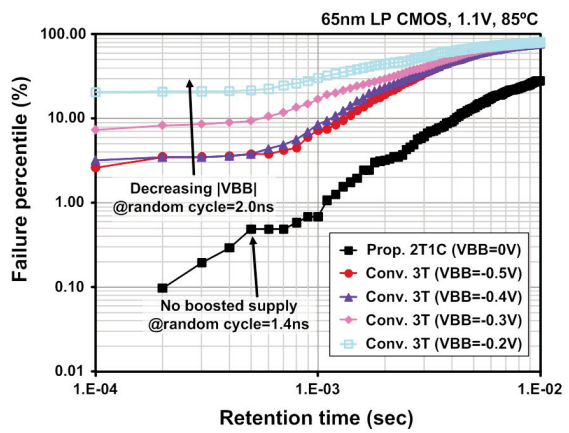


Figure 28.10.5: Retention time distribution of the proposed 2T1C and conventional 3T.

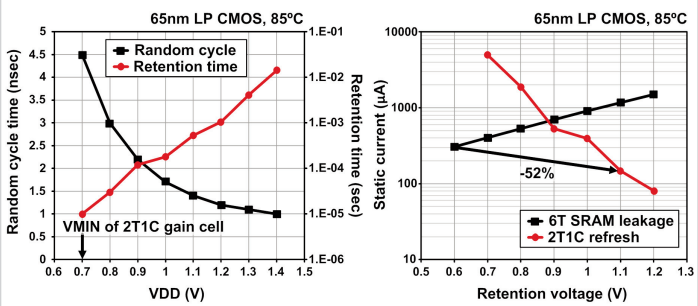
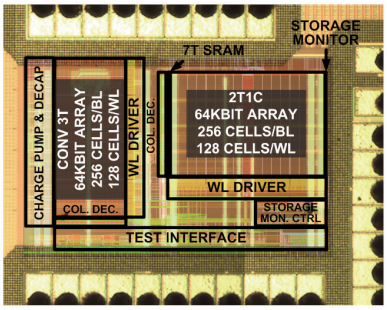


Figure 28.10.6: Measured VDD shmoo and static power comparison between 6T SRAM and 2T1C eDRAM.



Process	65nm LP CMOS
Ckt dimension	555.5x345μm^2
Array size	2x64kbits (Conv. 3T & Prop. 2T1C)
Cell size	58% of 6T SRAM
Retention time	500μs @ 1.1V, 85ºC
Random cycle time	1.40ns (714MHz) @ 1.1V
VMIN	0.7V @ 10μs retention
*Refresh power	161.8μW per Mb (**0.48X of 6T SRAM)

*@ 1.1V, 85ºC, 500μsec refresh rate
**@ Retention voltage of 0.6V

Figure 28.10.7: Test chip microphotograph and chip feature summary.

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