Reliability Monitoring Ring Oscillator Structures for Isolated/Combined NBTI and PBTI Measurement in High-K Metal Gate Technologies

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***Abstract*— Ring oscillator (RO) structures that separate NBTI and PBTI effects are implemented in a high-k metal gate technology. The measurement results clearly show significant RO frequency degradation from PBTI as well as NBTI. For comparison, RO structures with the same principle are also implemented in a SiO_2/poly-gate technology, where PBTI is negligible. Experimental results show noticeable frequency degradation under NBTI-only stress mode but negligible degradation under PBTI-only mode, which illustrates the validity of the proposed principle and structures.**

Keywords- NBTI, PBTI, Ring Oscillator, Circuit

I. INTRODUCTION

Ring oscillator (RO) based monitor circuits have been a mainstay for characterizing Negative Bias Temperature Instability (NBTI) in SiO_2/poly-gate technologies utilizing the fact that Positive Bias Temperature Instability (PBTI) is negligible compared to the dominant NBTI effect in the technologies [1][2]. However, the advent of high-k metal-gates increases PBTI making it significant compared with NBTI [3], which prevents the conventional RO from separating out NBTI and PBTI effects. Fig. 1 shows the RO structure that has been traditionally used for NBTI measurement. During the non-ringing stress period, PMOS and NMOS transistors in alternate stages are stressed. Therefore, the measurement result quantifies the impact of mixed NBTI and PBTI. The PMOS and NMOS devices in an RO structure can be separately

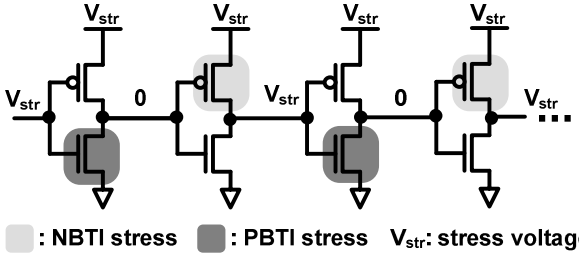

Fig. 1. DC Stress condition for conventional RO used for NBTI measurement in SiO_2/poly-gate technology [1][2].

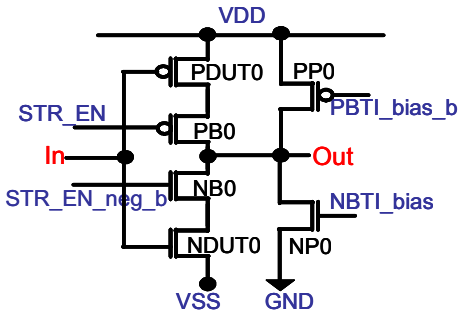

Fig. 2. Proposed ring oscillator (RO4) (1-stage).

stressed if the input of each stage is selectively biased and isolated from the output of the previous stage [4]. In this paper, several RO structures based on this principle are proposed and implemented in a SiO_2/poly-gate technology and a high-k metal gate technology. Experimental results are presented that highlight the ability of these structures to successfully isolate NBTI and PBTI effects while maintaining the simplicity of RO.

II. ISOLATED/ COMBINED NBTI/PBTI MONITOR IMPLEMENTATION IN A HIGH-K/METAL GATE TECHNOLOGY

Fig. 2 shows a single stage of the proposed multi-staged RO structure for separately measuring the impact of NBTI and PBTI on circuit delay. PMOS (PDUT0 for NBTI-only) or NMOS (NDUT0 for PBTI-only) devices can be selectively stressed based on the control inputs (Table 1). In addition, both PMOS and NMOS devices in each stage can be simultaneously

Table 1. Input signal conditions for circuits in Fig. 2 and 4.

Signal	Stress Mode			Meas. Mode
	NBTI	PBTI	N/PBTI	
VDD	Vstr	Vstr	Vstr	Vnom
STR_EN	Vstr	Vstr	Vstr	GND
STR_EN_neg_b	GND	GND	-Vstr	Vnom
PBTI_bias_b	Vstr	GND	Vstr	Vnom
NBTI_bias	Vstr	GND	Vstr	GND
VSS	GND	GND	-Vstr	GND

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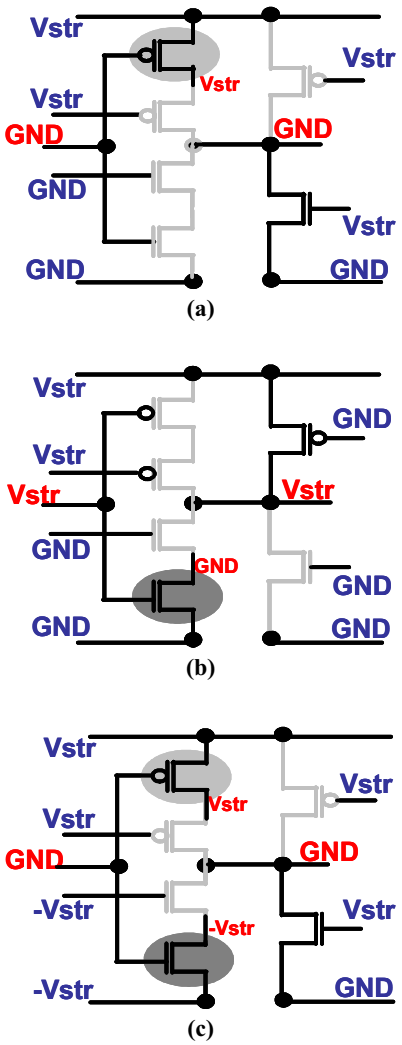

Fig. 3. DC static stress conditions and internal voltages for the proposed RO. (a) NBTI-only stress mode, (b) PBTI-only stress mode. (c) simultaneous N/PBTI stress mode

stressed. During stress, a voltage (Vstr) that is higher than the nominal supply voltage (Vnom) is applied. In static NBTI-only stress mode (Fig. 3a), STR_EN (at Vstr) and STR_EN_neg_b (at GND) turn off PB0 and NB0. The output node (OUT) is forced to GND by NBTI_bias (Vstr) which enables NP0, while PBTI_bias (Vstr) turns off PP0. Thus, the PMOS device-under-test (DUT) in each stage is stressed at DC stress voltage. The stressing of NMOS devices in PBTI-only mode can be explained in complementary fashion (Fig. 3b). In simultaneous N/PBTI stress mode (Fig. 3c), the OUT node is biased to GND (NBTI_bias and PBTI_bias are both at Vstr) while STR_EN_neg_b and VSS receive negative voltage –Vstr. Thus, both NMOS DUTs and PMOS DUTs are simultaneously stressed. In measurement mode, PB0 and NB0 are turned on while NP0 and PP0 are turned off so that the structure becomes equivalent to the conventional RO.

This structure (RO4) was implemented in a high-k/metal gate PD/SOI CMOS technology. In addition, three other simpler structures shown in Fig. 4 with the same design principle [4] were implemented (RO1: NOR structure for NBTI-only, RO2: NAND structure for PBTI-only, and RO3: Unified structure to measure NBTI or PBTI selectively). During the stress mode, the input of every stage in the NOR-style RO1 is biased to Vstr for NBTI stress and the input of every stage in the NAND-style RO2 is biased to GND for PBTI stress.

The die photo is shown in Fig. 5. Each RO frequency is observable through a dedicated frequency divider at an output pad enabling simultaneous measurement of all 4 ROs. The circuits were stressed at various high stress voltages and an elevated temperature for 10,000 seconds followed by an equal relaxation period at VDD=0V. Frequency degradation is monitored at Vnom by interrupting the stress or relaxation for 20ms at periodic intervals. Note that the measurement time is longer than that reported in [2] (2 µs measurement time) due to the use of simple frequency divider for readout. Our intention was to utilize these ROs early on in the technology development stage, and therefore we chose to use simple and

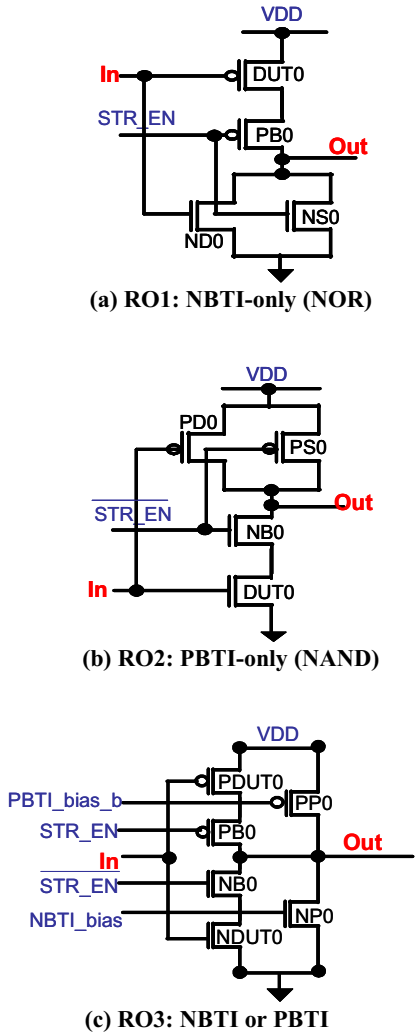

Fig. 4. Simpler RO Structures [4] implemented in the test chip in addition to the RO shown in Fig. 2 (RO4). See Table 1 for input conditions.

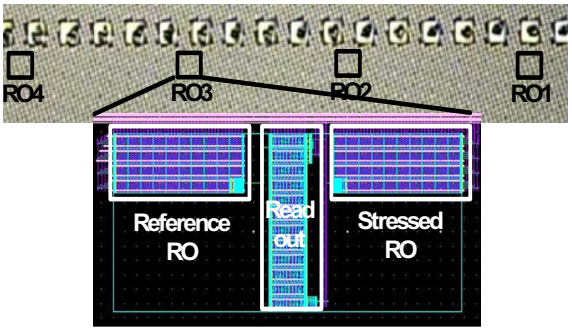

Fig. 5 Die micrograph and layout for BTI monitors for a high-k/metal gate technology. (170x22µm^2 for 4 RO experiments)

robust read circuitry. The proposed RO structures can be connected to the faster readout circuitry [2] seamlessly if necessary. As shown in Fig. 5, a corresponding reference RO is placed next to each RO. The power supply voltage of the reference RO is biased to GND during stress mode and is raised to the nominal operating VDD during measurement mode only. The RO output frequency change due to the environmental variations such as VDD or temperature fluctuations can be separated from the change due to BTI stress by measuring both the reference RO and stressed RO frequencies [2]. Fig. 6 shows the RO frequency degradation as a function of time for one particular stress voltage. The first data point plotted at 100 second of stress time when $T_{relaxation}/T_{stress}$ = 20ms/100s = 0.02%. This mitigates the effect of BTI recovery on the analysis as the recovery depends on the ratio between stress time and relaxation time [5]. As expected, combined NBTI and PBTI frequency degradation is the highest. RO frequency degradation due to NBTI effect was slightly higher than the one due to PBTI in the technology we used for this study. The frequency degradation due to NBTI in

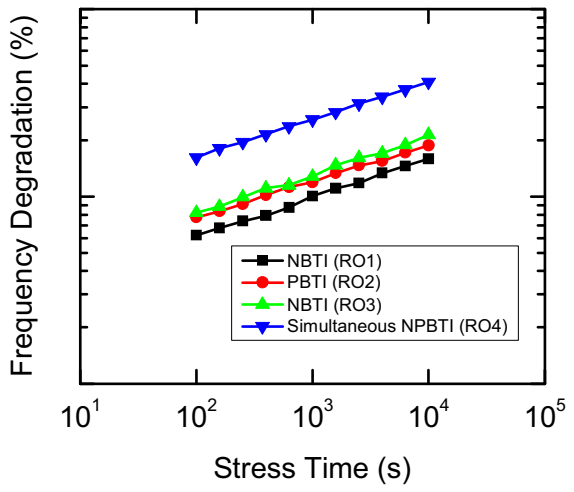

Fig. 6 RO frequency degradation vs. stress time. NBTI results from RO1 and RO3 differ because W_{PDUT}/W_{PB}= 1:1 in RO1 and W_{PDUT}/W_{PB}= 1:9 in RO3.

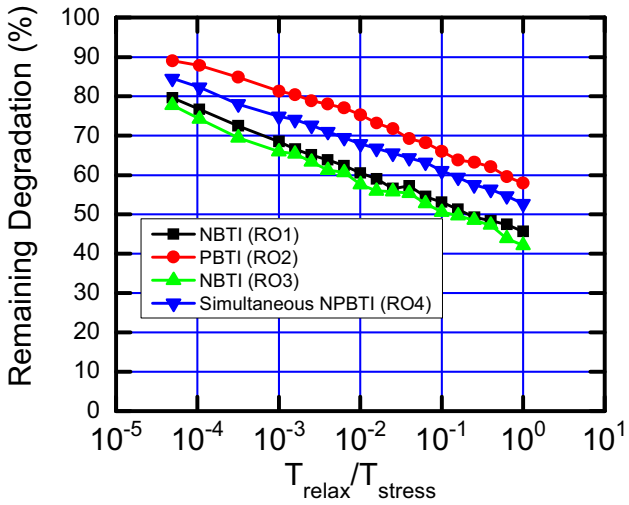

Fig. 7 Remaining Frequency degradation vs. ratio between relaxation time and stress time (relaxation starts after 10,000s stress)

RO3 is larger than in RO1 because device width ratios between PDUT and PB are different (1:1 in RO1 and 1:9 in RO3). The larger PB width makes the overall RO frequency more sensitive to the Vth change in PDUT. The impact of recovery during relaxation is shown in Fig. 7. NBTI relaxes faster than PBTI, which is consistent with previously reported device level data [6].

Fig. 8 shows that frequency degradation from simultaneous N/PBTI stress is close to the sum of degradations from individual NBTI and PBTI as expected. Measurement results for different stress voltages showed that the slope for voltage acceleration for PBTI (~5.6) is steeper than the one for NBTI (~4.3), which is consistent with a device level measurement report [7].

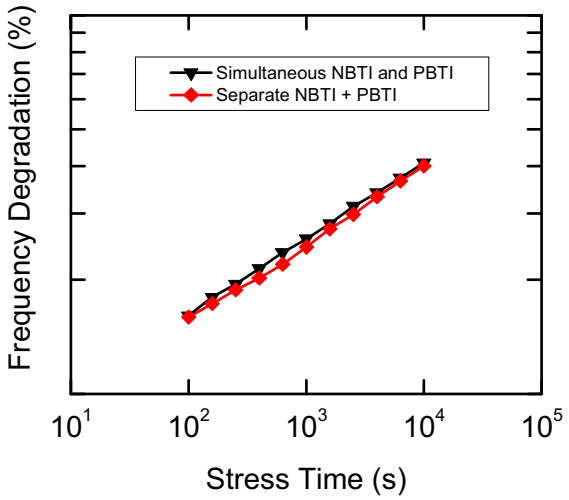

Fig. 8 RO4 frequency degradation comparison between simultaneous N/PBTI stress case and sum of individual NBTI and PBTI stress cases.

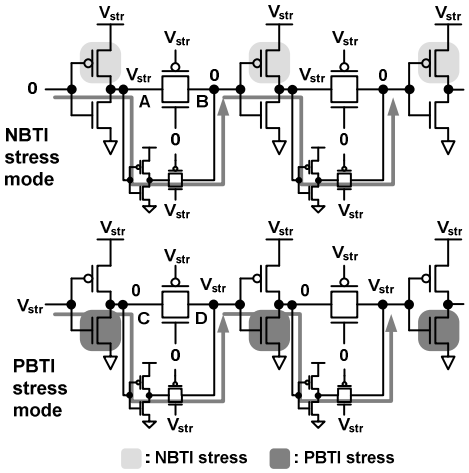

Fig. 9. Alternative circuit topology implemented in a SiO_2/poly-gate technology (stress mode)

III. Implementation in a SiO_2/poly-gate technology

Fig. 9 depicts an alternative transmission-gate based structure. The circuit consists of two signal paths; a measurement path for frequency measurements and a control path for applying NBTI or PBTI stress. During stress mode, the transmission gate in the measurement path is cut off while that in the control path is turned on. Signal A is inverted and transferred to B, making the input of each inverter in the measurement path identical. For static NBTI stress, the primary input of the ring oscillator is connected to ground in order to stress all PMOS transistors. Likewise, the input of the ring oscillator is connected to Vstr for PBTI stress. We implemented the circuit in a SiO_2/poly-gate technology. As shown in Fig. 10, the RO frequency is degraded noticeably after NBTI-only stress but there is little change in RO frequency after PBTI-only stress. This, combined with measurement results from the high-k/metal gate technology in the previous section, confirms that the proposed RO structures successfully isolate NBTI and PBTI effects. Fig. 11 shows the die photo for the design.

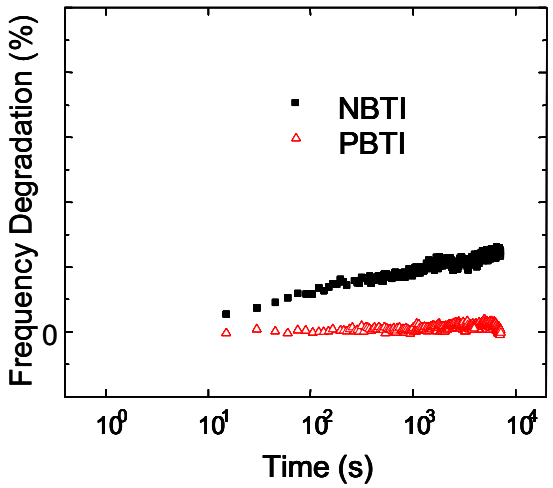

Fig. 10. RO frequency degradation comparison between NBTI stress and PBTI stress for the proposed circuit (Fig. 9) in SiO_2/poly-gate technology

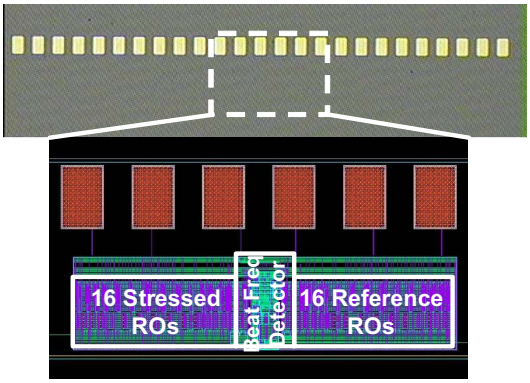

Fig. 11 Die micrograph and layout for BTI monitor in Fig. 9 (372x90µm^2)

IV. Summary

We propose new ring oscillator circuits which monitor NBTI and PBTI separately. In case the conventional ring oscillator circuit is used for characterization of model-to-hardware correlation for NBTI and PBTI, it can only provide overall frequency degradation information due to combined NBTI and PBTI effects. In such a case, the modeled value of each BTI component can be quite different from the real value even when the overall degradation is close to the values from the models. The proposed circuits can provide information for each BTI component and enables more accurate model-to-hardware correlation.

Acknowledgment

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