A 1.1V, 667MHz Random Cycle, Asymmetric 2T Gain Cell Embedded DRAM with a 99.9 Percentile Retention Time of 110µsec

Ki Chul Chun, Pulkit Jain, Tae-Ho Kim, Chris H. Kim

Dept. of ECE, University of Minnesota, 200 Union Street SE, Minneapolis, MN 55455, USA (Email: chunx041@umn.edu)

Abstract

A logic compatible embedded DRAM test macro fabricated in a 65nm LP CMOS process has a 512 cells-per-BL array architecture and achieves a random access frequency and latency of 667MHz and 1.65nsec, respectively at 1.1V, 85°C. The refresh period for a 99.9% bit yield was 110µsec. Key features include an asymmetric 2T gain cell, a pseudo-PMOS diode based current sensing scheme, a half swing write BL driver, and a stepped write WL technique.

Introduction

The ever-increasing demand for larger on-die caches is facing critical scaling challenges. 6T SRAM has been the memory cell of choice but its ratioed operation has resulted in shrinking operating margins. 1T1C embedded DRAMs (eDRAMs) have replaced SRAMs in several server and mobile applications improving performance with 4X higher bit-cell density and a random cycle time around 2nsec [1,2]. However, the additional process steps, destructive read operation, and the weak access transistor necessary to meet retention time targets make 1T1C cells less attractive in future process technologies. Gain cells which are typically 2X denser than SRAM cells are logic compatible and offer good low voltage margin by having decoupled read and write paths and a read port capable of driving a bit-line load [3,4,5]. Attaining practical retention times and improving random access speed remain as key challenges in gain cell eDRAM designs. In this paper, we present circuit techniques for realizing a 1.1V, 667MHz random cycle eDRAM with a retention time comparable to that of a 1T1C cell.

Asymmetric 2T Gain Cell

PMOS only gain cells were used in recent designs for improving retention time as they have roughly an order of magnitude lower gate leakage compared to their NMOS counterparts [3,4]. However, the poor channel mobility of PMOS devices limits the read performance. The new 2T gain cell structure proposed in this work achieves a long retention time without sacrificing read speed by using a Read Word-line (RWL)-connected NMOS read device for high drive current and a PMOS write device to keep the speed critical data '1' voltage close to VDD. Fig. 1 shows the proposed 2T cell and a previous Asymmetric 3T Cell (ATC) which was chosen for comparison because it also contains both NMOS and PMOS devices, albeit the structure and operating principle are different [5]. In the ATC cell, a PMOS device was used for the write access transistor to extend the cell retention time by compensating the NMOS gate leakage with the PMOS gate overlap and junction leakages. However, the leakage compensation effect of this cell is poor under PVT variations because the gate leakage through the inverted channel of the NMOS storage device is dominant for data '1' as shown in Fig. 1. In the proposed cell, the read access transistor is replaced by the RWL signal whose pre-charge level is VDD. The storage transistor is nominally off making its gate leakage negligible. Since there is no subthreshold leakage through the read path, low Vth transistors can be utilized to further improve read speed. Monte-Carlo simulations in Fig. 1 show that the data '1' voltage which determines the read speed is 0.26V higher than the ATC cell at the same retention time while the voltage window between data '1' and data '0' is improved by 0.18V.

Current Sense Amplifier with a Pseudo-PMOS Diode

Unlike 3T cells, Read Bit-Line (RBL) voltage of 2T cells must be clamped during sensing to prevent the leakage current of the unselected cells from causing a read failure as illustrated in Fig. 2 (top). The small voltage swing results in a poor read sensing margin. To overcome this problem, a Current-mode Sense Amplifier (C-S/A) is employed in our design to hold the RBL voltage close to VDD while sensing, allowing a large number of low Vth cells to be connected to a single RBL. The proposed C-S/A shown in Fig. 2 (bottom) consists of a PMOS latch and a pseudo-PMOS diode gated by the negative supply which is already present on-chip for the Write Word-Line (WWL) under-drive. The two PMOS pairs in saturation mode have better matching with voltage headrooms similar to that in [6] ensuring robust sensing. The proposed C-S/A shows stable operation for up to 512 cells on a single RBL without a significant read delay penalty. As a result, BL-S/As account for only 4.5% of the total array area even with the additional C-S/A and write-back circuit shown in Fig. 4. Fig. 3 shows a 192kb test array structure with a 512 cells/BL and 192 cells/WL architecture featuring the proposed 2T cell, BL-S/A, RWL split pull-down driver to suppress ground noise, and upsized dummy cells to minimize random variation. Fig. 6 shows simulated waveforms for a 1.5nsec random cycle time considering cell voltage distributions, random Vth variations of the selected and dummy cells, and the C-S/A mismatch.

Half Swing Write BL Driver and Stepped Write WL Scheme

With a fast read operation, write-back delay becomes the performance bottleneck as it is directly proportional to the Write Bit-Line (WBL) capacitance. By using a half swing WBL scheme with a tri-state buffer shown in Fig. 4, the write speed is improved by 50% and the average WBL charging current is reduced by 25% without sacrificing retention characteristics of the proposed 2T cell. DRAMs require a positive boosted voltage (VPP) to suppress the subthreshold leakage in the write access device as well as a negative boosted voltage (VBB) to write data into the cell without a Vth drop. In order to reduce the power and area overhead of charge pumps during fast chip operation, we adopted a stepped WWL control scheme which minimizes the current drawn from the boosted VPP and VBB voltages by utilizing the main VDD and GND supplies for most of the WWL transition as shown in Fig. 5. With this stepped WWL control scheme, 60% of the boosted supply current and 4.4% of the chip area can be saved with two additional peripheral control signals and four more transistors in the WWL control circuit.

EDRAM Chip Measurements

A 192kb eDRAM macro was implemented in a 1.2V, 65nm low-power logic CMOS process for concept verification. Cell retention time characteristics were efficiently collected using a fully-automated chip test setup including a LabView™ controlled logic-analyzer/pattern-generator module and on-chip BIST circuits. The chip microphotograph and key features are shown in Fig. 11. For a 99.9% bit yield at 1.1V and 85ºC, our design achieves a 667MHz random cycle for a 110µsec refresh period, and a 500MHz random cycle for a 1200µsec refresh period as shown in Fig. 7. Fig. 8 shows the measured retention time spatial map for a 1kb sub-array. The large number of cells/BL and random Vth variations in the dummy cell and C-S/A resulted in multiple weak cells in the RBL direction. This can be easily fixed by column redundancy. By adjusting the VPP level which affects subthreshold and gate overlap leakages, optimal retention time can be achieved considering both data '1' and data '0' as shown in Fig. 9. This dependency can be exploited for post-fabrication trimming to cope with die-to-die variations. The fabricated chip has a wide operating voltage range from 1.4V down to 0.8V (Fig. 10).

Acknowledgements

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References

[1] J. Barth, ISSCC, pp.486-487, 2007. [2] S. Romanovsky, ISSCC, pp.270-271, 2008. [3] D. Somasekhar, ISSCC, pp.274-275, 2008. [4] K. Chun, VLSI Circuits Symp., pp. 134-135, 2009. [5] M. Ichihashi, VLSI Circuits Symp, pp. 366-369, 2005. [6] J. Sim, VLSI Circuits Symp, pp. 294-297, 2002.

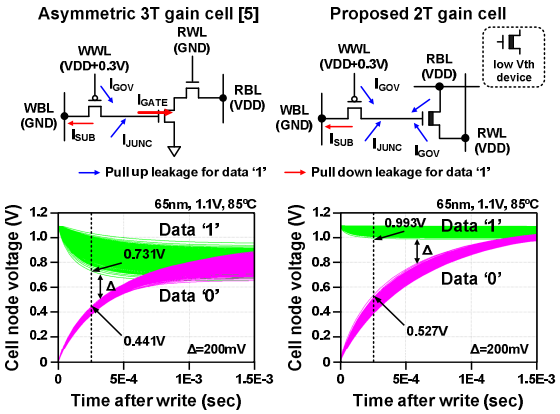


Fig. 1. Schematics and retention characteristics under Tox and Vth variations of the previous Asymmetric 3T Cell (ATC) and the proposed 2T gain cell.

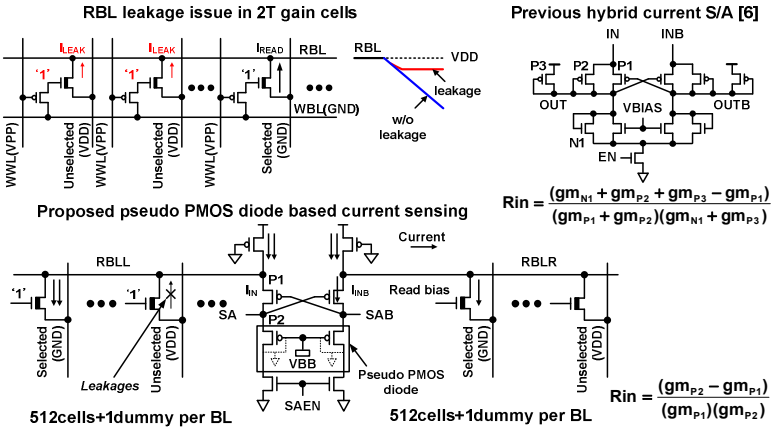


Fig. 2. Read Bit-Line (RBL) leakage issue in 2T gain cells (top) and the proposed Current Sense Amplifier (C-S/A) utilizing a pseudo-PMOS diode pair (bottom).

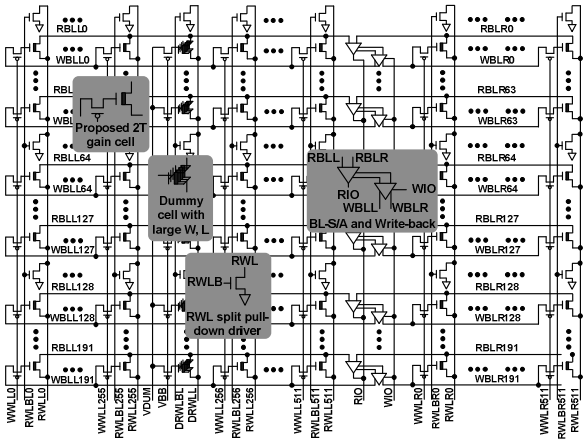


Fig. 3. A 192kb test macro structure with a 512 cells/BL and 192 cells/WL array architecture.

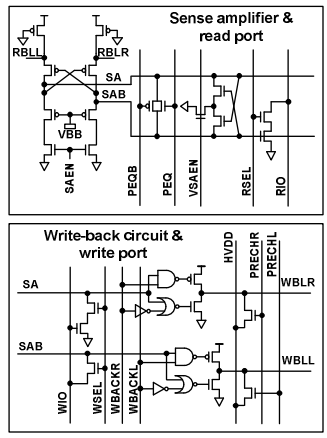


Fig. 4. Complete schematic of the C-S/A, read port, write-back circuit, and write port.

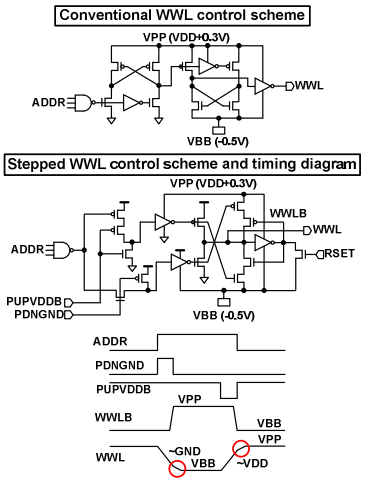


Fig. 5. Stepped Write Word-Line (WWL) control scheme.

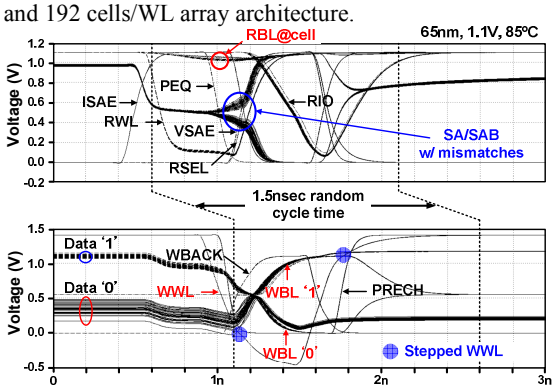


Fig. 6. Signal waveforms simulated with BL-S/A mismatches and cell node voltage variations at a 1.5ns random cycle time for read and write-back operation.

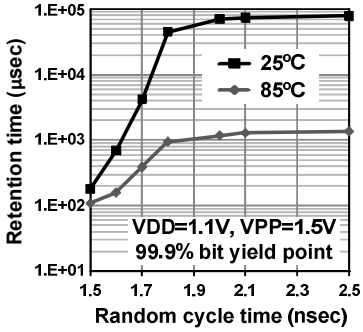


Fig. 7. Measured random cycle time versus retention time at the 99.9% bit yield point.

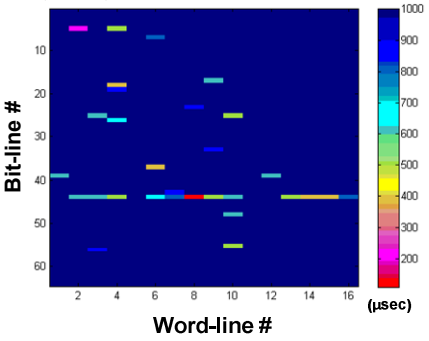


Fig. 8. Measured retention time bitmap of a 1kb sub-array at 1.1V, 85ºC, and 1.5nsec random cycle time.

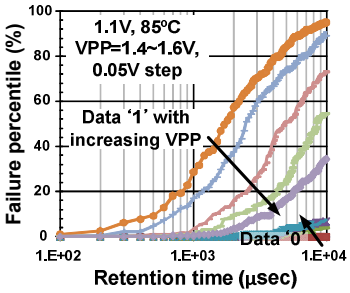


Fig. 9. Measured retention time distribution versus VPP level for data '1' and data '0' in hold mode.

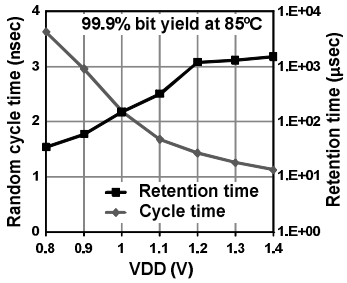
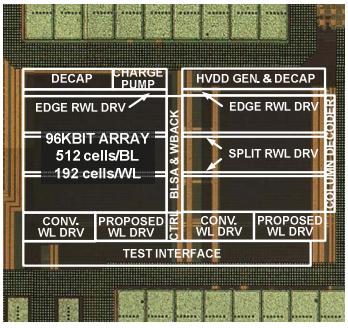


Fig. 10. VDD shmoo of random cycle time and corresponding retention time.



Process	65nm LP CMOS
Ckt dimension	556 x 298µm²
Array size	192kb (192 WLs, 2x512 BLs)
Cell size	41% of 6T SRAM
* Retention time @ 1.1V, 85ºC	110µs @ 667MHz 1200µs @ 500MHz
Latency	1.39ns @ 1.2V 1.65ns @ 1.1V
** Refresh power @ 1.2V, 85ºC	2.09mW/Mb @ 667MHz 248µW/Mb @ 500MHz

* 99.9% bit yield condition
** 100µsec refresh rate for 667MHz
1000µsec refresh rate for 500MHz

Fig. 11. Die photo and key features of the eDRAM test chip.