Microelectronics Reliability 50 (2010) 1039–1053

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Introductory Invited Paper

On-chip reliability monitors for measuring circuit degradation

John Keane [a,b], Tae-hyoung Kim [a,1], Xiaofei Wang [a], Chris H. Kim [a,*]

[a] Department of Electrical and Computer Engineering, University of Minnesota, 200 Union Street SE, Minneapolis, MN 55455, United States
[b] Intel Corporation, Ronler Acres 3, 2501 NW 229th Avenue, Hillsboro, OR 97124, USA

ARTICLE INFO

Article history:
Received 4 April 2010
Received in revised form 15 April 2010

ABSTRACT

Front-end-of-line reliability issues such as Bias Temperature Instability (BTI), Hot Carrier Injection (HCI), and Time Dependent Dielectric Breakdown (TDDB) have become more prevalent as electrical fields continue to increase in scaled devices. The rapid introduction of process improvements, such as high-k/metal gate stacks and strained silicon, has lead to new reliability issues including BTI in n-type devices. Precise measurements of the circuit degradation induced by these reliability mechanisms are a key aspect of robust design. This article will review a number of unique test chip designs pursued by circuit designers that demonstrate the benefits of utilizing on-chip logic and a simple test interface to automate circuit aging experiments. This new class of compact on-chip sensors can reveal important aspects of circuit aging that would otherwise be impossible to measure, and can lead us down the path to real-time aging compensation in future processors.

1. Introduction

The Integrated Circuits (IC) design community is facing unprecedented challenges as CMOS technology approaches its fundamental limit. Process variability, leakage power and device reliability issues have emerged as serious problems that nullify the performance benefits gained by traditional device scaling. In particular, the parametric shifts or circuit failures caused by device reliability issues such as Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), and Time Dependent Dielectric Breakdown (TDDB) have become more severe with shrinking device sizes and voltage margins.[2] Aging-related circuit degradation has been an unfamiliar notion to most chip designers until recently, as its impact was not significant in previous systems where the heat dissipation was moderate and operating margins were sufficient. However, the higher voltage stress and elevated temperatures in modern chips are causing circuit aging to become an increasingly important design consideration in high performance systems. Moreover, process improvements such as high-k/metal gate devices have introduced new degradation concerns including positive-BTI in n-type devices, adding to the already complex aging behavior [1].

Semiconductor companies generally deal with this aging problem by playing it safe. For example, operating frequencies of their products are relaxed to ensure they will continue to operate over the intended product lifetime [2,3]. This means that clocks have to be slowed down to well under the limits for fresh circuits in order to account for the impending logic slow-down that comes with aging, among other variables. By doing so, manufacturers throw out a portion of the performance benefit that comes with scaling because of problems that could arise after long periods of use. Device dimensions have now been pushed to the atomic scale, though, and we are approaching physical limitations where transistors no longer act as reliable switches. In addition, manufacturers are facing significant challenges in the fabrication process which could become too costly to surmount. In this environment where we cannot count on continued performance improvements from scaling alone, making conservative estimations about circuit aging will no longer do. Research, design, and process development groups are all now devoting significant resources to better understanding the aging mechanisms, and exploring strategies to reduce the cushion put into clock speeds or maximum operating voltages.

One critical aspect of that work involves developing accurate and efficient means to measure the effects of the different aging mechanisms on circuit parameters. This review article introduces a new class of test structures that can efficiently collect circuit aging data using compact on-chip circuits. This new paradigm provides a number of benefits over traditional device probing, such as higher measurement resolution, shorter stress interruptions, reduced test structure area, shorter test times, and simpler test setups. The remainder of this paper is organized as follows. Section 2 provides a brief introduction on the three major transistor degradation mechanisms. Section 3 introduces ring oscillator based test structures to measure the frequency degradation in digital circuits. A novel circuit that can separate the effects of HCI and BTI is introduced in Section 4, followed by an array based circuit for fully-automated characterization of TDDB in Section 5. Measured

* Corresponding author. Tel.: +1 612 625 2346; fax: +1 612 625 4583.
E-mail address: chriskim@umn.edu (C.H. Kim).

[1] Present address: School of Electrical & Electronic Engineering, Nanyang Technological University, Block S1, 50 Nanyang Avenue, Singapore 639798, Singapore.

[2] This review article will focus on front-end-of-line reliability concerns.

0026-2714/$ - see front matter © 2010 Elsevier Ltd. All rights reserved.
doi:10.1016/j.microrel.2010.04.024

data collected from a number of odometer test chips are shown to demonstrate the benefits of utilizing on-chip logic and a simple test interface to automate aging experiments. Finally, in Section 6, we will summarize the benefits and shortcomings of utilizing on-chip reliability monitors and make concluding remarks.

2. Overview of device aging mechanisms

As shown in Fig. 1, CMOS devices suffer from HCI, BTI, and TDDB stress under standard digital operating conditions. This section will briefly examine these three major front-end-of-line reliability mechanisms that circuit designers should be aware of.

HCI degradation appears when a large drain-to-source voltage and gate-to-source voltage is applied [4–10]. Hot carriers (i.e. those with high kinetic energy) accelerated toward the drain by the corresponding lateral electric field across the channel lead to secondary carriers generated through impact ionization (Fig. 2a) [11,12]. Either the primary or secondary carriers can gain enough energy to be injected into the gate stack. This creates traps at the silicon substrate/gate dielectric interface, as well as dielectric bulk traps, and hence degrades device characteristics such as the threshold voltage (V_{th}). These "traps" are electrically active defects that capture carriers at energy levels within the bandgap. HCI is more prominent in NMOS transistors since the majority carriers are electrons, which face a smaller potential barrier than holes at the gate oxide interface. This aging mechanism has become less prominent with the reduction of operating voltages, but remains an important concern due to the high local electric fields found in scaled devices. In addition, the higher power-law time dependence exponent of HCI compared with BTI could lead to the former mechanism dominating the overall aging picture after long periods of use.

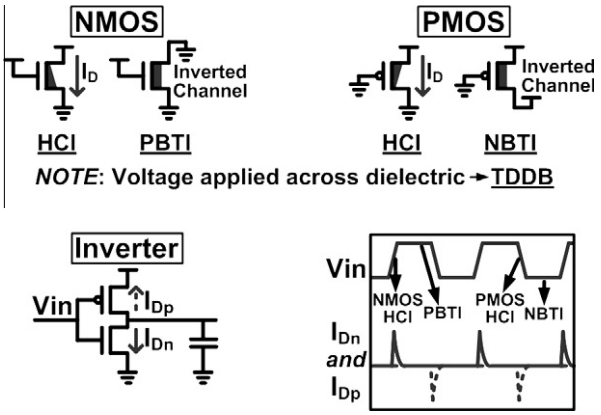


Fig. 1. HCI, BTI, and TDDB stress illustrated for NMOS and PMOS transistors, as well as for an inverter during standard operation.

Negative Bias Temperature Instability (NBTI) [13–16] in PMOS transistors is often cited as the primary reliability concern in modern processes, especially after the introduction of nitrogen into gate stacks, which reduces boron penetration and gate leakage, but leads to worse NBTI degradation [17]. This mechanism is characterized by a positive shift in the absolute value of the PMOS V_{th}, which occurs when a device is biased in strong inversion, but with a small, or no, lateral electric field (i.e. $V_{DS} \approx 0$ V). The V_{th} shift is generally attributed to hole trapping in the dielectric bulk, and/or to the breaking of Si–H bonds at the gate dielectric interface by holes in the inversion layer, which generates positively charged interface traps (Fig. 2c) [17,18]. When a stressed device is turned off, it immediately enters the "recovery" phase, where trapped holes are released, and/or the freed hydrogen species diffuse back towards the substrate/dielectric interface to anneal the broken Si–H bonds, thereby reducing the absolute value of the V_{th} (Fig. 2d) [19–25]. Positive Bias Temperature Instability (PBTI) in NMOS transistors was not critical in silicon dioxide dielectrics (such as those used in the test circuit implementations presented here), but is now contributing to the aging of high-k gate stacks [1].

Finally, voltage across the gate stack can cause the creation of traps within the dielectric. These defects may eventually join together and form a conductive path through the stack in a process known as TDDB, or oxide breakdown (Fig. 2b) [26–30]. Oxide breakdown has been a cause for increasing concern as gate dielectric thicknesses are scaled down to the one nanometer range, because a smaller critical density of traps is needed to form a

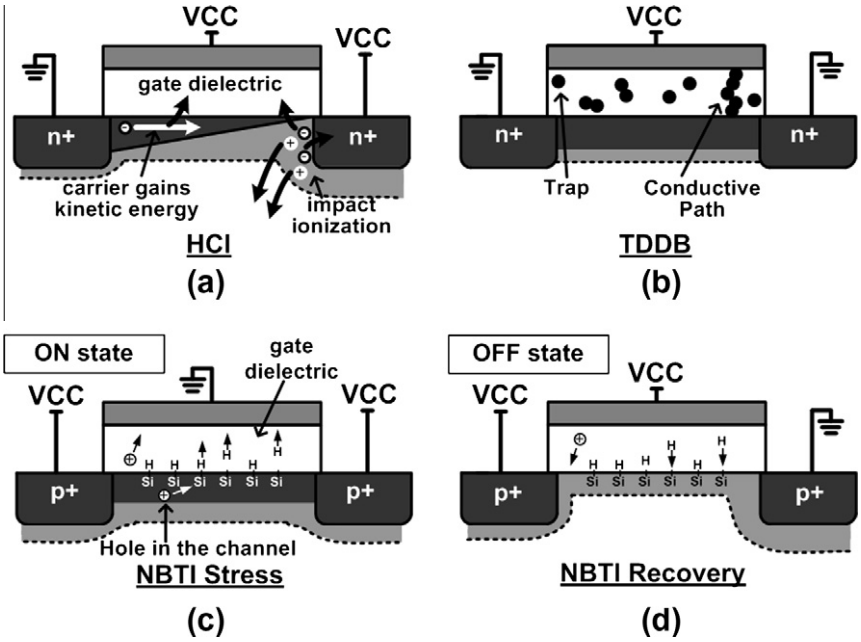


Fig. 2. Transistor cross sections illustrating (a) HCI, (b) On-state TDDB, (c) NBTI stress, and (d) NBTI recovery. PBTI is equivalent to NBTI in a PMOS but occurs in an NMOS device.

conducting path through these thin layers, and stronger electric fields are formed across gate insulators when voltages are not reduced as aggressively as device dimensions [31,32]. While TDDB has traditionally been studied under inversion-mode stress conditions, it can also happen during an off-state stress condition where a high drain bias can cause a breakdown in the gate-to-drain overlap region [33–35]. The scaling of the physical dimensions of gate stacks can now be slowed or reversed with the introduction of high-k dielectrics, but TDDB remains a critical aging mechanism in those materials, and is currently being studied extensively by reliability physicists [1,36].

3. Techniques for measuring degradation in digital circuits

This section will start by outlining the design goals of a degradation monitor design and describing possible circuit techniques to meet the required specifications. This is followed by experimental data collected from several test chip designs gathered under various stress conditions that demonstrate the effectiveness and convenience of using on-chip sensors for reliability monitoring.

The primary goal is to implement an on-chip test structure that can measure extremely small shifts in circuit operating frequency induced by BTI and HCI, within a very short measurement window. These two requirements are essential in reliability monitor designs, as realistic stress data can only be obtained under relaxed stress conditions that require a high sensing precision, while unwanted BTI recovery can only be prevented by having a short measurement time (e.g. less than a microsecond). A degradation monitor should also be able to independently characterize the different aging mechanisms (focus of Section 4), perform sensitivity analysis under various stress conditions, occupy a reasonably small silicon area, and preferably use a fully-digital test interface for convenient off-chip testing. The aforementioned requirements for the on-chip reliability monitor can be met using a novel beat frequency detection concept illustrated in Fig. 3 [37,38]. (Note that, although we chose to measure circuit frequency rather than current–voltage characteristics in this design, the latter can be recorded with an array based circuit which will be discussed in Section 6.)

3.1. Illustration of the beat frequency concept

The operation of the beat frequency detection scheme is as follows. During the short measurement periods, a phase comparator uses a fresh reference Ring OSCillator (ROSC) to sample the output of an identical stressed ROSC. The phase comparator can be built using a standard D-flip-flop circuit with outputs from the two ring oscillators connected to the data and clock inputs, respectively [37]. In this configuration, the output of the stressed ROSC is sampled at every rising edge of the reference ROSC output producing a signal that exhibits the beat frequency as shown in Fig. 3 (right). ROSCs can be either put into stress mode or kept fresh by switching the local power supply to VSTRESS or ground respectively using on-chip devices. The output signal of this phase comparator exhibits the beat frequency, which is the difference between the frequencies of the two ROSCs. A counter is used to measure the beat frequency by counting the number of reference ROSC periods during one period of the phase comparator output signal. This count is recorded after each stress period to calculate the shift down in the stressed ROSC frequency.

Suppose the initial frequency of the reference ROSC is called f_{ref}, that of the fresh ROSC to be stressed is f_{stress}, and the initial output count is N_1. Also, without the loss of generality, we can assume that f_{ref} is slightly higher than f_{stress}. This condition can be achieved in a real chip using frequency trimming circuits and a simple scan-in test interface. The period of the beat frequency signal is the time it takes for the reference ROSC to accumulate N_1 periods and for the stressed ROSC, which has a slightly lower frequency, to accumulate $(N_1 - 1)$ periods. This one clock period difference arises from the fact that the output of the stressed ROSC with a longer period will take one less period to cycle back and align with the output of the reference ROSC. Hence, the period of the beat frequency signal can be expressed as:

$$1/f_{ref} \cdot N_1 = 1/f_{stress} \cdot (N_1 - 1). \tag{1}$$

At the end of a stress period, f_{ref} will remain unchanged, but f_{stress} will be decreased due to aging, and we call the new frequency f'_{stress}. We also have a new output count (N_2), so the resulting equation is:

$$1/f_{ref} \cdot N_2 = 1/f'_{stress} \cdot (N_2 - 1). \tag{2}$$

Using these two equations, we can calculate a frequency shift during stress as follows:

$$\frac{f'_{stress} - f_{stress}}{f_{stress}} = \frac{N_1 \cdot (N_2 - 1)}{N_2 \cdot (N_1 - 1)} - 1 = \frac{(N_2 - N_1)}{N_2 \cdot (N_1 - 1)}. \tag{3}$$

Those simple calculations show that if f_{ref} is only slightly higher than f_{stress}, the output count is high. For example, the count N_1 is 100 for a 1% frequency difference. This slight difference can be ensured with trimming capacitors and calibration. The subsequent small decreases in f_{stress} due to aging cause a large change in this count. For instance, a 2% difference between the ROSC frequencies gives an N_2 of 50, so a 1% shift to that point is translated into a decreased count of 50. Consider another example in which the count value changes from 100 before stress, to 99 after stress. In this scenario, the corresponding frequency shift according to Eq. (3) can be calculated as

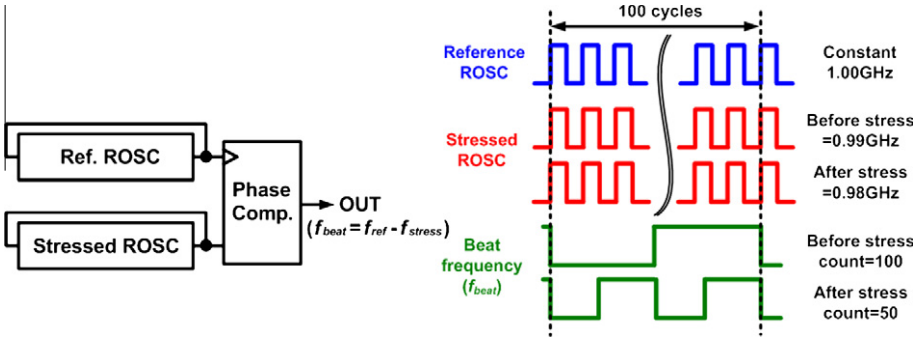


Fig. 3. Concept behind the beat frequency detection system. Small frequency shifts induced by circuit aging are magnified by measuring the beat frequency (i.e. Δf) rather than the actual frequency of a single ring oscillator. The technique can be implemented using simple digital logic and a scan interface readily available in chips for testing.

$$\frac{f'_{stress} - f_{stress}}{f_{stress}} = \frac{(99 - 100)}{99 \cdot (100 - 1)} \approx -0.010\%. \quad (4)$$

Therefore, with high frequency ROSCs, the beat frequency detection system can achieve extremely high measurement resolution on the sub-picosecond order. It is important to note that the number of counts required to obtain such high resolution is very small (i.e. around 100 ROSC cycles). This is crucial for preventing the fast BTI recovery that occurs within microseconds after the stress conditions are removed for measurements. It is also worth noting that although most of the published data confirm that microsecond measurement times do not results in any measureable recovery, some papers suggest the possibility of fast recovery down to several hundred nanoseconds [39,40].

The output count relationship with the difference between the reference ROSC (REF_ROSC) and stressed ROSC (STR_ROSC) frequencies is illustrated in Fig. 4a. This figure shows that the odometer operates correctly with a reference ROSC frequency that is either slower or faster than the stressed ROSC. In the former case, the output count will increase with stress, while it decreases in the latter. We choose to start experiments with a reference frequency that is slightly faster than the stressed ROSC frequency which results in a monotonic decrease in the output count. This allows for a maximum frequency measurement resolution in the early phases of stress, and to avoid the dead zone shown in Fig. 4a.

Fig. 4b shows measurement result characteristics with monotonic count decreases, and four different initial counts. Note again that a smaller difference between the two ROSC periods leads to a higher initial count, and therefore a higher initial frequency resolution, while lengthening the measurement time. Typical starting counts of ~125 were used in our hardware measurements, which correspond to initial frequency shift resolution ranging down to 0.0065%. The resolution decreases with time, but we are primarily concerned with the small initial degradation steps which can be obtained with stress that is closer to real operating conditions. It has been shown that stress at excessively high voltages, for example, can lead to unrealistic degradation characteristics that are not useful for predicting device lifetimes under standard operating conditions [41,42].

Fig. 5 compares the beat frequency technique with other ROSC based systems for monitoring frequency shifts. The scheme denoted as "single ROSC" measures the output of one ROSC whose frequency is divided down by a counter for easier off-chip frequency measurements using test equipments [23]. The "two ROSC, simple" scheme measures the degradation in one stressed ROSC by counting the number of periods it cycles through during a set number of reference ROSC periods [43]. An edge capture scheme can be with any of these techniques to count the number of stages (rather than ROSC periods) an input edge could travel through before and after stress [40,44]. This added feature could potentially make the measurements faster in all three designs, but due to the considerable circuit overhead associated with the design, we do not include it in the comparison table.

The resolution of the first two schemes in Fig. 5 is simply the measurement time divided by the ROSC period, while that of the beat frequency technique can be derived from Eq. (3). We see that the latter technique reaches a maximum resolution of 0.01% within only 0.3 μs with a single measurement recorded, while the other systems require 100X more time to reach the same accuracy. The longer measurement times in the standard period counter systems would result in unwanted BTI recovery which can occur within a few microseconds or less. In addition to the high frequency resolution, the beat frequency technique benefits from a high immunity to voltage or temperature variations due to its differential nature. Given that the reference and stressed ROSCs are identical structures that are laid out next to each other, both ROSCs will see essentially identical temporal variations, so their frequencies should be affected by roughly the same amount. Simulation data provided in the bottom row of Fig. 5 verifies that both the "two ROSC, simple" and "two ROSC, beat frequency" schemes have significantly less error compared to the "Single ROSC" scheme in the presence of common mode supply voltage fluctuations. Comparing the area of the three sensor configurations is rather difficult since most papers including [23,38,43] do not mention the circuit area. This is understandable as these implementations were not meant for embedding in a real product but for process characterization purposes. Considering that these reliability sensors are simpler than the critical path monitors widely used in real products such as the one described in [45], we do not anticipate the sensor area to be a major concern. In case of applications with stringent area requirements, one may choose to further optimize the sensor

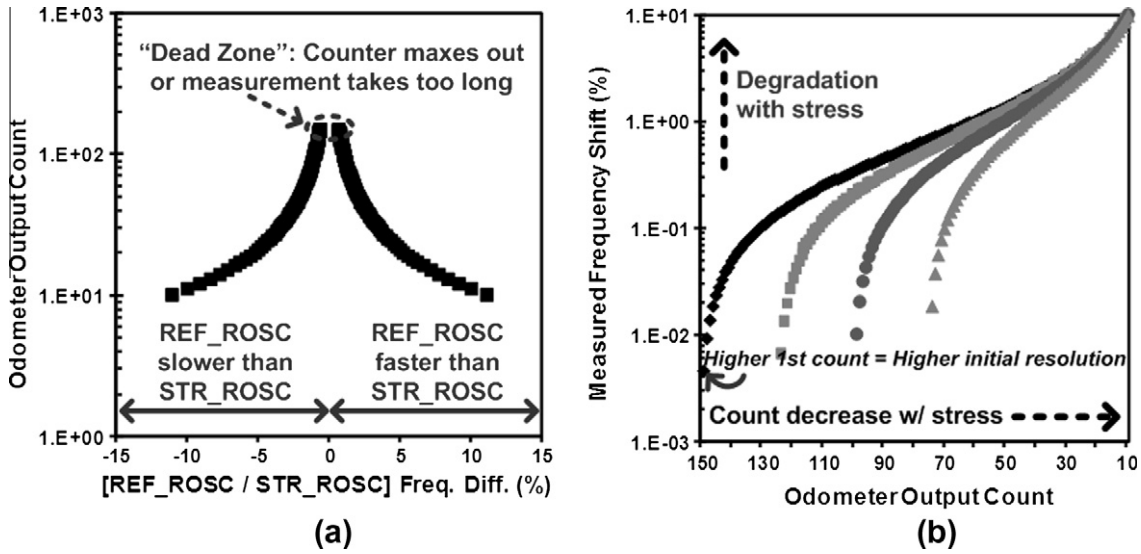
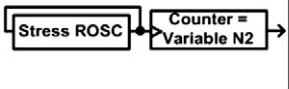
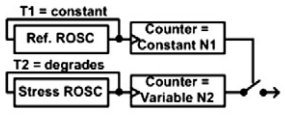
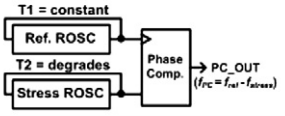


Fig. 4. (a) Sensor output count vs. the frequency difference between the reference and stressed ROSCs. When the two frequencies become extremely close, a high output count is observed, which provides a higher precision but requires a larger counter and longer measurement time. (b) Output count vs. frequency shift during a stress experiment. Curves are shown for varied initial counts, where a higher count corresponds to a smaller frequency difference between the two ROSCs, as was shown in part (a) of this figure.

System	Single ROSC	2 ROSC, simple	2 ROSC, beat freq.
Block Diagram			
Function	Count Stress ROSC periods during externally controlled meas. time	Count Stress ROSC periods during N1 periods of Ref. ROSC	Count Ref. ROSC periods during one period of PC_OUT
Features	Simple; compact	Simple; immune to common mode variations	High resolution w/ short meas. time; immune to common mode variations
Issues	Voltage and temp. varations; meas. time vs. resolution tradeoff; requires absolute timing reference (e.g. oscilloscope)	Meas. time vs. resolution tradeoff	Requires extra circuits (e.g., Phase Comp., edge detector, etc...)
Meas. time for 1% max resolution *	30 μs	30 μs	0.3 μs
Meas. error wrt. common mode variations **	+10.18% / -8.57%	+0.26% / -0.38%	+0.06% / -0.07%

*ROSC period = 3 ns ** simulated with +/- 4% ΔVCC

Fig. 5. Comparison of ring oscillator based systems for frequency shift measurements.

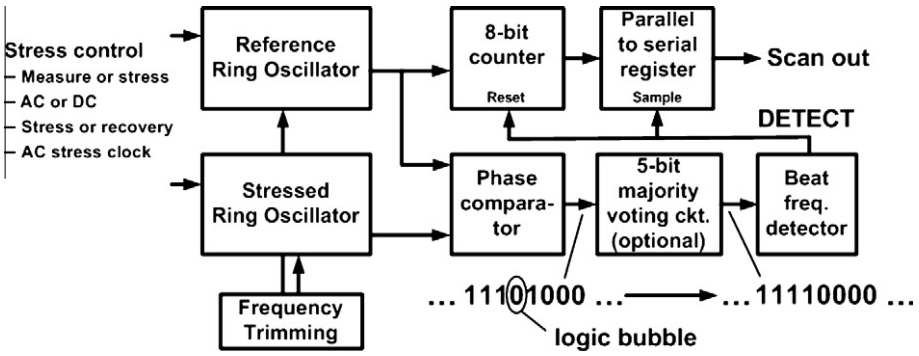


Fig. 6. High level circuit diagram of the beat frequency detection system.

area by reducing the number of ROSC stages or simplifying the control logic.

In summary, the beat frequency technique achieves a significantly higher frequency measurement resolution (sub-picosecond) in a shorter measurement time (sub-microsecond) than traditional measurement techniques with only a modest increase in the number of circuits, and is immune to common mode environmental variations.

3.2. Chip implementation and test procedure

A high level circuit diagram of the beat frequency detection technique is shown in Fig. 6. The two ring oscillators are identical structures with different control signals which minimize any systematic mismatch due to layout differences. Thick oxide Input/Output (I/O) devices are used for the stress control so that no appreciable degradation occurs in these circuits. As described above, the phase comparator produces an output signal exhibiting the beat frequency between the reference and stressed ring oscillators. Logic bubbles (e.g. a lone '1' in a bit stream of '0's) that may occur due to signal jitter and other circuit uncertainties are eliminated using a majority voting circuit. We decided to use a 5 bit majority voting circuit which can filter out two bubbles in a sequence of 5 bits. This optional circuit block consists of five flip-flops required to store the previous 5 bit data and several NAND and NOR gates to perform the Boolean operation of a majority function. A longer majority circuit (e.g. 7 bit, 9 bit, and so on) can eliminate more bubbles but requires additional flip-flops and complex gates, and has a longer measurement time. The DETECT pulse generated by the beat frequency detector block samples the counter value and resets the counter for the next measurement cycle. A parallel-to-serial register is used for scanning out the results.

The entire measurement was automated with LabVIEW™ software through a National Instruments data acquisition board. During the initial setup, capacitor trimming circuits were used to ensure that the frequencies of the stressed and reference ROSCs are close to each other to increase the measurement resolution. Both ring oscillators contain trimming circuits allowing for a wider and finer calibration range. An initial count of 100–150 was used in all experiments as this was the highest we could reliably achieve using the trimming circuits while preventing injection locking between the two ROSCs. The frequency measurement resolution cor-

responding to the initial counts was 0.01% or less which was sufficiently high for our purpose. An 8 bit counter was implemented in the test chip to accommodate a counter output up to 256. Fresh chips were used in each measurement because, circuits will not fully recover to their initial fresh state after stress. A stress clock generated by an on-chip voltage controlled oscillator (VCO) was

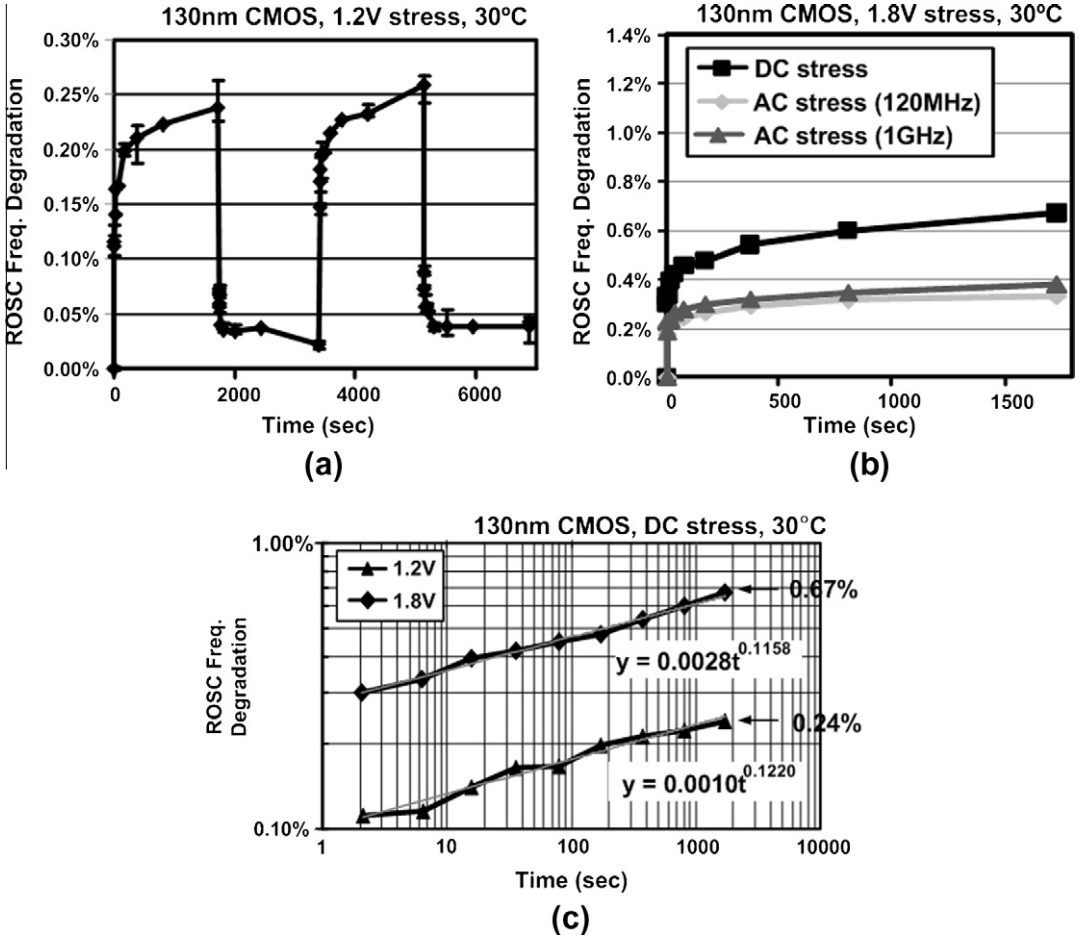


Fig. 7. Measurement results: (a) A common saw tooth curve showing the stress-recovery characteristics. (b) Frequency degradation under DC and AC stress. (c) Frequency degradation for different stress voltages.

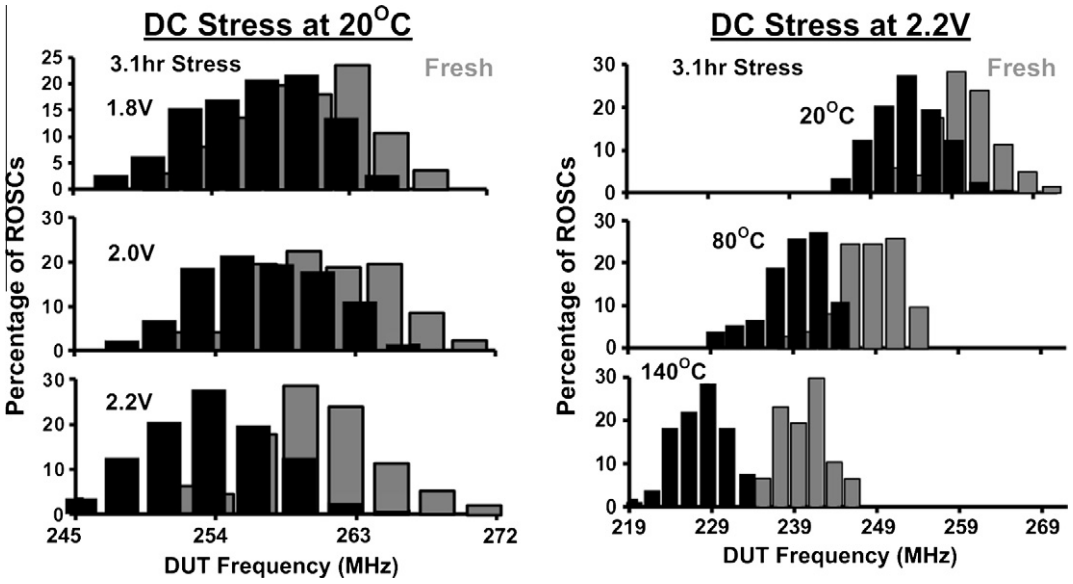


Fig. 8. Statistical aging data collected from an array of ROSCs in a 65 nm CMOS process using the beat frequency technique.

used for the AC stress experiments. An analog bias voltage is used to set the VCO frequency, and an external MEAS_STRESS signal is pulsed to initiate each measurement period. This signal triggers various internal control signals timed and driven properly by an on-chip finite state machine. The supply voltages of the stressed and reference ROSCs are switched to the nominal supply voltage from VSTRESS and 0 V, respectively. The power gating devices were sized such that the supply switching is completed within a few nsecs. Three counts are taken for each measurement and are post-processed to calculate the actual frequency degradation, which ensures robust results. Note that the two ROSCs are automatically sent back to their respective stress or no stress conditions as soon as the three beat frequencies have been measured in order to achieve measurement times of $\leqslant 1$ μs.

3.3. Chip measurement results

Measured data from a 1.2 V, 130 nm bulk CMOS test chip under various stress conditions are shown in Fig. 7. The observed stress-recovery characteristic is shown in Fig. 7a which follows the expected saw-tooth waveform. The ROSC frequency shift after the first stress period was 0.238% at a nominal 1.2 V and 30 °C stress condition. Removing the stress voltage for the same amount of time resulted in a 90.5% recovery from the maximum frequency shift point. DC and AC stress measurement results are shown in Fig. 7b. DC stress results are purely based on BTI degradation while AC stress at higher frequencies may include some HCI degradation. DC stress shows significantly worse degradation compared with AC stress, while no noticeable difference was observed between the two AC stress frequency measurements. This could be attributed to the fact that: (i) BTI is dominant at shorter time frames and that (ii) BTI is at most weakly dependent on switching frequency [46]. An improved odometer circuit that allows us to examine the contribution of HCI and BTI separately will be presented in Section 4. Fig. 7c shows the frequency degradation measured at two stress voltages. As expected, frequency shift follows a power-law behavior and the fitted curves have exponents of 0.1220 and 0.1158 for stress voltages of 1.2 V and 1.8 V, respectively.

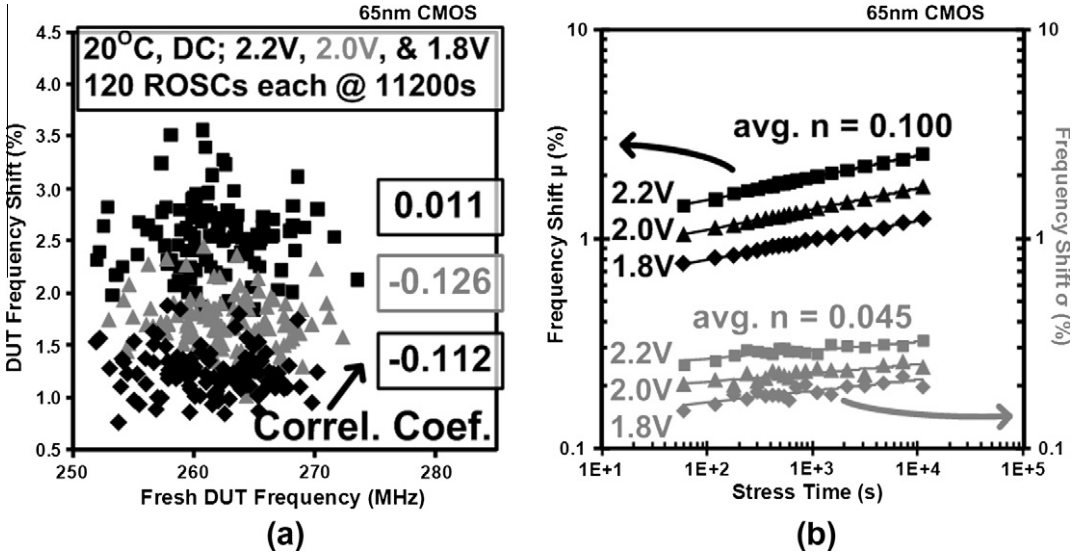


Fig. 9. (a) No significant correlation of the % frequency shift with fresh frequency. (b) Time evolution of mean and standard deviation of the % frequency shift.

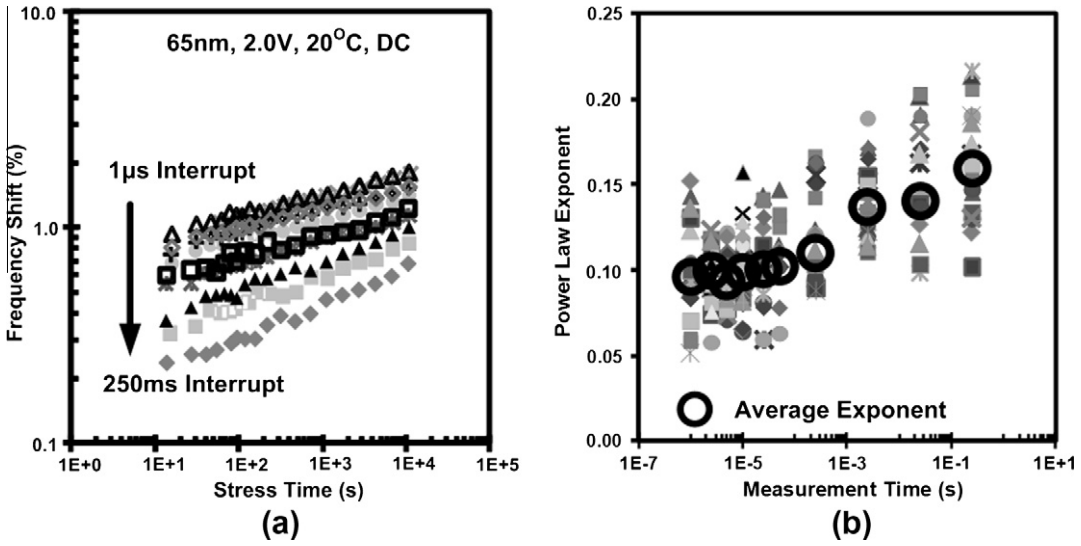


Fig. 10. (a) Steeper slopes for longer stress interruptions due to recovery. (b) Power law exponent vs. measurement time.

The beat frequency framework can be extended to efficiently gather statistical aging data from an array of ROSCs which are stressed in parallel. Measurement results in Fig. 8 from another test chip design, built in a 1.2 V, 65 nm CMOS process, illustrate the probability density functions of fresh and stressed ROSCs after 3.1 h of DC stress at different stress voltages and temperatures. Each distribution is based on measurements from 100 ROSCs. The primary degradation mechanism at work in these experiments was NBTI, since PBTI is not significant when high-k dielectrics are not used, and there was no switching during stress.

In Fig. 9a we see that there was no significant correlation between the fresh ROSC frequency and the stress-induced shift. This lines up with previous findings that the stress-induced V_{th} mismatch in PMOS pairs was uncorrelated to the initial mismatch [47], and that the initial spread in the V_{th} is not correlated to that caused by aging [48]. Fig. 9b shows the average (μ) frequency shifts and the standard deviation (σ) of the shifts vs. stress time. The σ increases with stress [48–50], roughly following a power law with an exponent (n) of just under 1/2 that of the μ shift. Therefore, the σ/μ ratio of the shift decreases with stress time [51].

The short but programmable measurement time of the proposed circuit also allows us to quantify the impact of measurement times on BTI results, as shown in Fig. 10. Long interruptions take up a significant portion of the total experiment time at early measurement points. This means a large percentage of the time is spent in recovery state, which pulls down the early results and leads to a steeper degradation slope, as seen in Fig. 10a. Several previous publications have clearly demonstrated this phenomenon [52–55]. Fig. 10b shows the power law exponents that were fitted to the data from different measurement times. Results show that stress interruptions of tens of microseconds or less are required to observe the average power law exponent of ~0.1 under the listed DC stress conditions. The significant spread in the range of exponents observed at each measurement time (roughly ±0.05) illustrates the variation in the aging process, and the importance of characterizing a statistically significant sample set.

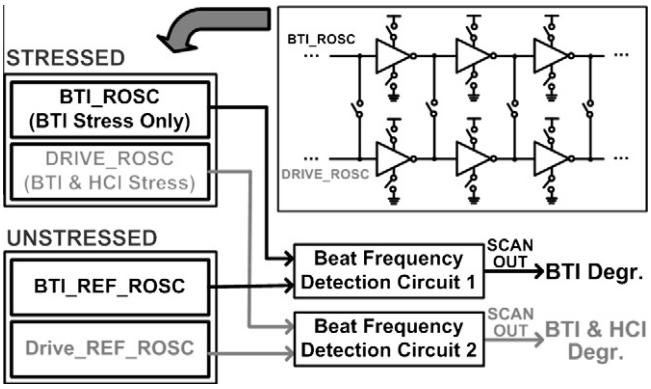


Fig. 11. Proposed system for separately monitoring BTI- and HCI-induced frequency degradation. TDDB degradation can also be observed with long-term or high voltage stress experiments.

4. Circuit technique for separately monitoring HCI and BTI

In order to examine the contributions of HCI and BTI to overall circuit degradation, an on-chip monitor capable of subtracting out the BTI component is needed. This is because a normal circuit will undergo both BTI and HCI under standard voltage switching conditions, so the circuits-based HCI/BTI measurement design must focus on isolating the effects of these two mechanisms. This section describes an odometer circuit that achieves this goal in addition to meeting the requirements of the generic frequency degradation monitor discussed in the previous section (i.e. high precision, fast measurement time, and an all digital implementation).

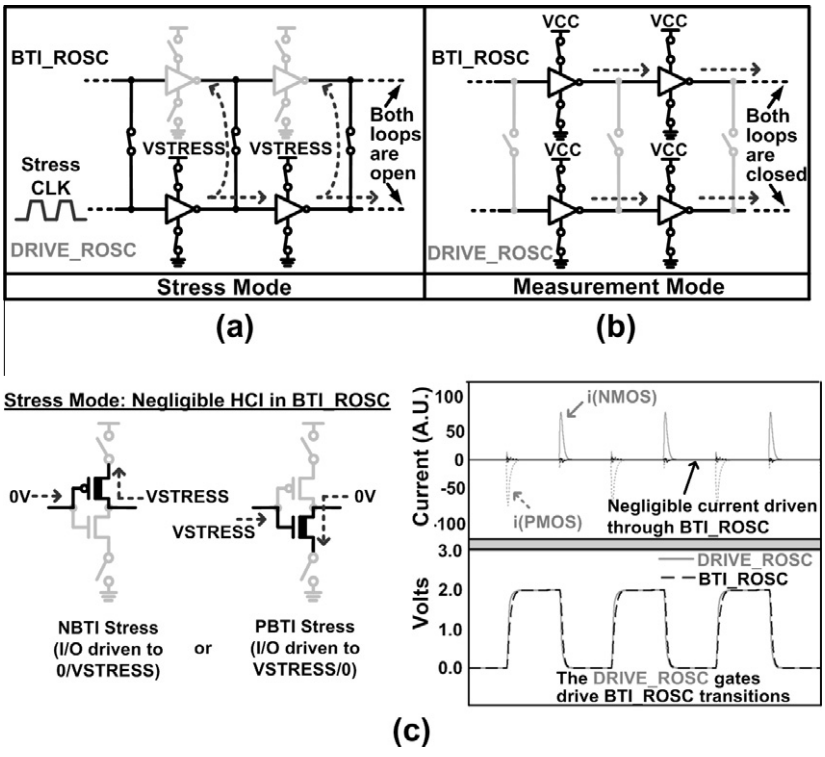


Fig. 12. ROSC configuration during (a) stress (b) measurement modes.and (c) the BTI_ROSC transistors suffer the same amount of BTI as the DRIVE_ROSC transistors during stress, but with negligible HCI degradation, since very little current is driven through the channels of the devices under test the former structure.

4.1. Illustration of the backdrive concept

A block diagram of the proposed odometer for separately measuring HCI and BTI is shown in Fig. 11 [56,57]. This circuit contains four ROSCs in total: two stressed, and two unstressed to maintain fresh reference points. Each of the stressed oscillators is paired with its identical fresh reference during measurements, and its frequency degradation is monitored with the beat frequency detection circuit described in the previous section. All ROSC structures are identical to ensure minimal drift under Process-Voltage–Temperature (PVT) variation. The switches were sized up enough to prevent them from becoming a bottleneck to the switching transients in the inverters. This makes the behavior of the proposed circuit representative of that of a standard inverter based ROSC. Fig. 12 presents the pair of stressed ROSCs in both (a) stress and (b) measurement modes. During stress, the BTI_ROSC stages are gated off from the power supplies, while the DRIVE_ROSC maintains a standard inverter configuration with the supply set at VSTRESS. Both ROSC loops are opened, and the input of the DRIVE_ROSC is driven by a stress clock generated by an on-chip clock source. The switches between these two ROSCs are closed so the DRIVE_ROSC can drive the internal node transitions for both structures.

Simulated voltage and current waveforms are shown in Fig. 12c. The internal nodes of the BTI_ROSC switch between the supply level (VSTRESS) and 0 V, as would be the case in standard operation. However, the peak drain current though the "on" devices in this structure is only 3–5% of that in the DRIVE_ROSC, since their sources are gated off from the supplies. Note that the sources of these "on" devices in the stressed BTI_ROSC are held at their respective supply levels due to the backdriving action of the DRIVE_ROSC. Therefore, the BTI_ROSC will age due only to BTI stress, while the DRIVE_ROSC suffers both BTI and HCI. We can extract the contribution of HCI to the latter ROSC's frequency degradation with the equation $HCI_{DEG} = DRIVE_{DEG} - BTI_{DEG}$, where DEG stands for degradation. During measurement periods, both ROSCs are connected to the digital logic power supply (VCC) and the switches between them are opened, so they each operate independently in a standard closed-loop configuration. Each delay stage contains two header switches and two footer switches (not shown in the figure for simplicity) [57]. One pair is used for stress and the other pair (which is kept fresh) is only used during measurements.

4.2. Test chip measurements

A die photo and a summary of the 65 nm HCI/BTI odometer test chip characteristics are presented in Fig. 13, along with a picture of the test lab setup. Fig. 14 presents example measurement results for both ROSCs under AC and DC stress. HCI-induced degradation is calculated by subtracting out the effects of BTI on the DRIVE_ROSC results. As expected, both BTI and HCI degradation follow a power-law behavior, although the latter is seen to saturate at long stress times. This can be explained by the finite number of bonds to be broken at the Si–SiO_2 interface and/or the self-limiting nature of

Technology	65 nm, 7M
Logic/IO Supplies	1.2 V / 2.5 V
Active Area	38,040 μm^2
Total Area	(214.22 X 551.43) μm^2
ΔT Resolution	< 1 ps
Measure Interrupt	< 1 μs

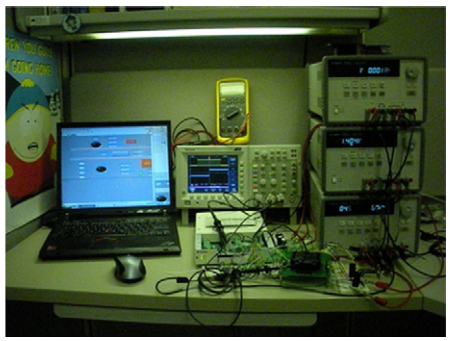


Fig. 13. Test chip microphotograph, summary of characteristics, and chip measurement environment.

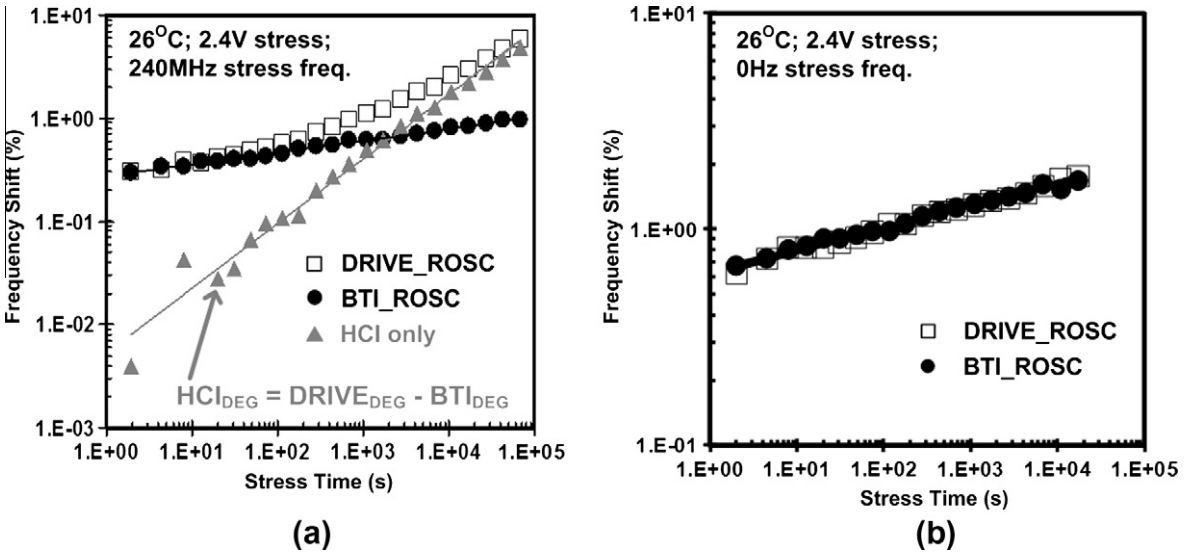


Fig. 14. Example measured results with AC stress conditions. HCI-induced degradation is calculated by subtracting out the effects of BTI on the DRIVE_ROSC results.

HCI, where the degraded drain current produces fewer hot carriers. The power law exponent for BTI in this case was 0.12, while that of HCI was 0.63 in the range fitted on this plot. The larger value for HCI is expected, and one possible reason for this is an increasing contribution of broken Si–O bonds at the oxide interface during HCI stressing, rather than Si–H bonds [58,59].

Fig. 15a illustrates the impact of frequency on BTI and HCI. These results verify that BTI is at most weakly dependent on frequency, while HCI degrades with increased switching activity. More switching leads to an increase in current driven through the channels, meaning more hot carriers are present. A decrease in the power law exponent of HCI was observed at higher frequencies, which is apparently due to the quick saturation of degradation in this case. In Fig. 15b, we see that increased load capacitance, which causes longer transition times, accelerated HCI and had little impact on BTI. This acceleration of HCI with both increased input transition time and output load capacitance was reported in early HCI work [60,61]. Those variables have been listed as two of the

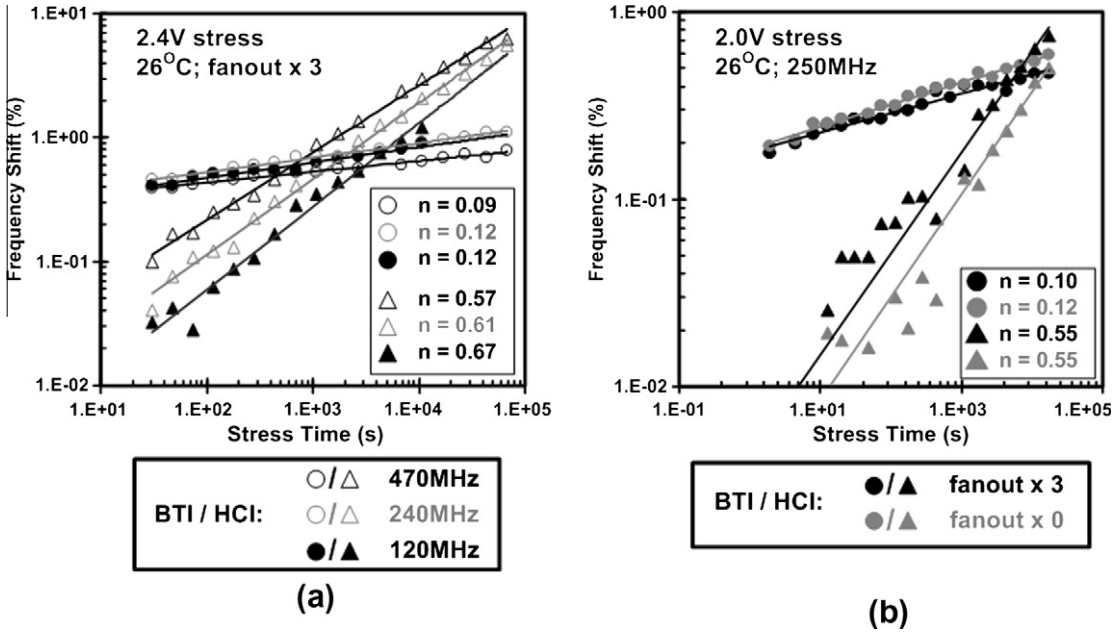


Fig. 15. Measured frequency degradation results for (a) three stress frequencies and (b) increased load capacitance, with power law exponents (n). The decreasing exponent with increasing stress frequency in part (a) is attributed to a faster saturation of the frequency degradation. Increased node cap increases transition times and leads to more hot carriers, which accelerates HCI.

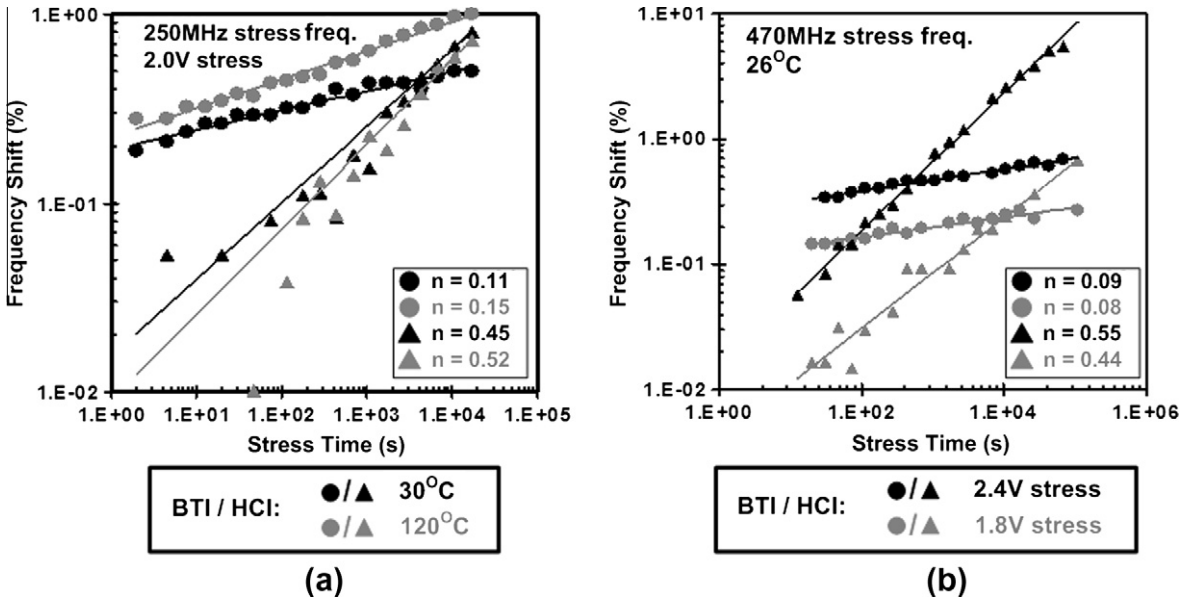


Fig. 16. Effect of (a) stress temperature and (b) stress voltage. It is well known that BTI becomes more severe with increased temperatures, while HCI is negatively correlated with temperature due to reduced carrier mobility as that parameter is increased. While both mechanisms decrease with lower stress voltages, note that the crossover point when HCI begins to dominate the overall aging is pushed out in time by more than an order of magnitude. This illustrates the assertion that BTI aging becomes dominant under real operating conditions.

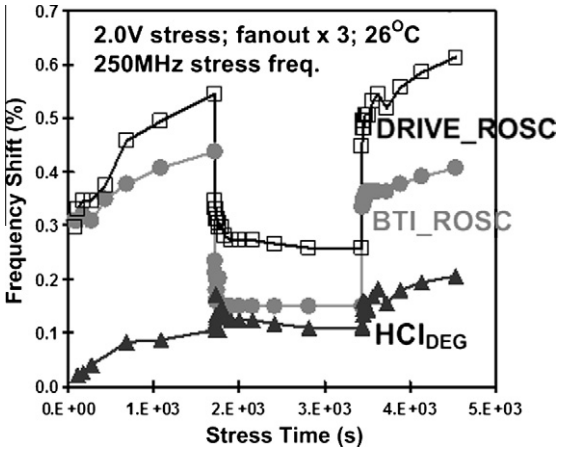


Fig. 17. Periodic stress/recovery characteristics. The BTI frequency curve shows a common sawtooth characteristic, while the HCI curve does not recover when stress conditions are removed.

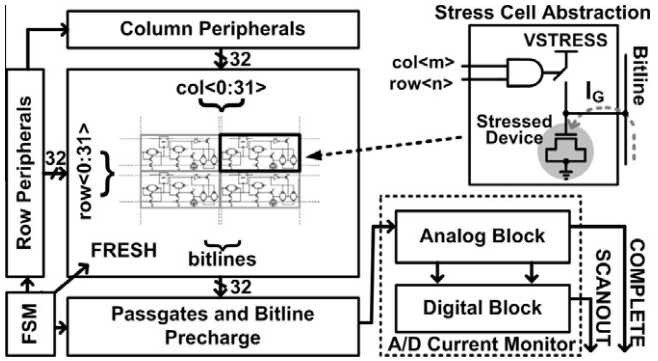


Fig. 18. Conceptual diagram of a 32×32 array for fully automated TDDB characterization.

main controllable factors affecting hot carrier-induced degradation.

Fig. 16a shows BTI's positive correlation with temperature, and that HCI aging was slightly reduced at higher temperatures due to increased phonon scattering, which reduces drain current. Both aging mechanisms degrade with voltage (Fig. 16b), and we observe a decrease in HCI's power law exponent at lower voltages. This has been explained by a possible decreasing contribution of broken Si–O bonds (in comparison to Si–H bonds) at lower voltages, closer to real operating conditions [58,59]. Also note the crossover point when HCI begins to dominate the overall aging is pushed out in time by an order of magnitude at 1.8 V stress compared to 2.4 V. This helps to illustrate the claim that BTI becomes dominant in modern technologies operating at lower supply levels. Fig. 17 shows a common NBTI recovery characteristic, while the HCI_{DEG} component did not improve when stress was removed. One explanation for this behavior is the Si–H bonds at the interface broken by cold carriers during BTI stress are recoverable, while hot carriers also break Si–O bonds, which do not recover [58,59].

5. Circuit technique for characterizing TDDB

The design goal of a TDDB odometer is drastically different from those of a BTI or HCI monitor given in the previous sections. This is due to TDDB's strong statistical component which causes identical devices to break at significantly different times. Up to thousands of measurement samples are required to observe the relevant TDDB characteristics and time-to-breakdown distributions [32,62]. This makes serial probing of individual devices a time-consuming and cumbersome process [63,64]. An automated test structure consisting of an array of transistors with dedicated stress controls can facilitate the collection of large time-to-breakdown distributions with shorter experiments through the parallel stressing of those devices under test. While this type of design would be very valuable for TDDB characterization, we do not envision it becoming a real-time monitor to trigger aging compensation schemes in products due to the statistical nature of this aging process. As such, each aging mechanism needs to be handled differently.

5.1. Illustration of the breakdown current measurement array

Fig. 18 show a TDDB characterization system consisting of a 32×32 array of structures we call "stress cells" that contain the Devices Under Test (DUTs), whose gate currents (I_G) are periodically measured using an Analog-to-Digital (A/D) current monitor and on-chip control logic [65]. After an initialization sequence, cells are cycled through automatically without the need to send or decode cell addresses, in order to simplify the logic and attain faster measurement times. The stress cell was implemented to facilitate the accelerated stressing of the DUTs by using thick oxide I/O transistors in the supporting circuitry to avoid excessive aging or breakdown in these other devices. (The dual-oxide requirement for the present design is commonly met by modern processes, but implementing stressing circuits with a single oxide thickness is also possible using a number of circuit tricks. A test chip has been recently taped out by the authors to demonstrate this concept.) A switch drives the DUT gate to the stress voltage if the cell has been turned on for a stress test.

Gate currents (I_G) are periodically measured using an A/D current monitor and on-chip control logic. Automatic measurements were completed with LabVIEW™ software and a National Instruments data acquisition board connected to a laptop. During a pre-stress calibration procedure, the current monitor is run normally, as it would during stress measurements, but with a range of known off-chip resistance values. This step allows us to map DUT gate resistance values to the circuit's digital outputs. A microphotograph of the chip and a summary of the circuit characteristics are shown in Fig. 19. In the picture on the right of this figure, which captures a larger portion of the total chip, we point out a number of individual devices that were fabricated to verify that the results from the array match well with probing measurements.

5.2. TDDB characterization array measurements

Cumulative distribution functions (CDF) of the time to breakdown, both on a standard percentage scale as well as the Weibull scale, are displayed in Fig. 20a and b, respectively. That data was

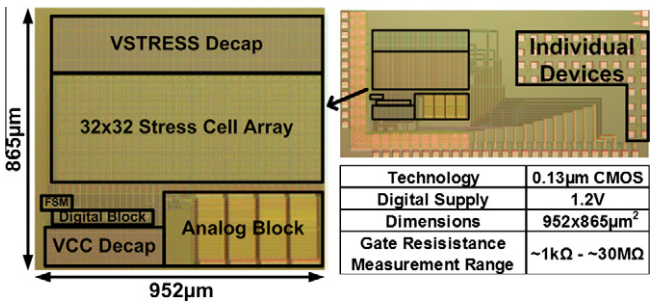


Fig. 19. Microphotograph and summary of the test chip characteristics. The individual devices reserved for probing experiments are labeled to the right of the TDDB array measurement system.

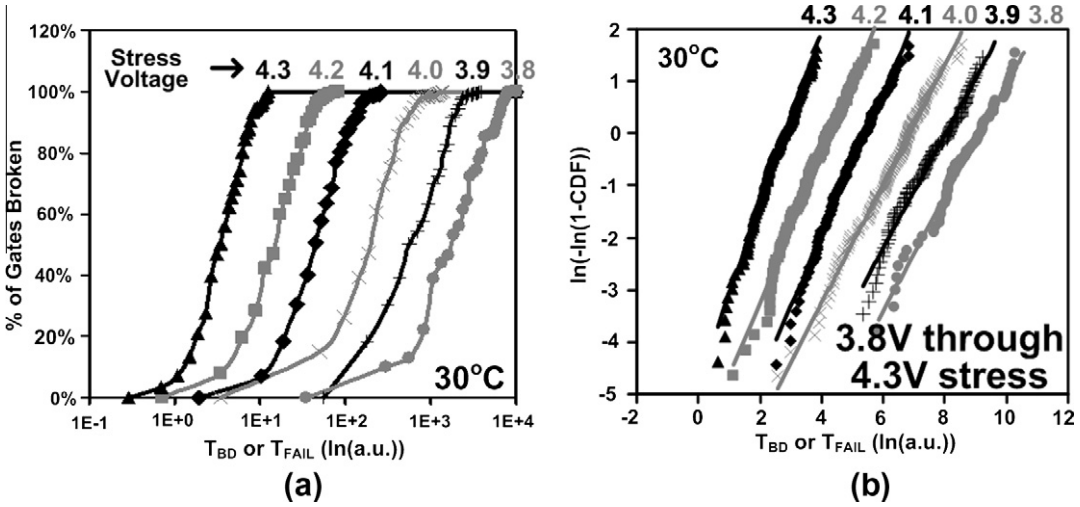


Fig. 20. Measured T_{BD} CDFs on (a) a standard percentage scale and (b) a Weibull scale.

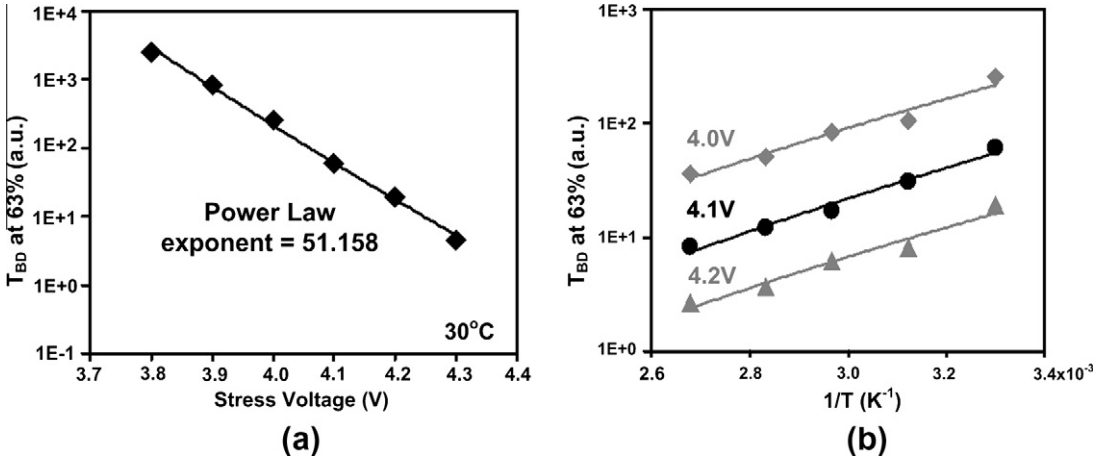


Fig. 21. (a) Voltage acceleration of T_{BD} at the 63% point. (b) T_{BD} at the 63% point vs. the inverse of the temperature in Kelvins.

gathered at 30 °C, with stress voltages from 3.8 V to 4.3 V in this 1.2 V process. TDDB follows Weibull statistics because this mechanism has a weakest-link character. There are a large number of spots in each gate where the first breakdown can occur, and the breakdown process proceeds independently at each of them. The first breakdown at any of those locations leads to device degradation or failure though, so it can be thought of as the "weakest link." When we have a weakest-link process, extreme value distributions are the first functions we try to fit measured data. Since in the case of time to breakdown the distribution is bounded from below at time zero, specifically we use a Weibull distribution [66]. The Weibull slope factor (β) for 4.2 V stress was 1.443, with that factor slightly decreasing for lower stress voltages, and increasing at 4.3 V. The slope values are in good agreement with other published data [32,67].

The exponential relationship of the Weibull characteristic life (time at which 63% of the devices have failed) with voltage is illustrated in Fig. 21a. The power law exponent is ~51, which is slightly larger than that reported in previous work where the time to the first breakdown event (soft or hard) was recorded [68]. Note that Wu et al. provided a physics-based explanation for voltage acceleration power law factors in the 40–50 range in that paper. The measured dependency of the time to breakdown on stress temperature is shown in Fig. 21b for a range of voltages. In this temperature range of 30–100 °C, TDDB follows Arrhenius behavior with only small errors. Although the temperature dependence of breakdown is often modeled using Arrhenius behavior, non-Arrhenius dependence has also been reported at temperatures over 100 °C, particularly for thin gate dielectrics [69,70]. At any rate, the temperature acceleration of TDDB imposes more severe limits on

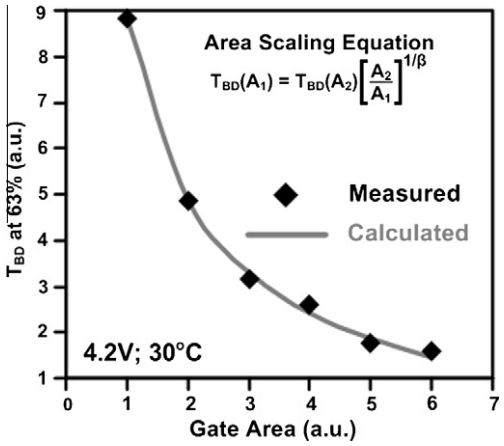


Fig. 22. Area scaling data computed from the combined measurement results of spatially adjacent stress cells, compared with theoretical results.

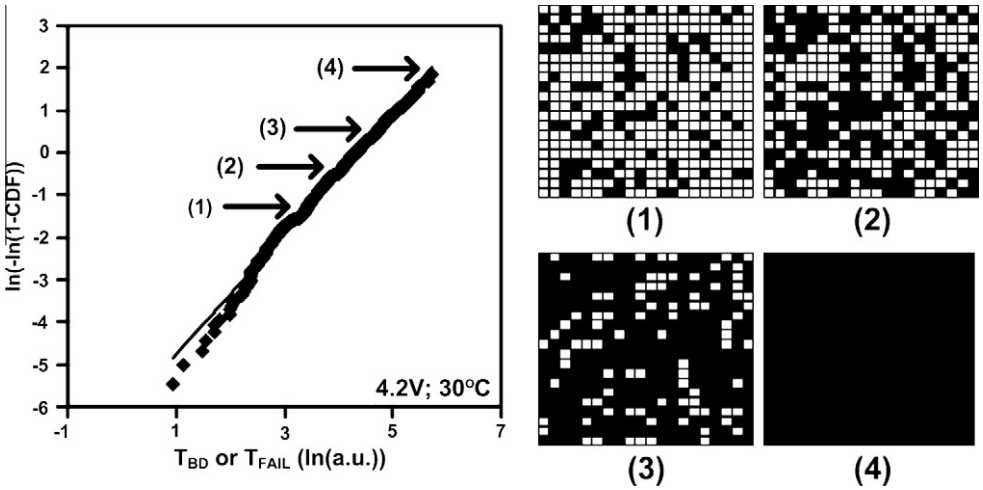


Fig. 23. Spatial distribution of TBD in a 20 × 20 stress cell array at four time points on the Weibull scale CDF. Cell locations are filled in once their DUT gates have broken down.

modern CMOS designs where device density and high clocking rates lead to increased local heating.

The fact that CDFs are in the form of a straight line on a Weibull scale justifies the use of extreme value statistics to describe the TDDB process. This can be further verified by checking the area scaling property shown in Fig. 22. (Although it has long been established that TDDB follows Weibull statistics, we address this issue to illustrate the concept of area scaling.) In our test chip, since all DUTs are the same size, the measured numbers for different areas were obtained by combining the results for a given number of spatially adjacent DUTs. We then selected the smallest time to breakdown from each group, due to the weakest-link character of dielectric breakdown. The results shown in Fig. 22 indicate that our measured data matches well with the theoretical area scaling equation [32,66,68].

Test arrays where a large number of devices are closely spaced facilitate investigations of any spatial correlation in the process or characteristics being studied. For example, spatial correlation of gate oxide thicknesses could lead to a correspondingly correlated breakdown process [71]. The spatial distribution of T_{BD} in a 20×20 portion of a test array stressed at 4.2 V is plotted in Fig. 23, along with the corresponding Weibull distribution. The four spatial diagrams correspond to the four divisions of the Weibull plot representing 25% of the cells each. No spatial correlation is apparent from these plots, and we verified that conclusion quantitatively by calculating the local and global Moran's I statistics [72,73],

6. Remarks and conclusions

The parametric shifts or circuit failures caused by HCI, BTI, and TDDB have become more severe with shrinking device sizes and voltage margins. These mechanisms must be studied in order to develop accurate reliability models, which are used to design robust circuits. Another option for addressing aging effects is to use on-chip reliability monitors that can trigger real-time adjustments to compensate for lost performance or device failures. For example, the system clock could be slowed down as performance degrades, rather than adding a large frequency guard band at the beginning of the circuit's life. The need for efficient technology characterization and aging compensation is exacerbated by the rapid introduction of process improvements, such as high-k/metal gate stacks and strained silicon.

In this review paper, we have introduced a number of unique test chip designs that demonstrate the benefits of utilizing on-chip logic and a simple test interface to automate transistor aging characterization experiments. In addition to avoiding the use of expensive probing equipment, implementing on-chip logic to control the measurements enables much better timing resolution. This is critical when interrupting stress to record BTI measurements, as this mechanism is known to recover within microseconds or less. We also saw that the beat frequency detection system allows us to measure ring oscillator frequency shifts with resolution ranging down to a theoretical limit of less than 0.01%. That mix of speed and accuracy is not possible with standard off-chip equipment. This capability also allows us to obtain aging data at non-accelerated stress conditions (e.g. at a nominal supply voltage) that is closer to the actual aging occurring in a real circuit. Next, the silicon area needed to collect statistical data is significantly reduced compared with traditional device probing, as multiple test structures can share the same read-out circuitry and I/O pads. In addition, differential circuit measurements such as the beat frequency technique can mitigate the impact of supply voltage or temperature drift effects that can occur during the long stress experiments. Finally, the compact all-digital circuit structures could enable circuit prognostics in real product designs, and eventually lead us down the path to real time adaptation.

Although on-chip aging monitors are beneficial for these reasons, they do have some limitations. For instance, early technology characterization is often performed before many metallization layers are being fabricated. So process engineers will want to measure the characteristics of new transistors when only one or two metal layers are available, which would be difficult to do with anything but the most basic of on-chip circuits. In addition, device probing would still be a competitive solution for extracting analog parameters such as *I–V* or *C–V* characteristics, due to the well established test procedures. On-chip reliability monitors can be used to validate the probing results and provide more insight into circuit degradation, but we do not envision them as a complete replacement for device probing.

In conclusion, recent developments in the circuit design community on on-chip degradation monitors indicate that these new circuits can play a critical role in understanding the circuit-level aging behavior in nanoscale devices. This new capability will allow chip manufacturers to develop techniques to avoid wasteful overdesign and frequency guard banding based on pessimistic degrada-

tion projections, and hence more fully realize the benefits of CMOS scaling.

Acknowledgements

This work was supported in part by the Semiconductor Research Corporation (SRC) under award 2008-HJ-1805, and an IBM Ph.D. fellowship award. The authors would also like to thank Intel, IBM, Broadcom, AMD, Freescale, Texas Instruments, and Samsung for the technical feedback and financial support.

References

[1] Degraeve R, Aoulaiche M, Kaczer B, et al. Review of reliability issues in high-k/metal gate stacks. In: IEEE international symposium on the physical and failure analysis of integrated circuits; 2008. p. 1–6.
[2] Lee Y, Mielke N, Sabi B, et al. Effect of PMOST bias-temperature instability on circuit reliability performance. In: IEEE international electron devices meeting, December 2003. p. 14.16.11–14.
[3] Lee Y, McMahon W, Mielke N, et al. Managing bias-temperature instability for product reliability. In: VLSI technology, systems and applications, April 2007. p. 1–2.
[4] Chen Z, Hess K, Lee J, et al. On the mechanism for interface trap generation in MOS transistors due to channel hot carrier stressing. IEEE Electron Dev Lett 2000;21:24–6.
[5] Hess K, Lee J, Chen Z, et al. An alternative interpretation of hot electron interface degradation in NMOSFETs: isotope results irreconcilable with major defect generation by holes? IEEE Trans Electron Dev 1999;46:1914–6.
[6] Takeda E. Hot-carrier effects in submicrometre MOS VLSIs, solid-state and electron devices. IEE Proc I 1984;131:153–62.
[7] Acovic A, LaRosa G, Sun Y. A review of hot-carrier degradation mechanisms in MOSFETs. Microelectron Reliab 1996;36:845–69.
[8] Chan VH, Chuang JE. The impact of NMOSFET hot-carrier degradation on CMOS analog subcircuit performance. IEEE J Solid State Circ 1995;30:644–9.
[9] Yang P, Chern JH. Design for reliability – the major challenge for VLSI. Proc IEEE 1993;81:730–44.
[10] Mistry KR, Fox TF, Preston RP, et al. Circuit design guidelines for n-channel MOSFET hot carrier robustness. IEEE Trans Electron Dev 1993;40:1284–95.
[11] Mihnea A, Rudeck PJ, Chen C, et al. Direct observation of secondary ionization current in N-channel MOSFETs. IEEE Trans Electron Dev 2002;49:2301–7.
[12] Arnold D, Cartier E, Dimaria DJ. Theory of high-field electron-transport and impact ionization in silicon dioxide. Phys Rev B 1994;49:10278–97.
[13] Huard V, Denais M. Hole trapping effect on methodology for DC and AC negative bias temperature instability measurements in PMOS transistors. In: IEEE international reliability physics symposium, April 2004. p. 40–5.
[14] Denais M, Huard V, Parthasarathy C, et al. New perspectives on NBTI in advanced technologies: modeling and characterization. In: IEEE European solid-state device research conference, September 2005. p. 399–402.
[15] Vattikonda R, Wang W, Cao Y. Modeling and minimization of PMOS NBTI effect for robust nanometer design. In: IEEE design automation conference, July 2006. p. 1047–52.
[16] Ershov M, Lindley R, Saxena S, et al. Transient effects and characterization methodology of negative bias temperature instability in PMOS transistors. In: IEEE international reliability physics symposium, April 2003. p. 606–7.
[17] Ielmini D, Manigrasso M, Gattel F, et al. A new NBTI model based on hole trapping and structural relaxation in MOS dielectrics. IEEE Trans Electron Dev 2009;56:1943–52.
[18] Grasser T, Kaczer B. Evidence that two tightly coupled mechanisms are responsible for negative bias temperature instability in oxynitride MOSFETs. IEEE Trans Electron Dev 2009;56(May):1056–62.
[19] Keane J, Kim TH, Kim CH. An on-chip NBTI sensor for measuring PMOS threshold voltage degradation. In: IEEE international symposium on low-power electronics; 2007. p. 189–94.
[20] Aota S, Fujii S, Jin ZW, et al. A new method for precise evaluation of dynamic recovery of negative bias temperature instability. In: IEEE international conference on microelectronic test structures, April 2005. p. 197–9.
[21] Schlunder C, Heinrigs W, Gustin W, et al. On the impact of the NBTI recovery phenomenon on lifetime prediction of modern p-MOSFETs. In: IEEE international integrated reliability workshop, October 2006. p. 1–4.
[22] Zafar S. Statistical mechanics based model for negative bias temperature instability. J Appl Phys 2005;97:1–9.
[23] Reddy V, Krishnan A, Marshal A, et al. Impact of negative bias temperature instability on digital circuit reliability. In: IEEE international reliability physics symposium; 2002. p. 248–54.
[24] Rangan S, Mielke N, Yeh E. Universal recovery behavior of negative bias temperature instability. In: IEEE international electron devices meeting; 2003. p. 14.13.11–14.
[25] Yang T, Li MF, Shen C, et al. Fast and slow dynamic NBTI components in p-MOSFET with SiON dielectric and their impact on device life-time and circuit application. In: IEEE symposium on VLSI technology, June 2005. p. 92–3.
[26] Suñé J, Wu E, Lai W. Statistics of competing post-breakdown failure modes in ultrathin MOS devices. IEEE Trans Electron Dev 2006:224–34.
[27] Suñé J, Wu E, Tous S. A physics-based deconstruction of the percolation model of oxide breakdown. Microelectron Eng 2007;84:1917–20.
[28] Krishnan A, Nicollian P. Analytical extension of the cell-based oxide breakdown model to full percolation and its implications. In: IEEE international reliability physics symposium; 2007. p. 232–9.
[29] Lee Y, Mielke N, Agostinelli M, et al. Prediction of logic product failure due to thin-gate oxide breakdown. In: IEEE international reliability physics symposium; 2006. p. 18–28.
[30] Kerber A. Lifetime prediction for CMOS devices with ultra thin gate oxides based on progressive breakdown. In: IEEE international reliability physics symposium; 2007. p. 217–20.
[31] Degraeve R, Groeseneken G, Bellens R, et al. New insights in the relation between electron trap generation and the statistical properties of oxide breakdown. IEEE Trans Electron Dev 1998;45:904–11.
[32] Wu EY, Nowak E, Vayshenker A, et al. CMOS scaling beyond the 100 nm node with silicon-dioxide-based gate dielectrics. IBM J Res Dev 2002:287–98. March/May.
[33] Wu E, Nowak E, Wing L. Off-state mode TDDB reliability for ultra-thin gate oxides: new methodology and the impact of oxide thickness scaling. In: Reliability physics symposium proceedings, 2004. 42nd Annual 2004 IEEE international; 2004. p. 84–94.
[34] Dumin NA, Kaiping L, Shyh-Horng Y. Gate oxide reliability of drain-side stresses compared to gate stresses. In: Reliability physics symposium proceedings, 2002. 40th Annual; 2002. p. 73–8.
[35] Hofmann K, Holzhauser S, Kuo CY. A comprehensive analysis of NFET degradation due to off-state stress. In: Integrated reliability workshop final report, 2004 IEEE international; 2004. p. 94–8.
[36] Lee BH. Unified TDDB model for stacked high-k dielectrics. In: IEEE international conference on IC design and technology; 2009. p. 83–7.
[37] Kim TH, Persaud R, Kim CH. Silicon odometer: an on-chip reliability monitor for measuring frequency degradation of digital circuits. IEEE J Solid State Circ 2008;43:874–80. April.
[38] Ketchen MB, Bhushan M, Bolam R. Ring oscillator based test structure for NBTI analysis. In: IEEE international conference on microelectronics test structures; 2007. p. 42–7.
[39] Shen C, Li MF, Foo CE, et al. Characterization and physical origin of fast *V*th transient in NBTI of pMOSFETs with SiON dielectric. In: International electron devices meeting, 2006 (IEDM 06); 2006. p. 1–4.
[40] Saneyoshi E, Nose K, Mizuno M. A precise-tracking NBTI-degradation monitor independent of NBTI recovery effect. In: IEEE international solid-state circuits conference digest of technical papers (ISSCC 2010); 2010. p. 192–3.
[41] Wu E, Nowak E, Lai W. Off-state mode TDDB reliability for ultra-thin gate oxides: new methodology and the impact of oxide thickness scaling. In: IEEE international reliability physics symposium; 2004. p. 84–94.
[42] Wu E, Nowak E, Vayshenker A, et al. CMOS scaling beyond the 100 nm node with silicon-dioxide-based gate dielectrics. IBM J Res Dev 2002:287–98. March/May.
[43] Stawiasz K, Jenkins KA, Pong-Fei L. On-chip circuit for monitoring frequency degradation due to NBTI. In: IEEE international reliability physics symposium, 2008 (IRPS 2008); 2008. p. 532–5.
[44] Gebara F, Hayes J, Keane J, et al. Delay-based bias temperature instability recovery measurements for characterizing stress degradation and recovery. In: Corporation I, editor. USA: International Business Machines Corporation; 2009.
[45] Drake A, Senger R, Deogun H, et al. A distributed critical-path timing monitor for a 65 nm high-performance microprocessor. In: IEEE international solid-state circuits conference digest of technical papers, 2007 (ISSCC 2007); 2007. p. 398–9.
[46] Jeppson KO, Svensson CM. Negative bias of MOS devices at high electric fields and degradation of MNOS devices. J Appl Phys 1977;48:2004–14.
[47] Rauch III SE. The statistics of NBTI-induced VT and beta mismatch shifts in pMOSFETs. IEEE Trans Dev Mater Reliab 2002;2:89–93.
[48] Pae S, Maiz J, Prasad C, et al. Effect of BTI degradation on transistor variability in advanced semiconductor technologies. IEEE Trans Dev Mater Reliab 2008;8:519–25.
[49] Agostinelli M, Pae S, Yang W, et al. Random charge effects for PMOS NBTI in ultra-small gate area devices. In: IEEE international reliability physics symposium; 2005. p. 529–32.
[50] Kang K, Park SP, Roy K, et al. Estimation of statistical variation in temporal NBTI degradation and its impact on lifetime circuit performance. In: IEEE/ACM international conference on computer-aided design; 2007. p. 730–4.
[51] Rauch SE. Review and reexamination of reliability effects related to NBTI-induced statistical variations. IEEE Trans Dev Mater Reliab 2007;7:524–30.
[52] Grasser T, Wagner PJ, Hehenberger P, et al. A rigorous study of measurement techniques for negative bias temperature instability. IEEE Trans Dev Mater Reliab 2008;8:526–35.
[53] Reisinger H, Vollertsen RP, Wagner PJ, et al. A study of NBTI and short-term threshold hysteresis of thin nitrided and thick non-nitrided oxides. IEEE Trans Dev Mater Reliab 2009;9:106–14.
[54] Zhigang J, Jian Fu Z, Mo Huai C, et al. An analysis of the NBTI-induced threshold voltage shift evaluated by different techniques. IEEE Trans Electron Dev 2009;56:1086–93.
[55] Ming-Fu L, Daming H, Chen S, et al. Understand NBTI mechanism by developing novel measurement techniques. IEEE Trans Dev Mater Reliab 2008;8:62–71.
[56] Keane J, Persaud D, Kim CH. An all-in-one silicon odometer for separately monitoring HCI, BTI, and TDDB. In: Symposium on VLSI circuits; 2009. p. 108–9.

[57] Keane J, Wang X, Persaud D, et al. An all-in-one silicon odometer for separately monitoring HCI, BTI, and TDDB. IEEE J Solid State Circ 2010;45:817–29.
[58] Kufluoglu H. MOSFET degradation due to negative bias temperature instability (NBTI) and hot carrier injection (HCI) and its implications for reliability aware VLSI design. PhD dissertation, Purdue University, West Lafayette (IN) USA; 2007.
[59] Mahapatra S, Saha D, Varghese D, et al. On the generation and recovery of interface traps in MOSFETs subjected to NBTI, FN, and HCI stress. IEEE Trans Electron Dev 2006;53(July):1583–92.
[60] Jiang W, Le JCH, Kopley T, et al. Assessing circuit-level hot-carrier reliability. In: IEEE international reliability physics symposium; 1998. p. 173–9.
[61] Quader K, Minami E, Huang W, et al. Hot-carrier reliability design guidelines for CMOS logic circuits. In: IEEE custom integrated circuits conference; 1993. p. 30.37.31–34.
[62] Tous S, Wu E, Suñé J. A compact model for oxide breakdown failure distribution in ultrathin oxides showing progressive breakdown. IEEE Electron Dev Lett 2008;29:949–51.
[63] Pang L, Nikolic B. Impact of layout on 90 nm CMOS process parameter fluctuations. In: IEEE symposium on VLSI circuits; 2006. p. 69–70.
[64] Agarwal K, Liu F, McDowell C, et al. A test structure for characterizing local device mismatches. In: IEEE symposium on VLSI circuits; 2006. p. 67–8.
[65] Keane J, Venkatraman S, Butzen P, et al. An array-based test circuit for fully automated gate dielectric breakdown characterization. In: IEEE custom integrated circuits conference; 2008. p. 121–4.
[66] Wolters D, Verwey J. Breakdown and wear-out phenomena in SiO_2 films. Instabilities in silicon devices, vol. 6. Amsterdam (The Netherlands): Elsevier; 1986.
[67] Röhner M, Kerber A, Kerber M. Voltage acceleration of TBD and its correlation to post breakdown conductivity of N- and P-channel MOSFETs. IEEE Int Reliab Phys Symp 2006:76–81.
[68] Wu E, Vayshenker A, Nowak E, et al. Experimental evidence of TBD power-law for voltage dependence of oxide breakdown in ultrathin gate oxides. IEEE Trans Electron Dev 2002;49(December):2244–53.
[69] DiMaria D, Stathis J. Non-Arrhenius temperature dependence of reliability in ultrathin silicon dielectric films. Appl Phys Lett 1999;74:1752.
[70] Kaczer B, Degraeve R, Pangon N, et al. The Influence of elevated temperature on degradation and lifetime prediction of thin silicon-dioxide films. IEEE Trans Electron Dev 2000;47:1514–21.
[71] Chopra K, Zhuo C, Blaauw D, et al. A Statistical approach for full-chip gate-oxide reliability analysis. IEEE/ACM Int Conf Comput Aided Des 2008:698–705.
[72] Anselin L. Local indicators of spatial association-LISA. Geograph Anal 1995;27:93–115.
[73] Hebeler F, Moran's I. 2007. <http://www.mathworks.com/matlabcentral/fileexchange/13663>.