An All-In-One Silicon Odometer for Separately Monitoring HCI, BTI, and TDDB

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***Abstract*—We present an on-chip reliability monitor capable of separating the aging effects of hot carrier injection (HCI), bias temperature instability (BTI), and time-dependent dielectric breakdown (TDDB) with high frequency resolution. This task is accomplished with a pair of modified ring oscillators (ROSCs) which are representative of standard CMOS circuits. We use a "backdrive" concept, in which one ROSC drives the voltage transitions in both structures during stress, such that the driving oscillator ages due to both BTI and HCI, while the other suffers from only BTI. In addition, long term or high voltage experiments facilitate TDDB measurements in both oscillators. Sub-μs measurements are controlled by on-chip logic in order to avoid excessive unwanted BTI recovery during stress interruptions. Sub-ps frequency resolution is achieved during these short measurements using a beat frequency detection system, and we automate the experiments through a simple digital interface. Measurement results are presented from a 65 nm test chip over a range of stress conditions.**

***Index Terms*—Aging, bias temperature instability, circuit reliability, dielectric breakdown, digital measurements, hot carriers.**

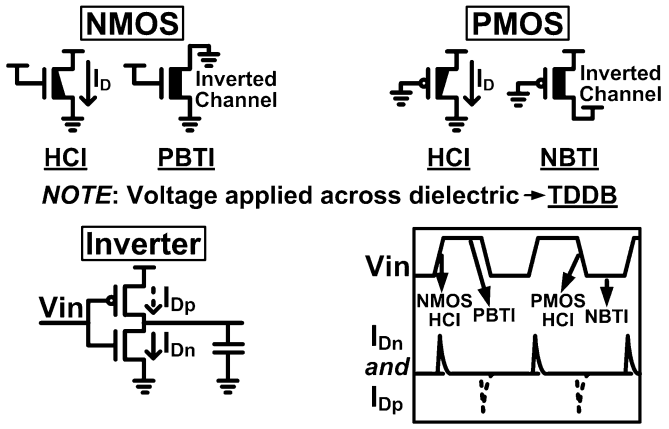

Fig. 1. HCI, BTI, and TDDB stress illustrated for NMOS and PMOS transistors, as well as for an inverter during standard operation.

I. Introduction

THE parametric shifts or circuit failures caused by hot carrier injection (HCI), bias temperature instability (BTI), and time-dependent dielectric breakdown (TDDB) have become more severe with shrinking device sizes and voltage margins. These mechanisms must be studied in order to develop accurate reliability models, which are used to design robust circuits. Another option for addressing aging effects is to use on-chip reliability monitors that can trigger real-time adjustments to compensate for lost performance or device failures. The need for efficient technology characterization and aging compensation is exacerbated by the rapid introduction of process improvements, such as high-k/metal gate stacks and stressed silicon. However, addressing many separate reliability mechanisms is a time consuming and expensive task. Any cost-effective methods developed to expedite this process would be highly valuable.

As shown in Fig. 1, CMOS devices suffer from HCI, BTI, and TDDB stress under standard digital operating conditions. HCI has become less prominent with the reduction of operating voltages, but remains a serious concern due to the large local electric fields in scaled devices. Hot carriers (i.e., those with high kinetic energy) accelerated toward the drain by a lateral electric field across the channel lead to secondary carriers generated through impact ionization [Fig. 2(a)]. Either the primary or secondary carriers can gain enough energy to be injected into the gate stack. This creates traps at the silicon substrate/gate dielectric interface, as well as dielectric bulk traps, and hence degrades device characteristics such as the threshold voltage ($\mathrm{V_{th}}$). These "traps" are electrically active defects that capture carriers at energy levels within the bandgap.

Negative bias temperature instability (NBTI) in PMOS transistors is often cited as the primary reliability concern in modern processes, especially after the introduction of nitrogen into gate stacks, which reduces boron penetration and gate leakage, but leads to worse NBTI degradation [1]. This mechanism is characterized by a positive shift in the absolute value of the PMOS $\mathrm{V_{th}}$, which occurs when a device is biased in strong inversion, but with a small, or no, lateral electric field (i.e., $\mathrm{V_{DS}} \approx 0$) V. The $\mathrm{V_{th}}$ shift is generally attributed to hole trapping in the dielectric bulk, and/or to the breaking of Si-H bonds at the gate dielectric interface by holes in the inversion layer, which generates positively charged interface traps [Fig. 2(c)] [1], [2]. When a stressed device is turned off, it immediately enters the "recovery" phase, where trapped holes are released, and/or the freed hydrogen species diffuse back towards the substrate/dielectric interface to anneal the broken Si-H bonds, thereby reducing the absolute value of the $\mathrm{V_{th}}$ [Fig. 2(d)]. Positive bias temperature instability (PBTI) in NMOS transistors was not critical in silicon dioxide

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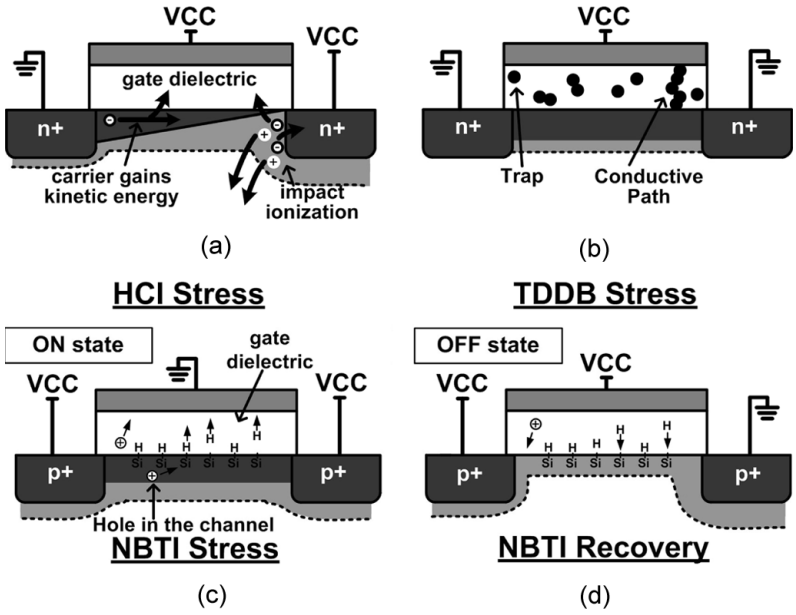


Fig. 2. Transistor cross sections illustrating (a) HCI, (b) TDDB, (c) NBTI stress, and (d) NBTI recovery.

dielectrics (such as those used in the current test circuit implementation), but is now contributing to the aging of high-k gate stacks [3].

Finally, any voltage drop across the gate stack can cause the creation of traps within the dielectric. These defects may eventually join together and form a conductive path through the stack in a process known as TDDB, or oxide breakdown [Fig. 2(b)]. Breakdown has been a cause for increasing concern as gate dielectric thicknesses are scaled down to the one nanometer range, because a smaller critical density of traps is needed to form a conducting path through these thin layers, and stronger electric fields are formed across gate insulators when voltages are not reduced as aggressively as device dimensions. The scaling of the physical dimensions of gate stacks can now be slowed or reversed with the introduction of high-k dielectrics, but TDDB remains a critical aging mechanism in those materials, and is currently being studied by device physicists [3], [4].

Each of these three aging mechanisms has different sensitivities to operating conditions and process changes, and can be more critical in certain circuit topologies. Therefore, they should each be examined separately. Much of the device aging data gathered for process characterization is obtained through device probing experiments. The equipment used in those tests can be expensive, and testing each device individually leads to long experiment times. Several on-chip systems have recently been proposed to monitor circuit aging [5]–[11]. However, no method has been presented to isolate the effects of these three major reliability mechanisms in a single test structure.

In this work, we accomplish that task with a pair of ring oscillators (ROSCs) which are representative of standard circuits [5]. We use a "backdrive" concept in which one ROSC drives the transitions in both structures during stress, such that the driving oscillator ages due to both BTI and HCI, while the other suffers from only BTI. The latter ROSC is gated off from the supplies during stress so that no current is driven through the channels of its transistors, and therefore the carriers cannot become "hot." In addition, long term or high voltage experiments facilitate TDDB measurements. It is now well known that BTI degradation recovers on a sub-μs timescale after the removal of stress conditions [2]. Therefore, we use a beat frequency detection method to take sub-μs measurements and avoid unwanted device recovery during stress interruptions. Sub-ps frequency measurement resolution is achieved for finely-tuned HCI and BTI readings, and experiments are automated through a simple digital interface. This design allows us to test the frequency, temperature, and voltage dependencies of the stress mechanisms. In addition, we can monitor both sustained stress and recovery characteristics, and can observe the effects of increased load capacitance on the frequency shift induced by aging.

II. Prior Work in On-Chip Reliability Monitors

As stated in the previous section, much of the device aging data gathered for process characterization is obtained through individual device probing experiments. However, probing stations can be expensive, and they have other drawbacks such as limited timing resolution for minimizing stress interruptions when recording measurements. In order to resolve these issues, and to develop real-time aging monitors for compensation schemes, several on-chip systems have recently been proposed to measure device aging.

Kim *et al.* presented the first version of the Silicon Odometer, which is a digital reliability monitor for high resolution frequency shift measurements [6]. This technique measures the beat frequency between two ROSCs, where one is stressed and the other is unstressed to maintain a fresh reference. They achieved 50X higher delay sensing resolution than prior schemes in the early stages of degradation. This concept is utilized in the present work, and will be explored further in Section III. However, in Kim's work, stress was applied by simply raising the supply of the standard inverter-based stressed ROSC, so aging was due to a combination of the mechanisms discussed in Section I. Our new Odometer implementation

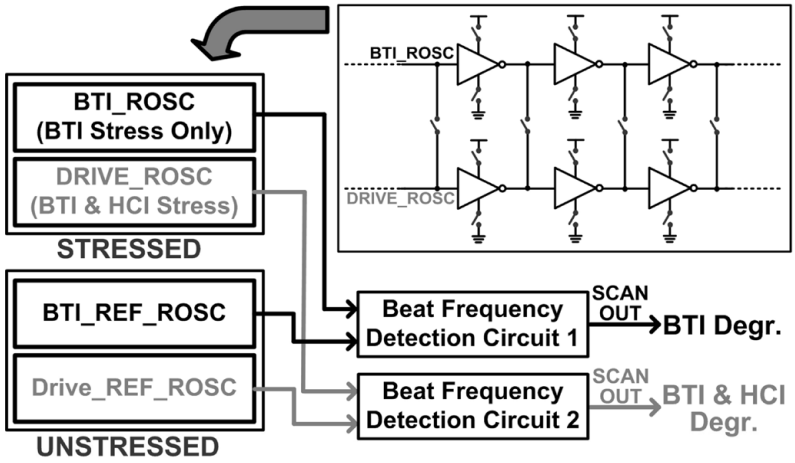


Fig. 3. Proposed system for separately monitoring BTI- and HCI-induced frequency degradation. TDDB degradation is also observed with long-term or high voltage stress experiments.

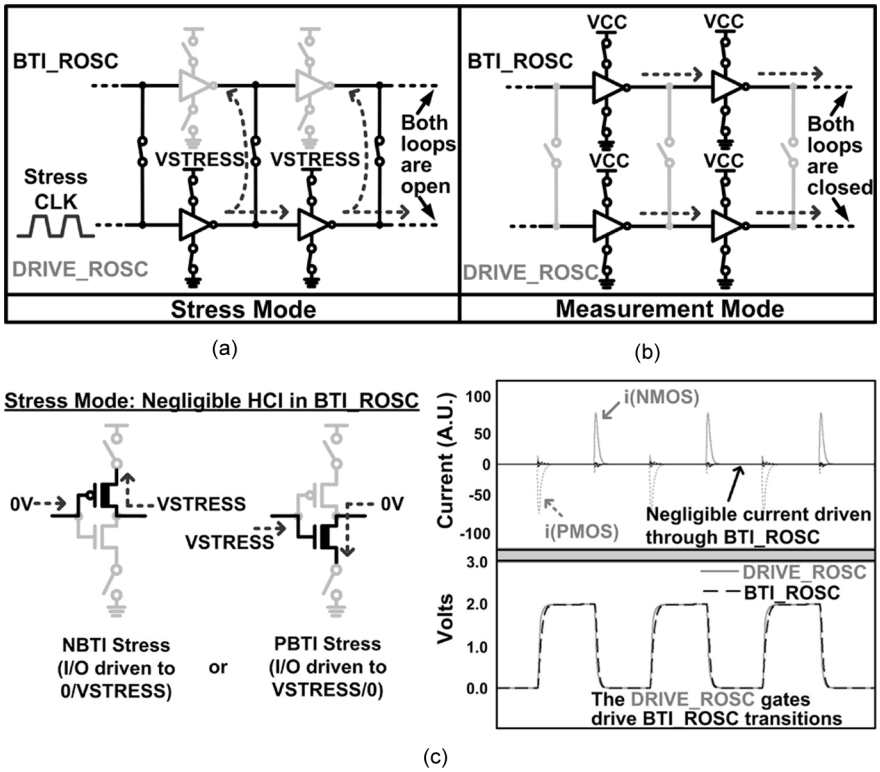


Fig. 4. ROSC configuration during (a) stress and (b) measurement modes. (c) The BTI_ROSC transistors suffer the same amount of BTI as the DRIVE_ROSC transistors during stress, but with negligible HCI degradation, since very little current is driven through the channels of the devices under test the former structure.

separates the effects of the different aging mechanisms, along with other improvements discussed later.

Karl *et al.* proposed two separate compact circuits for monitoring NBTI and TDDB, with the goal of facilitating real-time characterization [7]. First they measured the frequency shift of a ROSC with a PMOS header that is placed under NBTI stress, and then biased in subthreshold during measurements for high ΔV_{th} sensitivity. Their work relies on a complex mathematical model to map temperature and V_{th} variations to the measured ROSC frequencies after extensive calibration. Next, the TDDB aging results were provided in the form of a frequency shift of a Schmitt trigger oscillator which is modified by the increasing gate leakage through a pair of stressed PMOS transistors.

We previously presented an on-chip NBTI degradation sensor using a delay-locked loop (DLL), in which the increase in PMOS V_{th} due to NBTI stress is translated into a control voltage shift in the DLL for high sensing gain [8]. Measurements from a test chip fabricated in a 130 nm bulk CMOS process showed an average gain of 10X, with measurement times in tens of microseconds possible for minimal unwanted V_{th} recovery. However, it is preferable to avoid the use of analog systems such as DLLs for simplicity.

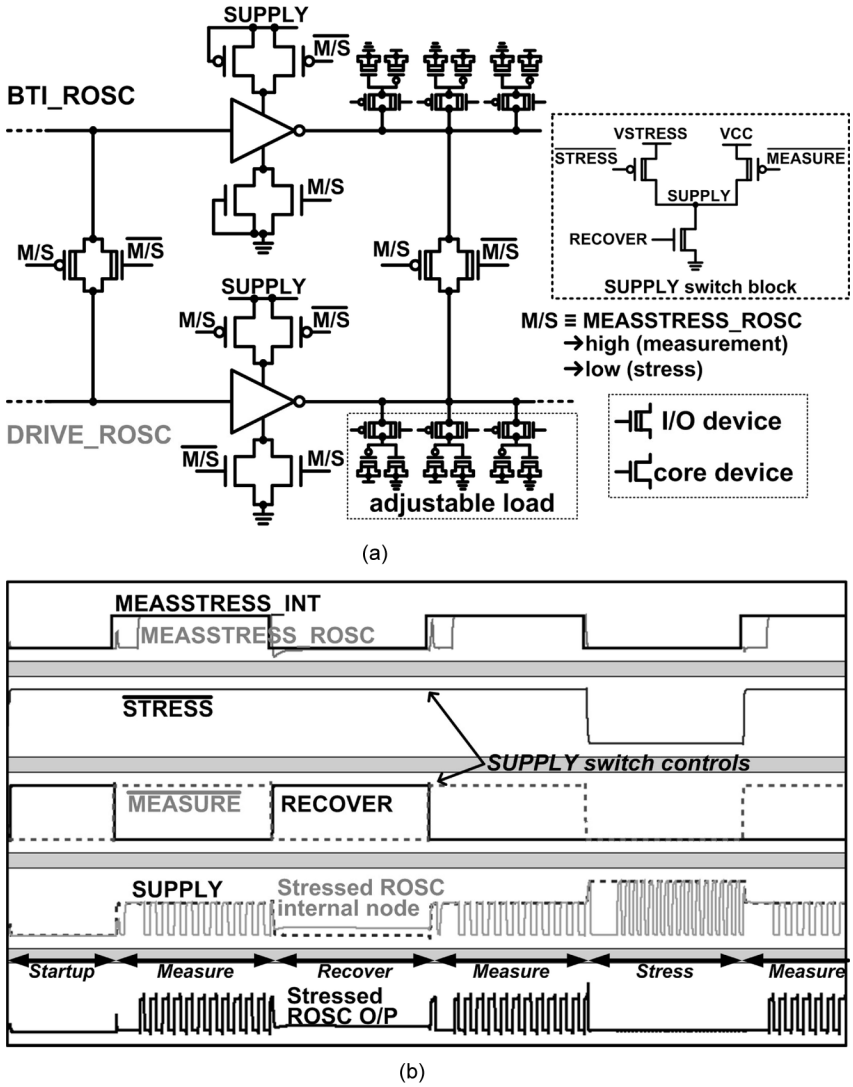


Fig. 5. (a) Schematic of one stage of the paired ROSCs. (b) Simulation waveforms from a stressed ROSC during measurement, stress, and recovery periods. Note that any initial lone pulses seen at the stressed ROSC output are rejected by the beat frequency detection logic.

We also implemented an array-based test circuit for efficiently characterizing TDDB, where many devices are stressed in parallel, and experiments are automated through a digital interface [9]. That design is highly beneficial when studying this statistical process, where up to thousands of samples are needed to create an accurate time-to-breakdown Weibull distribution. The goal of our breakdown measurements in the present work is not to provide statistical data, but to show the effects of breakdowns within a ROSC, and to combine this with BTI and HCI data from a single test circuit.

While several other designs have been proposed [10], [11], none have presented a method to monitor each of the three main front end of line reliability mechanisms with one test circuit. The All-In-One Silicon Odometer efficiently achieves that goal using the techniques described in the next section. The benefits of this new design, include its simple all-digital structure and test interface, as well as sub-μs measurement time for minimal unwanted BTI recovery combined with sub-ps frequency resolution.

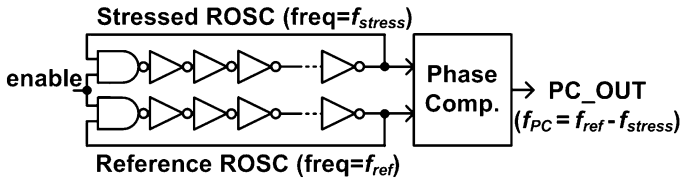


Fig. 6. Beat frequency detection between a stressed and an unstressed ROSC. This system achieves sub-ps frequency shift resolution for the stressed ROSC, with sub- μs measurement times [6]. (More system details covered later in Fig. 11(a)).

III. All-In-One Odometer Circuit Techniques

A block diagram of our proposed reliability monitor for separating the effects of HCI and BTI is shown in Fig. 3. This circuit contains four ROSCs in total: two stressed, and two unstressed to maintain fresh reference points. Each of the stressed oscillators is paired with its identical, fresh reference during measurements, and its frequency degradation is monitored with the Silicon Odometer beat frequency detection circuit [6].

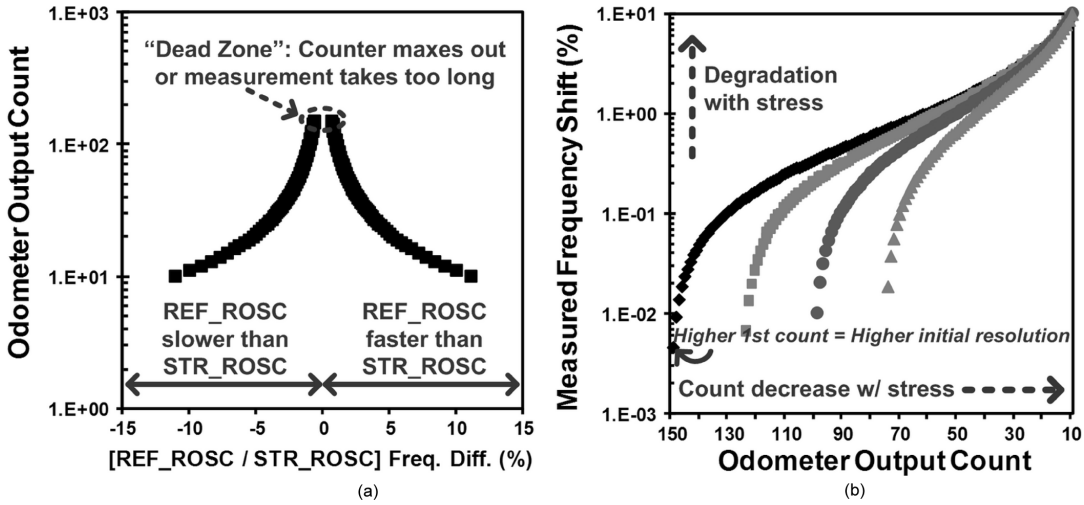


Fig. 7. (a) Silicon Odometer output count vs. the frequency difference between the reference and stressed ROSCs. When the two frequencies become extremely close, a high output count is observed, which requires a larger counter and longer measurement time. (b) Output count vs. frequency shift during a stress experiment. Curves are shown for varied initial counts, where a higher count corresponds to a smaller frequency difference between the two ROSCs, as was shown in part (a) of this figure.

A. Illustration of the Backdrive Concept

Fig. 4 presents the pair of stressed ROSCs in both (a) stress and (b) measurement modes. (Note that all body terminals are connected to their respective supply levels.) During stress, the BTI_ROSC stages are gated off from the power supplies, while the DRIVE_ROSC maintains a standard inverter configuration with the supply set at VSTRESS. Both ROSC loops are opened, and the input of the DRIVE_ROSC is driven by a stress clock generated by an on-chip voltage controlled oscillator (VCO) whose output is level-shifted up to VSTRESS. The switches between these two ROSCS are closed so the DRIVE_ROSC can drive the internal node transitions for both structures.

Simulated voltage and current waveforms are shown in Fig. 4(c). The internal nodes of the BTI_ROSC switch between the supply level (VSTRESS) and 0 V, as would be the case in standard operation. However, the peak drain current though the "on" devices in this structure is only 3–5% of that in the DRIVE_ROSC, since their sources are gated off from the supplies. Note that the sources of these "on" devices in the stressed BTI_ROSC are held at their respective supply levels due to the backdriving action of the DRIVE_ROSC. Therefore, the BTI_ROSC will age due only to BTI stress, while the DRIVE_ROSC suffers both BTI and HCI. We can extract the contribution of HCI to the latter ROSC's frequency degradation with the equation $\mathrm{HCI_{DEG}} = \mathrm{DRIVE_{DEG}} - \mathrm{BTI_{DEG}}$, where DEG stands for degradation. During measurement periods, both ROSCs are connected to the digital logic power supply (VCC) and the switches between them are opened, so they each operate independently in a standard closed-loop configuration.

B. ROSC Design Details for Backdrive

A detailed schematic of one stage of the paired ROSCs is shown in Fig. 5(a). The thick oxide I/O devices should not age appreciably during stress experiments aimed at the thin oxide core transistors. All core devices are either stressed devices under test (DUTs), or have no voltage drops across any pair of terminals during stress, so they will not age. The header and footer transistors in each inverter pin the source nodes of those gates to the supply levels when closed. The M/S signal here is used to start and end measurement periods. This signal is timed and driven by the on-chip finite state machine (FSM) after the external MEASSTRESS_EXT signal is asserted.

Both ROSCs contain three levels of adjustable fanout which allows us to test the effects of additional load capacitance on aging. Extracted simulations show that turning on each additional stage of fanout increases the transition times by an average of roughly 22%. It is expected that these changes will adjust the balance between HCI and NBTI stress during normal

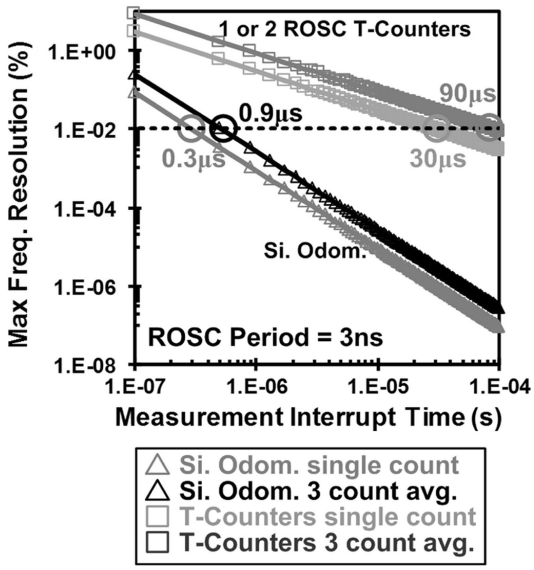


Fig. 8. Maximum frequency measurement resolution versus the total stress interruption time for measurements (note: lower frequency shift measured = higher resolution). A standard ROSC period counting system requires a 100X longer measurement time than the Odometer to achieve a measurement resolution of 0.01%.

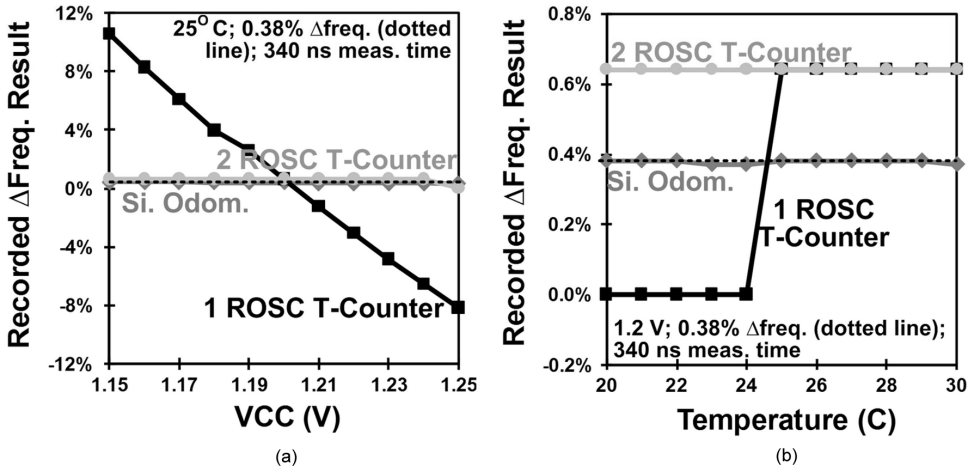


Fig. 9. Simulated effects of (a) voltage, and (b) temperature variations on the Silicon Odometer, and both 1 and 2 ROSC period counter (T-Counter) systems. The values shown here are the results recorded by each system when the actual stress-induced frequency shift is 0.38%. We assume both ROSCs in the differential systems see the same variations since they are adjacent and identical in the layout. The larger rounding errors seen in the T-Counter measurements at small percentages are a result of their lower frequency resolution with short measurement times.

voltage switching operation, as longer input and output transition times result in an increasing number of hot carriers [12], [13].

Fig. 5(b) contains waveforms from a stressed ROSC during measurement, stress, and recovery periods. After MEASSTRESS_INT is driven high by the FSM, there is a short delay before MEASSTRESS_ROSC goes high, which then causes the tapped output from the stressed ROSC to be connected to the input of the Odometer measurement system. This delay allows the SUPPLY node to settle after being switched to the standard operating supply of VCC, and having the ROSC loop closed. An external control signal is set high any time we wish to enter a recovery mode between measurements, but will not take effect until the end of the subsequent measurement period.

C. Silicon Odometer Background and Theory

The Silicon Odometer measures frequency changes in the stressed ROSCs with the concept illustrated in Fig. 6 (further details in [6]). During the short measurement periods, a phase comparator uses a fresh reference ROSC to sample the output of an identical stressed ROSC. The output signal of this phase comparator exhibits the beat frequency: $f_{\mathrm{PC}} = f_{\mathrm{ref}} - f_{\mathrm{stress}}$. A counter is used to measure the beat frequency by counting the number of reference ROSC periods during one period of the phase comparator output signal (see Fig. 11(a), to be covered later). This count is recorded after each stress period to calculate the shift down in the stressed ROSC frequency.

The details of the beat frequency calculation can be found in the previous publication [6], but are summarized here for convenience. If the initial frequency of the reference ROSC is called f_{ref}, that of the fresh ROSC to be stressed is f_{stress}, and the initial Odometer output count is N_1, then assuming f_{ref} is higher than f_{stress}, we have

$$1/f_{\mathrm{ref}} \cdot N_1 = 1/f_{\mathrm{stress}} \cdot (N_1 - 1)\,. \tag{1}$$

The $(N_1 - 1)$ term arises from the fact that the stressed ROSC with the lower frequency, f_{stress}, will take one less period to cycle back to the same point in the reference ROSC period while both are oscillating. After a stress period ends, f_{ref} will remain unchanged, but f_{stress} will be decreased due to aging, and we call the new frequency f'_{stress} (later we will show that these calculations result in very small errors even if f_{ref} is modified by temporal variations along with f_{stress}). We also have a new output count (N_2), so the resulting equation is

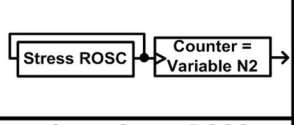
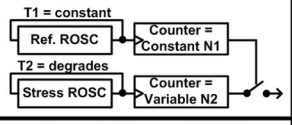
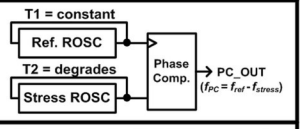
$$1/f_{\mathrm{ref}} \cdot N_2 = 1/f'_{\mathrm{stress}} \cdot (N_2 - 1)\,. \tag{2}$$

Using these two equations, we can calculate the frequency shift during stress as follows:

$$\frac{f'_{\mathrm{stress}}}{f_{\mathrm{stress}}} - 1 = \frac{N_1 \cdot (N_2 - 1)}{N_2 \cdot (N_1 - 1)} - 1 = \frac{(N_2 - N_1)}{N_2 \cdot (N_1 - 1)}. \tag{3}$$

Those simple calculations show that if f_{ref} is only slightly higher than f_{stress}, the output count is high. For example, the count is 100 for a 1% difference. This slight difference can be ensured with trimming capacitors and calibration. The subsequent small decreases in f_{stress} due to aging cause a large change in this count. For instance, a 2% difference between the ROSC frequencies gives a count of 50, so a 1% shift to that point is translated into a decreased count of 50. Therefore, with high frequency ROSCs, the beat frequency detection system achieves sub-ps frequency shift measurement resolution.

The Odometer output count relationship with the difference between the reference ROSC (REF_ROSC) and stressed ROSC (STR_ROSC) frequencies is illustrated in Fig. 7(a). This figure shows that the Odometer operates correctly with a reference ROSC frequency that is either slower or faster than the stressed ROSC. In the former case, the output count will increase with stress, while it decreases in the latter. A slower reference frequency is accounted for in (1) through (3) by changing the $(N_{\#} - 1)$ terms to $(N_{\#} + 1)$, because the faster stressed ROSC in this case goes through *one more* period than the slow reference during the beat frequency measurement, rather than *one less*. Additionally, it is possible for the reference frequency to transition from being slower than to faster than the stressed

System	1 ROSC T-Counter	2 ROSC T-Counter	Silicon Odometer
Block Diagram			
Function	Count Stress ROSC periods during externally controlled meas. time	Count Stress ROSC periods during N1 periods of Ref. ROSC	Count Ref. ROSC periods during one period of PC_OUT
Features	Simple; compact	Simple; immune to common mode variations	High resolution w/ short meas. time; immune to common mode variations
Issues	Voltage and temp. varations; meas. time vs. resolution tradeoff; requires absolute timing reference (e.g. oscilloscope)	Meas. time vs. resolution tradeoff	Requires extra circuits (e.g., Phase Comp., edge detector, etc...)
Meas. time for 1% max resolution *	30 µs	30 µs	0.3 µs
Meas. error wrt. common mode variations **	+10.18% / -8.57%	+0.26% / -0.38%	+0.06% / -0.07%

*ROSC period = 3 ns ** simulated with +/- 4% ΔVCC; 0.38% stress shift; 340 ns measurement time; error = (measured %) – (0.38%)

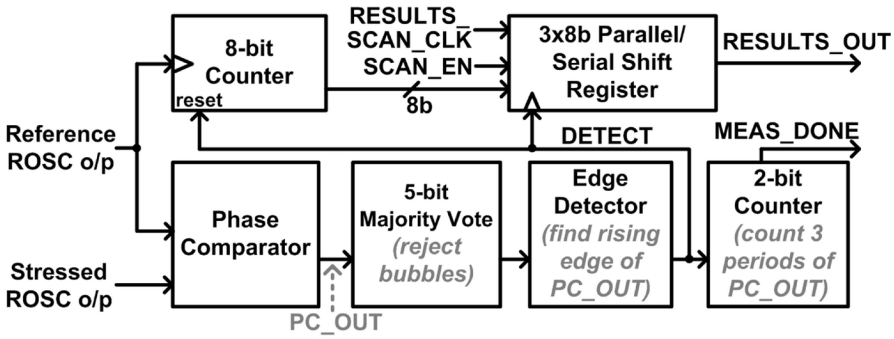
Fig. 10. Comparison of simple ROSC period counting systems with the Silicon Odometer.

ROSC, but this involves moving through a "dead zone" where the output count will either equal the counter max value, or if the counter is large enough, the measurement time will become excessively long as the difference between the two ROSC frequencies becomes extremely small.

We chose to start our experiments with a reference frequency that is slightly faster than the stressed ROSC frequency, so that we obtained a monotonic decrease in the output counts with stress. This allowed us to maximize the frequency measurement resolution in the early phases of stress, and to avoid the dead zone. Fig. 7(b) shows measurement result characteristics with monotonic count decreases, and four different initial counts. Note again that a smaller difference between the two ROSC periods leads to a higher initial count, and therefore a higher initial frequency resolution, while lengthening the measurement time. We achieved maximal starting counts of ~ 125 in our hardware measurements, which corresponds to initial frequency shift measurements ranging down to 0.0065%. The resolution decreases with time, but we are primarily concerned with the small initial degradation steps that can be obtained with stress that is closer to real operating conditions. It has been shown that stress at excessively high voltages, for example, can lead to unrealistic degradation characteristics that are not useful for predicting device lifetimes under standard operating conditions [14], [15].

The plot in Fig. 8 shows the theoretical maximum frequency measurement resolution for three measurement setups during a fixed time. In the "1 ROSC T-Counter" system (where T stands for period), a single ROSC's degradation is recorded with a single period counter during an externally controlled measurement time. The "2 ROSC T-Counter" measures the degradation in one stressed ROSC by counting the number of periods it cycles through while a set number of periods in a fresh reference ROSC are counted (see Fig. 10). Since the resolution of these period counters is simply the measurement time divided by the ROSC period, while that of the Odometer can be derived from (3), we see that the Odometer reaches a maximum resolution of 0.01% within only 0.3 μs in the ideal cause with a single measurement recorded, while the other systems require 100X more time. A large improvement is still seen when three counts are recorded during each Odometer measurement period for averaging, or to eliminate unpredictable initial counts (see Section III-D). The longer measurement times in the standard period counter systems would result in unacceptable unwanted BTI recovery.

In addition to the high frequency resolution, the Odometer benefits from a high immunity to voltage or temperature variations due to its differential nature. Given that the reference and stressed ROSCs are identical structures that are laid out next to each other, we assume that both will see essentially identical temporal variations, so their frequencies should be affected by roughly the same amount. The simulation results shown in Fig. 9 illustrate this noise immunity, and compare the Odometer results with those of the ROSC T-Counter setups. In these simulations, the stressed ROSC started out 0.64% slower than the reference when measured at nominal VCC (1.2 V) and temperature (25 °C), and the former structure is slowed by 0.38% due to aging (in the 1 ROSC T-Counter we only consider the 0.38% shift since there is no reference ROSC). However, if this post-stress measurement takes place under a different temperature or voltage condition, it will lead to some deviation from 0.38% in the measured value. Fig. 9 presents the simulated results gathered in this situation, and shows a clear benefit for the differential Odometer system. Also note that since we limited the measurement time to the ideal required by the Odometer system, the T-Counters suffer from



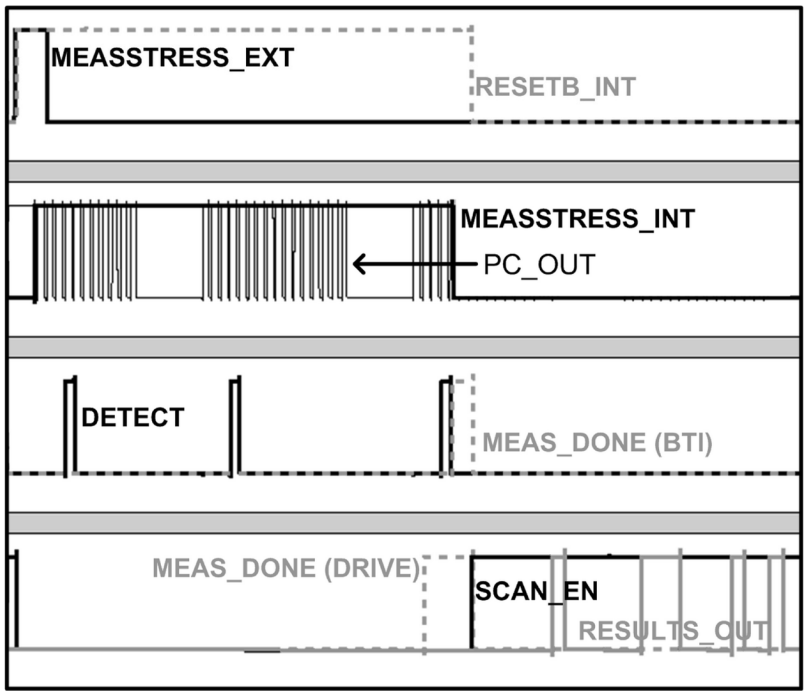


Fig. 11. (a) Block diagram of the improved beat frequency detection circuit. (b) Simulation results illustrating the operation of this system.

low frequency resolution, which results in further rounding errors.

Fig. 10 compares the three frequency measurement systems that have been discussed. While the Odometer requires additional circuits for the beat frequency detection, it achieves a significantly higher frequency measurement resolution in a shorter measurement time, and is immune to common mode environmental variations.

D. Improved Silicon Odometer Beat Frequency Detection Circuit

In this work, we improved the beat frequency detection system by including logic which sends the circuit back into stress after three results are recorded, in order to achieve measurement times of ≤ 1 μs. The completion of a measurement period is flagged by the MEAS_DONE signal [Fig. 11(a)] when the three rising edges from the phase comparator are counted, meaning three 8b count results have been recorded. In this automated scheme, the first two counts are generally smaller than the true result due to the unpredictable starting location of the measurement at some mid-point in the phase comparator period, so they are discarded. We verify that the third count is correct during calibration by using an externally controlled longer measurement period in which the initial smaller counts are overwritten by subsequent results. In this case, all counts should be roughly identical, and equal to the third result we record during the shorter automated measurements. Moving on, the MEAS_DONE flag is sent to the FSM, which restarts stress after it is asserted by both Odometers. Using on-chip logic to control this timing allows us to avoid generating very short, accurate measurement pulses externally.

The majority voting circuit [Fig. 11(a)] rejects a lone '1' signal in a series of '0's, or vice versa. These "bubbles" can be caused by temporal variations. The edge detector is used to find the beginning of each period of the phase comparator. Its output, DETECT, is used to sample the counter output, and then to reset the counter for a new period.

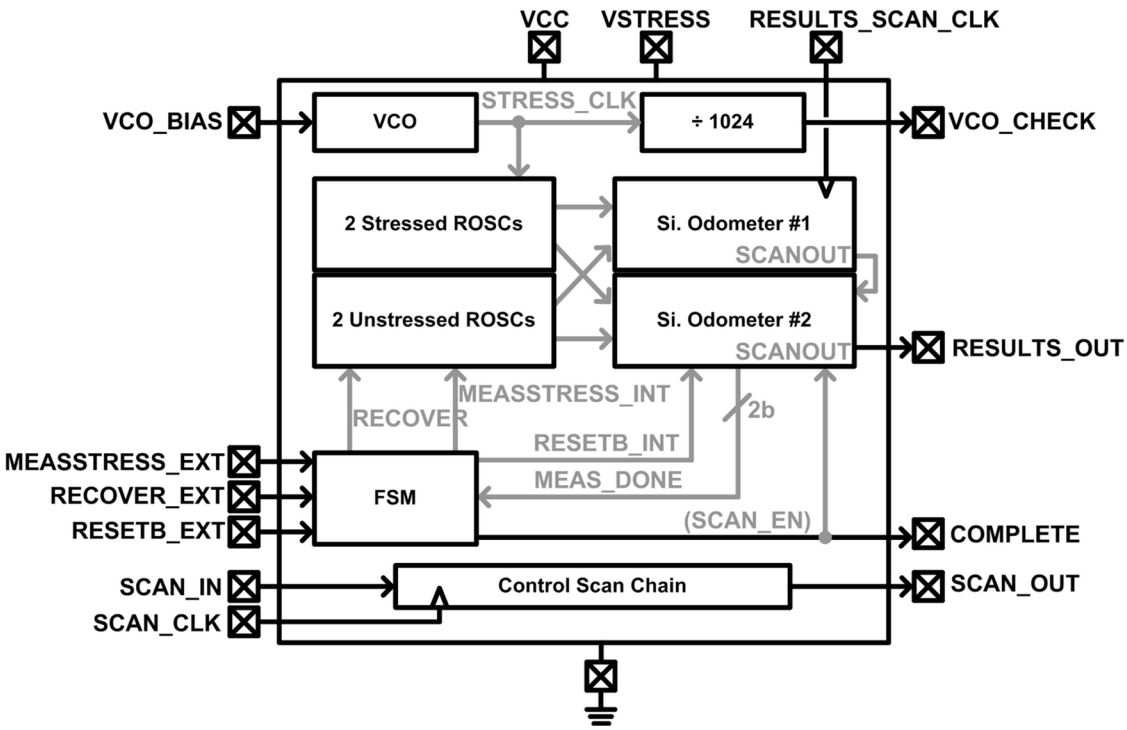
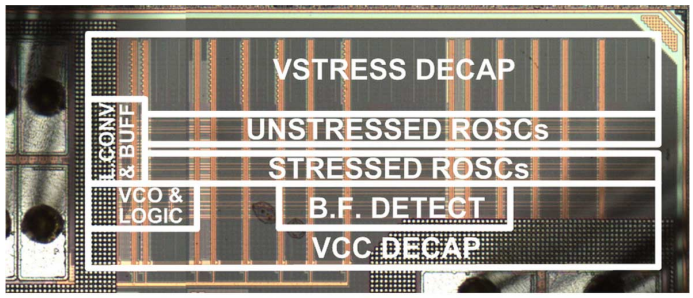


Fig. 12. High level pin I/O diagram with major internal signal routing.

Fig. 11(b) contains simulation waveforms illustrating the operation of this system. After the external MEASSTRESS signal is asserted, its internal counterpart is driven high by the FSM, which connects switching signals from the ROSCs to the phase comparator, and starts the measurement. After three high PC_OUT periods, we see the MEAS_DONE signal go high. As noted, these waves are from the Odometer monitoring the BTI_ROSC. The bottom line of this figure shows that the MEAS_DONE signal in the Odometer system monitoring the DRIVE_ROSC has already gone high. The combination of these two signals causes the FSM to end the measurement period and switch the parallel/serial shift registers to scan mode. An external clock is then used to scan out the results. The registers will be put back into parallel mode when MEASSTRESS_EXT is next asserted.

E. Test Setup and Procedure

A high-level pin diagram of the All-In-One Odometer system is shown in Fig. 12. VCO_BIAS is used to set the STRESS_CLK frequency, and MEASSTRESS_EXT is pulsed to initiate each measurement period. RECOVER_EXT is asserted to send the stressed ROSCs into recovery mode after the *next* measurement period. RESETB_EXT immediately sends the circuit into its initial startup state, where the SUPPLY node in the ROSCs is dropped to 0 V, and the FSM is left waiting for the next MEASSTRESS_EXT pulse. The RESULTS_SCAN_CLK signal is pulsed 48 times after each measurement is completed, which is indicated by a rising edge on COMPLETE. The results registers in the two Odometers are connected in series, so 48 pulses are required for the two sets of three 8b registers. Finally, VCO_CHECK is used to monitor the frequency of the VCO, and RESULTS_OUT is the scan-out port for both Odometer results.



Technology	65 nm, 7M
Logic/IO Supplies	1.2 V / 2.5 V
Active Area	38,040 μm^2
Total Area	(214.22 X 551.43) μm^2
ΔT Resolution	< 1 ps
Measure Interrupt	< 1 μs

Fig. 13. Test chip microphotograph and summary of characteristics.

IV. All-In-One Odometer Test Chip Measurements

A 214×551 μm^2 test circuit was implemented in a 65 nm bulk CMOS process for concept verification. A die photo and a summary of test chip characteristics are presented in Fig. 13. Measurements were automated with LabVIEW™ software through a National Instruments data acquisition board. Trimming capacitors were used in each 33-stage ROSC to ensure that the frequencies of the stressed structures began slightly slower than the reference frequencies (see Section III-C). Trimming was also utilized to push apart the oscillating frequencies of the two sets of paired ROSCs to prevent injection locking. The DUTs were 1.5 μm/60 nm NMOS and 3 μm/60 nm PMOS transistors in the

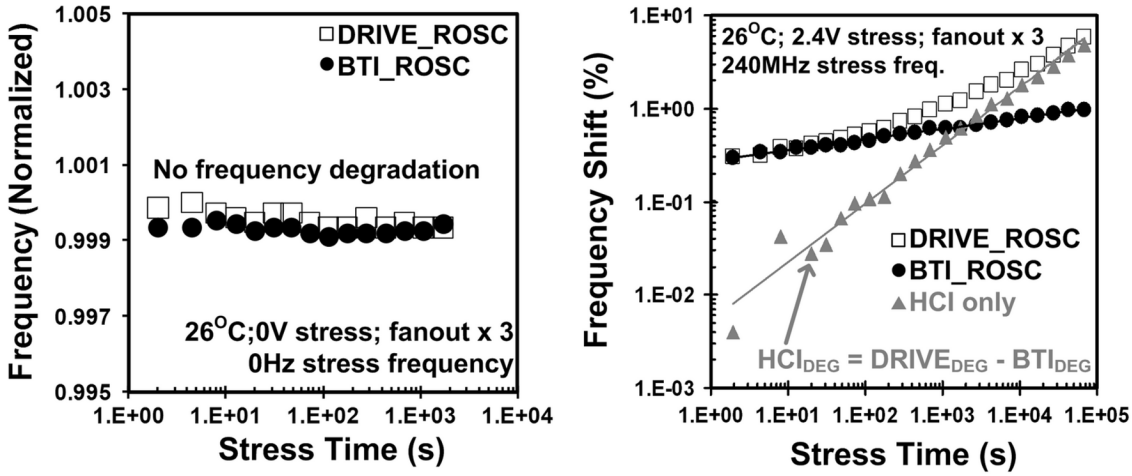


Fig. 14. (a) Results from an experiment in which the RECOVER_EXT signal was asserted to prevent the DUTs from being stressed. As expected, no frequency shifts are observed, so shifts in subsequent stress experiments can be attributed to device aging rather than any undesired circuit effects. (b) Example measured results with AC stress conditions.

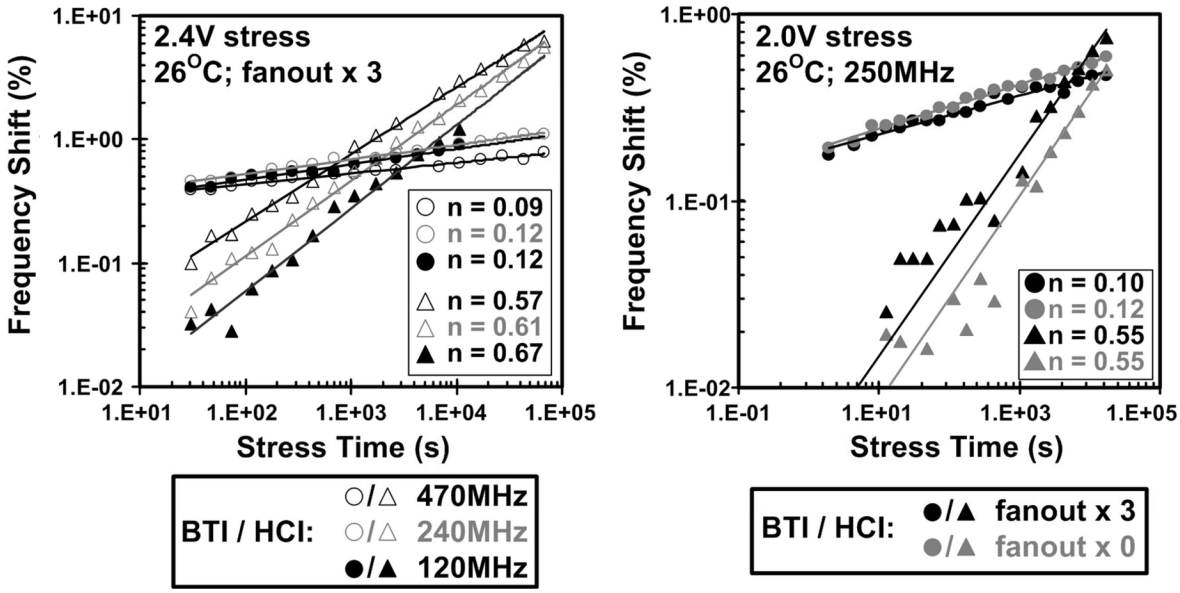


Fig. 15. Measured frequency degradation results for (a) three stress frequencies and (b) increased load capacitance, with power law exponents (n).

inverter stages of the stressed ROSCs. All automated measurement times were under 1 μs, but varied according to the exact beat frequency count results, as shown in Fig. 7.

A. Circuit Verification Measurements

We first we checked the result of a 0 V stress experiment, meaning the SUPPLY node of both normally stressed ROSCs was dropped to 0 V between measurements periods by keeping the RECOVER_EXT signal high, so no aging should have taken place. The results in Fig. 14(a) confirm this outcome, so we can be confident that frequency shifts shown in later results are not due to aging elsewhere in this system or other circuit effects.

Fig. 14(b) presents example measurement results for both ROSCs under 2.4 V stress, as well as the calculated degradation due to HCI $(\mathrm{HCI_{DEG}})$. As expected, both BTI and HCI degradation follow a power law behavior, although the latter is seen to saturate at long stress times. This can be explained by the finite number of bonds to be broken at the Si–SiO_2 interface and/or the self-limiting nature of HCI, where the degraded drain current produces fewer hot carriers. The power law exponent for BTI in this case was 0.12, while that of HCI was 0.63 in the range fitted on this plot. The larger value for HCI is expected, and one possible reason for this is an increasing contribution of broken Si–O bonds at the oxide interface during HCI stressing, rather than Si–H bonds [16], [17].

B. BTI and HCI Stress Measurements

Fig. 15(a) illustrates the impact of frequency on BTI and HCI. These results verify that BTI is at most weakly dependent on frequency, while HCI degrades with increased switching activity. More switching leads to an increase in current driven through the DUTs' channels, meaning more hot carriers are present. A decrease in the power law exponent of HCI was observed at higher frequencies, which is apparently due to the quick saturation of degradation in this case. In Fig. 15(b) we see that increased load capacitance, which causes longer transition times,

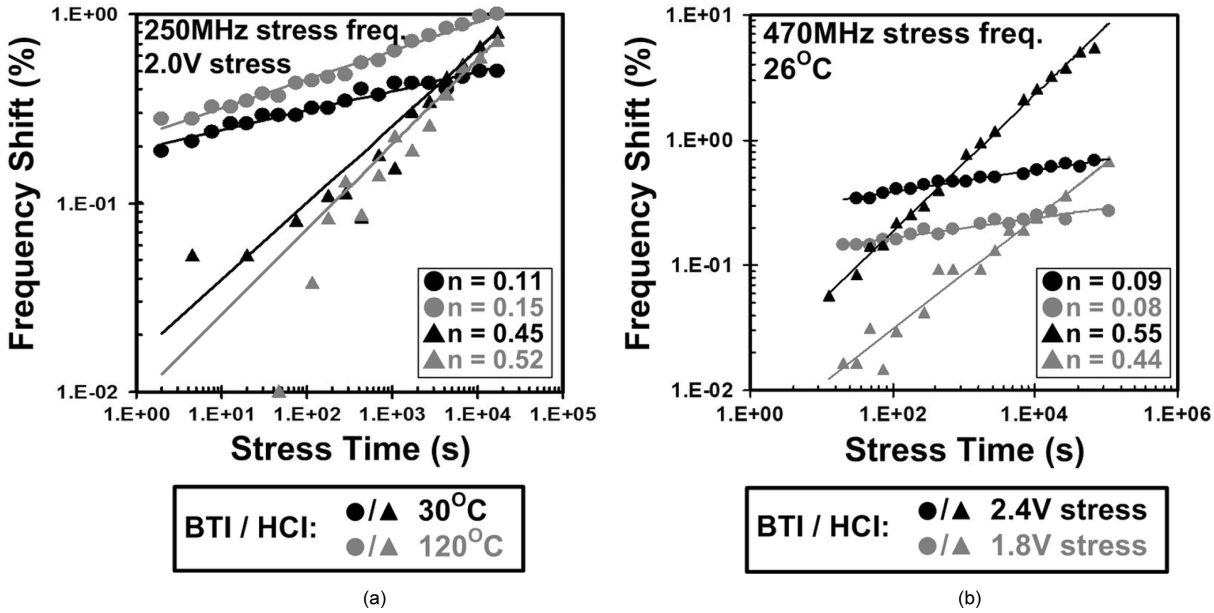


Fig. 16. Effect of (a) stress temperature and (b) stress voltage.

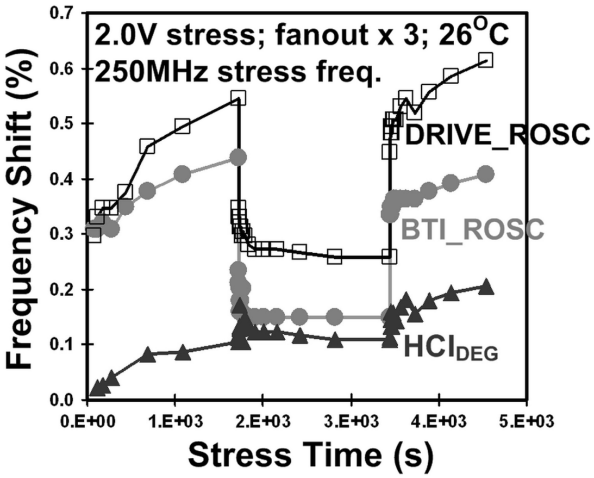


Fig. 17. Periodic stress/recovery characteristics. The BTI frequency curve shows a common sawtooth characteristic, while the HCI curve does not recover when stress conditions are removed.

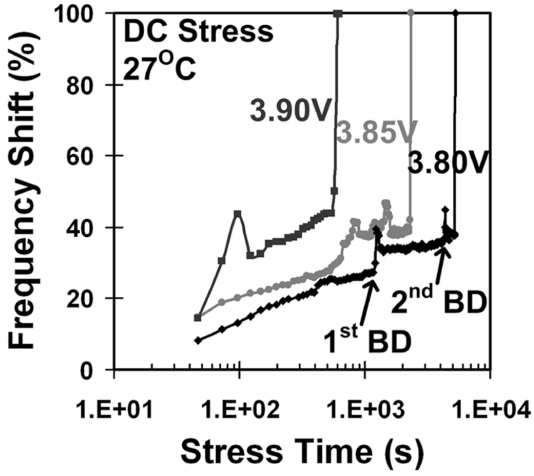


Fig. 18. ROSC frequency jumps attributed to TDDB before final circuit failure. The ROSCs continue to function after one or more apparent breakdowns.

accelerated HCI and had little impact on BTI. This acceleration of HCI with both increased input transition time and output load capacitance was reported in early HCI work [12], [13]. Those variables have been listed as two of the main controllable factors affecting hot carrier-induced degradation.

Fig. 16(a) shows BTI's positive correlation with temperature, and that HCI aging was slightly reduced at higher temperatures due to increased phonon scattering, which reduces drain current. Both aging mechanisms degrade with voltage [Fig. 16(b)], and we observe a decrease in HCI's power law exponent at lower voltages. This has been explained by a possible decreasing contribution of broken Si–O bonds (in comparison to Si–H bonds) at lower voltages, closer to real operating conditions [16], [17]. Also note the crossover point when HCI begins to dominate the overall aging is pushed out in time by an order of magnitude at 1.8 V stress compared to 2.4 V. This helps to illustrate the claim that BTI becomes dominant in modern technologies operating at lower supply levels.

Fig. 17 shows a common NBTI recovery characteristic, while the $\mathrm{HCI_{DEG}}$ component did not improve when stress was removed. One explanation for this behavior is the Si-H bonds at the interface broken by cold carriers during BTI stress are recoverable, while hot carriers also break Si-O bonds, which do not recover [16], [17].

C. TDDB Measurements in Stressed Ring Oscillators

Fig. 18 presents three examples of high voltage stress experiment results in which sudden jumps in ROSC frequency are interpreted as breakdown events. Thus far we have been ignoring TDDB in our results because it acts on a much longer timescale at lower stress voltages. In these experiments involving large frequency shifts, we did not use the beat frequency detection framework since it is aimed at high resolution measurements for smaller shifts. Instead, we directly read the frequency off-chip with an oscilloscope. Note that longer term experiments, or those done in future technology generations

where soft breakdowns are more prevalent, will be able to make use of the Odometer system. Fig. 18 shows that ROSCs do continue to function after one or more breakdowns, which only lead to reduced output swing and lower frequencies, as long as subsequent logic stages in the ROSC can restore full-rail swing [18].

V. Conclusion

We have implemented a test circuit in 65 nm technology that is capable of separately monitoring the frequency degradation induced by HCI, BTI, and TDDB. Sub-μs measurements are controlled by on-chip logic, and sub-ps frequency measurement resolution is achieved using the Silicon Odometer beat frequency detection system. This combination of fast measurements, which can avoid unwanted BTI recovery, along with high frequency resolution is facilitated by the Odometer framework, and is not possible in other standard measurement setups. We use a concept called "backdrive" to isolate BTI-induced aging in a ROSC gated off from the stress supply. This novel all-digital system can be used during process characterization, or for accurate real-time reliability monitoring and compensation schemes.

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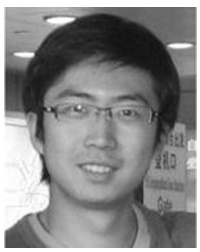

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