Variation Aware Performance Analysis of Gain Cell Embedded DRAMs

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Presentation Agenda

- Introduction to Gain Cell Embedded DRAM (EDRAM)
- Variation Analysis of EDRAM Performance
- Statistical Simulation Results and Analysis
- Conclusions and Future Work
# Embedded Memory Options

Source: K. Chun, VLSI Symp, 2010

<table>
<thead>
<tr>
<th>Cell Schematic</th>
<th>6T SRAM</th>
<th>1T1C eDRAM [1]</th>
<th>Gain cell eDRAM (2T[2], 3T[3])</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Cell Schematic" /></td>
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<tr>
<td>Process</td>
<td>Logic compatible</td>
<td>+2 (FEOL) +3 (Cap)</td>
<td>Logic compatible</td>
</tr>
<tr>
<td>Cell size (ratio)</td>
<td>1X</td>
<td>0.22X</td>
<td>0.48X</td>
</tr>
<tr>
<td>Data storage</td>
<td>Latch (Static)</td>
<td>Capacitor (20fF)</td>
<td>MOS gate (&lt;1fF)</td>
</tr>
<tr>
<td>Cell access</td>
<td>(+) Differential read (-) Ratioed operation</td>
<td>(-) Destructive read (-) refresh</td>
<td>(+) decoupled read and write, (-) refresh</td>
</tr>
<tr>
<td>Random cycle</td>
<td>1GHz</td>
<td>500MHz</td>
<td>500MHz</td>
</tr>
<tr>
<td>Static power (ratio)</td>
<td>1X</td>
<td>0.2X</td>
<td>0.23X</td>
</tr>
</tbody>
</table>

Cell Retention Time Issue

- Gain cells have very small storage capacitance
- Short retention time hurts read performance and increases refresh power (typical target ~ 100µsec)
- Retention time varies exponentially with PVT
• WL-to-BL delay (a.k.a. bitline delay) is critical
  – Time to develop voltage difference (ΔBL=100mV) between BL(D0) and BL(Reference)
  – Sensitive to data ‘0’ cell voltage at the time of access
  – Large variation due to gate leakage and junction leakage
Motivation: Corner Simulation Pitfall

- Corners fail to capture worst case eDRAM performance
  - Short hold period: worst case occurs at thick TOX, high VTH
  - Long hold period: worst case occurs at thin TOX, high VTH
Read Current Variation: TOX and VTH Effects

- TOX and VTH effects are independent in gain cells
- Thin TOX + high VTH combo results in worst case delay
VD0 vs. {TOX, VTH}

- DTOX or DVTH of each individual transistor swept
- Dominating parameter for VD0 is TOX
  - Gate leakage currents of write and storage devices determine VD0
**Bitline Delay vs. \{TOX, VTH\}**

- Dominating parameter for read current at fixed VD0 is VTH
- TOX and VTH affect gain cell performance in a different way as compared to standard logic
Comprehensive Monte-Carlo Results

- Incorporates global and local TOX and VTH variations
- Worst case cells change depending on hold period
Bitline Delay Map: TOX and VTH Effects

- EDRAM bitline delay colormap analysis
  - For simplicity’s sake, only global variations are applied (i.e. all devices have same TOX and VTH)
  - Examine equal delay contour at which 0.1% of the cells fail
  - Here, TOX and VTH are assumed to be independent Gaussian random variables

65nm LP, 1.1V, 85°C

Hold period: 300μsec

P_fail = 0.1%
Bitline Delay Map: Hold Period Effect

- Short hold period: VTH effect dominates
- Long hold period: TOX and VTH equally important
- Provides guidelines for process optimization considering eDRAM hold period targets
Conclusions and Future Work

• Gain cell eDRAM as an alternative for SRAM
  – 2X higher density, logic compatible, good low VDD margin
  – Short retention time due to small storage capacitance

• Standard corner simulations inaccurate for gain cell eDRAM performance analysis
  – TOX and VTH effects are independent in gain cells

• Gain cell eDRAM performance variation analyzed
  – Comprehensive Monte-Carlo, bitline delay colormap

• Future work
  – Performance analysis of novel gain cells (e.g. 2T, 2T1C, 3T)
  – Accurate and fast simulation methods for >6σ tail cells
  – Scaling trend analysis beyond 22nm