An *All-In-One* Silicon Odometer
for Separately Monitoring
HCl, BTI, and TDDB

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Outline of Presentation

• Introduction to Aging Mechanisms
• Proposed *All-In-One* Silicon Odometer Overview
• Improved Beat Frequency Detection System
• 65nm Test Chip Measurement Results
• Conclusions
### Aging in CMOS Transistors

- **Bias**
- **Temperature**
- **Instability**

- **Hot carrier injection**
- **Time dependent dielectric breakdown**

- Reports show ~10% circuit speed degradation after 10 years under normal usage
- Must account for 3 major aging mechanisms during process characterization

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J. Keane, et al., Trans. on VLSI 2009
M. Fakhruddin, et al., RFICS 2007
J. Keane, et al., CICC 2008
Combined Stress in Digital Circuits

NMOS

\[ I_D \]

Inverted Channel

HCl

PBTI

PMOS

\[ I_D \]

Inverted Channel

HCl

NBTI

NOTE: Voltage applied across dielectric → TDDB

Inverter

\[ V_{in} \]

\[ I_{Dn} \]

\[ I_{Dp} \]

Vin

\[ I_{Dn} \]

\[ I_{Dp} \]

V_{in} and

NMOS

HCl

PBTI

PMOS

HCl

NBTI

[Graph showing current levels for NMOS and PMOS with HCl, PBTI, and NBTI conditions]
Introduction to NBTI

Stress Conditions

- Channel holes interact with Si-H bonds at interface to create traps
- Increase in \(|V_{th}|\)
  - \(~20\text{-}30\%\) increase in 10 years
- Partial recovery occurs when PMOS is turned off

Recovery

T. Kim, et al., VLSI Symp. 2007
Introduction to HCl

HCl in NMOS

- Energetic carriers ($V_{DS} \neq 0V$) overcome Si-SiO$_2$ potential barrier
- Causes degradation of gate dielectric
  - Interfacial and oxide traps
  - Negatively trapped charges create potential hump
- Degradation not reversible
Introduction to TDDB

• Traps generated under influence of electric field
• Traps overlap
  – Conductive path between gate and substrate
• Gate dielectric no longer a reliable insulator
  – Parametric or functional failure
Aging Impacts on Circuits

- **BTI**
  - SRAM SNM degrades; write stability improves (when NBTI is dominant)

- **HCI/BTI**
  - $F_{\text{MAX}}$ degrades
  - Critical path changes due to asymmetric stress conditions
  - Subthreshold leakage decreases

- **TDDB**
  - Increased $I_{\text{GATE}}$ leads to reduced o/p swing, **SNM degradation**, etc...
  - Device failure

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R. Rodriguez, et al., IEDL, 2002

Breakdowns in different locations in SRAM cell
Prior Aging Measurement Methods

• Device probing with expensive wafer probes

• Karl proposed compact on-chip sensors for NBTI and TDDB (ISSCC 2008)

• Kim introduced the Silicon Odometer beat frequency detection concept (VLSI Symp. 2007; 2008 DAC/ISSCC Student Design Award)

• We implemented a test array for efficient statistical characterization of TDDB (CICC 2008; 2009 DAC/ISSCC Student Design Award)

• All-In-One Odometer presented here measures all three mechanisms with one test circuit
• 4 ROSCs: 2 stressed, and 2 unstressed
• One stressed suffers due to BTI only; the other "DRIVE" ROSC ages due to BTI & HCI
• Frequency degradation monitored with 2 Silicon Odometer beat frequency detection circuits
Backdrive Configuration

- **Stress Mode** (ROSC loops opened)
  - BTI_ROSC gated off from supply
  - DRIVE_ROSC drives transitions; I/P driven by VCO

- **Measurement Mode** (ROSC loops closed)
  - Both ROSCs connected to the power supply @ VCC
  - Switches between them are opened
BTI_ROSC in Stress Mode

Negligible HCI in BTI_ROSC

0V -- VSTRESS -- 0V

NBTI Stress  PBTI Stress

- BTI_ROSC gated off from supply in stress mode; node transitions driven by DRIVE_ROSC
- Peak I_D though “on” devices in the former is only 3-5% of that in the latter
- The BTI_ROSC ages due only to BTI, while the DRIVE_ROSC suffers both BTI and HCI
• **MEASURESTRESS (M/S)**
  - High during measurements; Low during stress
• 3 levels of adjustable fanout
• I/O transistors experience negligible aging compared to logic devices under same stress
Silicon Odometer Beat Frequency Detection

- Two free running ROSCs for beat frequency detection
- Sample stressed ROSC output using reference ROSC output
- Count PC_OUT to determine freq. degradation
- Insensitive to environmental variation

T. Kim, et al., VLSI Symp. 2007
Beat Frequency Detection Circuit

- Second implementation of the “odometer”
- Added 2b counter to automatically kick the circuit back into stress after 3 measurements are recorded
- With ROSC period of 3ns, and maximum count of ~100, sub-900ns measurement interruptions (3ns x 3 x 100)
**All-In-One Odometer 65nm Test Chip**

- **Technology**: 65nm, 7M
- **Logic/IO Supplies**: 1.2V / 2.5V
- **Active Area**: 38,040μm²
- **Total Area**: (214.22X551.43) μm²
- **ΔT Resolution**: < 1ps
- **Measure Interrupt**: < 1μs
Measured Aging Results

- No frequency shift is observed for 0V “stress”
  - Stress results are not the product of unforeseen circuit effects
- Under regular stress both BTI and HCI degradation follow a power law behavior
• BTI is at most weakly dependent on frequency; HCI degrades with increased switching
• Increased load cap $\rightarrow$ longer transition times,
  – Accelerated HCI
  – Little impact on BTI
Temperature and Voltage

- HCl slightly reduced with temperature
  - Reduced drain current
- Both mechanisms degrade with stress voltage
  - Point when HCl begins to dominate pushed out in time by >1 order of magnitude at 1.8V vs. 2.4V
Stress/Recovery and TDDB

- Common NBTI recovery; HCl\textsubscript{DEG} component did not improve when stress was removed
- Sudden drops in freq. interpreted as breakdowns
Conclusions

• Implemented single circuit to track BTI, HCl, and TDDB
  – Sub-µs measurement for minimal BTI recovery
  – Sub-ps frequency measurement resolution achieved with Silicon Odometer; measured frequency shifts down to ≤ 0.01%
• “Backdrive” used to isolate BTI-induced aging
• Test chip measurements presented with 1.8V – 3.9V stress, temperatures of 27°C & 120°C, and fanout increased by 3 inverter input caps
• Design can be used for cost and time efficient process characterization