An All-In-One Silicon Odometer for Separately Monitoring HCI, BTI, and TDDB

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Abstract

An on-chip reliability monitor capable of separating the aging effects of HCI, BTI, and TDDB with sub-ps precision is presented. A pair of stressed ring oscillators is implemented in which one ages due to both BTI and HCI, while the other suffers from only BTI. Frequency degradation is monitored with a beat frequency detection system achieving sub- μ s measurement times. Measurement results are presented from a 65nm test chip over a range of stress conditions.

Introduction

The parametric shifts or circuit failures caused by Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), and Time Dependent Dielectric Breakdown (TDDB) have become more severe with technology scaling, so these mechanisms must be studied in order to develop accurate reliability models. In addition to device probing experiments, several on-chip systems have been proposed to monitor circuit aging [1-2]. However, no method has been presented to isolate the effects of these three major reliability mechanisms in a single test. In this work, we accomplish that task with a pair of modified ring oscillators (ROSCs) which are representative of standard CMOS circuits. Unwanted device recovery during stress interruptions is avoided with automated subµs measurements. Sub-ps frequency measurement resolution is achieved for finely-tuned HCI and BTI readings, and experiments are automated through a simple digital interface. This design allows us to test the frequency dependency of stress mechanisms, monitor both sustained stress and recovery characteristics, and observe the effects of increased load capacitance. Finally, long term or high voltage stress is used to track time-to-gate dielectric breakdown.

Proposed Technique for Separating HCI and BTI

As shown in Fig. 1, CMOS devices suffer from HCI, BTI, and TDDB stress under standard digital operating conditions. Our proposed reliability monitor for separating the effects of the former two mechanisms is shown in Fig. 2. This circuit contains four ROSCs in total: two are stressed, and two unstressed to maintain fresh reference points. Each of the stressed oscillators is paired with its fresh reference during measurements, and the frequency degradation is monitored with the Silicon Odometer beat frequency detection circuit [1]. Fig. 3 presents the pair of stressed ROSCs in both stress and measurement states. During stress, the BTI_ROSC stages are gated off from the power supplies, while the DRIVE_ROSC maintains a standard inverter configuration with the supply set at VSTRESS. Both ROSC loops are opened, and the input of the DRIVE_ROSC is driven by a stress clock generated by an on-chip voltage controlled oscillator (VCO) whose output is level-shifted up to VSTRESS. The switches between these two ROSCS are closed so the DRIVE ROSC can drive the internal node transitions for both structures. Simulated voltage and current waveforms are shown in Figure 3. As seen there, the internal nodes of the BTI_ROSC switch between the supply level and 0V, as would be the case in standard operation. However, the peak drain current though the on devices in this structure is only 3-5% of that in the DRIVE_ROSC, since their sources are gated off from the supplies. Note that the sources of these "on" devices in the stressed BTI_ROSC are held at their respective supply levels due to the backdriving action of the DRIVE ROSC. Therefore, the BTI_ROSC will age due only to BTI stress, while the DRIVE_ROSC suffers both BTI and HCI stress. We can extract the contribution of HCI to the latter ROSC's frequency degradation with the equation $HCI_{DEG} = DRIVE_{DEG} - BTI_{DEG}$, where DEG stands for "degradation". During measurement periods, both ROSCs are connected to the power supply rails, the switches between them are opened, and they each operate independently in a standard closedloop configuration. A detailed schematic of one stage of the paired ROSCs is shown in Fig. 4. Both ROSCs contain three levels of adjustable fanout which allows us to test the effects of additional load capacitance on aging. The header and footer transistors in each inverter under test pin the source nodes of those gates to the supply rail levels when closed. During stress, there are no voltage drops across any pair of terminals in the headers or footers used during measurements, so we do not expect them to age significantly.

The Silicon Odometer measures frequency changes in the stressed ROSCs using the concept illustrated in Fig. 5. In this work, we improved that system by including logic which automatically sends the circuit back into a stress state after three consecutive beat frequency counts are recorded, in order to achieve measurement times of under 1µs. The completion of a measurement interruption is flagged by the MEAS_DONE signal in Fig. 6 when the three rising edges from the phase comparator are counted, meaning three 8b count results have been recorded for averaging. This flag is sent to the state machine which immediately restarts stress.

Test Chip Aging Measurements

A 214x551µm² test circuit was implemented in a 65nm CMOS process for concept verification. Measurements were automated with LabVIEWTM software through a National Instruments data acquisition board. Trimming capacitors were used in each 33 stage ROSC to ensure that the frequencies of the stressed structures began close to, but slower than, the reference frequencies. This guarantees a monotonic decrease in beat frequency count with stress degradation. Trimming was also utilized to push the oscillating frequencies of paired ROSCs apart to prevent injection locking. Fig. 7 presents example results for both ROSCs, as well as the calculated HCI_{DEG}. As expected, both BTI and HCI degradation follow a power law behavior, although the latter is seen to saturate at long stress times (it is predicted that BTI would also saturate in longer experiments). This can be explained by the finite number of bonds to be broken at the Si-SiO₂ interface and/or the self-limiting nature of HCI when the degraded drain current produces less hot carriers. Fig. 8(a) illustrates the impact of frequency on both stress mechanisms. These results verify that BTI is at most weakly dependent on frequency, while HCI degrades with increased switching activity. A decrease in the power law exponent n of the latter mechanism was observed at higher frequencies, which is apparently due to the quick saturation of degradation in this case. In Fig. 8(b) we see that increased load capacitance, which causes longer transition times, accelerated HCI and had little impact on BTI. Fig. 9 shows a common NBTI recovery characteristic, while the HCI_{DEG} component did not improve when stress was removed. Fig. 10(a) shows BTI's positive correlation with temperature, and that HCI aging was slightly reduced at higher temperatures due to increased phonon scattering which reduces drain current. Both aging mechanisms degrade with stress voltage (Fig. 10(b)), and we observe a marked decrease in HCI's power law exponent at lower voltages. This has been explained by a possible decreasing contribution of broken Si-O bonds (in comparison to Si-H bonds) at lower voltages, closer to real operating conditions. Also note the crossover point when HCI begins to dominate the overall aging is pushed out in time by an order of magnitude at 1.8V stress compared to 2.4V. This illustrates the claim that BTI becomes dominant in modern technologies operating at lower supply voltages. Fig. 11 presents three examples of high voltage stress experiment results in which sudden jumps in ROSC frequency are interpreted as breakdown events. Breakdowns cause the degradation curve to abruptly depart from its typical BTI-like characteristic.

References

T. H. Kim, et al., JSSC, vol. 43, no. 4, pp. 874-880, April 2008.
E. Karl, et al., ISSCC, pp. 410-411, 2008.



Stress conditions for NMOS and PMOS during typical Fig. 1. operation. BTI, HCI, and TDDB stress illustrated for an inverter.



Fig. 3. ROSC configuration during stress and measurement modes. The BTI_ROSC transistors suffer the same amount of BTI as the DRIVE_ROSC transistors, but with negligible HCI degradation.



Fig. 5. Beat frequency detection between a stressed and an unstressed ROSC achieves sub-1ps measurement precision [1].

Frequency Shift (%)

Frequency Shift (%)

1.E-01

both ROSCs under AC stress.

250MHz stress freq.

30⁰C: HCI_{DEG}↑, BTI_{DEG}↓

HCI_{DEG}↓, BT

2.0V stress



2.4V stress

.8V stress







Fig. 4. Schematic of one stage of the paired ROSCs including switch control signals.













1.E+00

1.E-0

(%)

Shift (

Frequency



1.E+02

3.90V

3.85\

1st

́вр

1.E+03

.85\

BC

Fig. 12. Chip photo and summary.

Measured frequency degradation results for (a) Fig. 8. three stress frequencies and (b) increased load capacitances.

%

Frequency Shift

26⁰C

470MHz stress freq

100

80

60

40

20

1.E+01

DC Stress

27⁰C