A Sub-0.9V Logic-compatible Embedded DRAM with Boosted 3T Gain Cell, Regulated Bit-line Write Scheme and PVT-tracking Read Reference Bias

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Abstract
Circuit techniques for enabling a sub-0.9V logic-compatible embedded DRAM (eDRAM) are presented. A boosted 3T gain cell increases read margin, enhances read speed and improves data retention time. A regulated bit-line write scheme and a read reference bias generator are proposed to cope with write disturbance issues and PVT variations. Measurement results from a 64kb eDRAM test chip implemented in a 65nm low-leakage CMOS process demonstrate the effectiveness of the proposed techniques.

Introduction
Embedded DRAMs (eDRAMs) are a potent alternative for mainstream SRAMs in nanoscale CMOS due to their small cell size and non-ratioed circuit operation. Recently, there have been a number of successful eDRAM designs in generic logic processes based on gain cells for embedded cache memories [1][2]. Gain cells can be implemented using 3 transistors, or even 2 transistors when used with delicate read control circuits, achieving roughly 2X higher bit cell densities. Furthermore, gain cells have a wider read/write margin than 6T SRAMs since there is no contention between the access device and the cross-coupled latch. Despite the recent advances in eDRAM circuit techniques, conventional gain cells still suffer from poor data retention time due to various leakage sources and Process-Voltage-Temperature (PVT) variation issues in sub-0.9V operating voltages.

Proposed 3T Gain Cell for Preferential Boosting
Read speed of eDRAMs is highly dependent upon the cell node voltage at the time of access. Even a small signal loss can cause severe speed degradation at low operating voltages. To overcome this problem, Luk et al. proposed a 3T1D gain cell where a diode transistor is used to preferentially boost the cell voltage via capacitive coupling [1]. However, this cell structure requires an additional transistor which increases the cell area as well as the gate tunneling leakage which is one the most critical constraints in eDRAM design. It also has a limited signal amplification effect as only a fraction of the node capacitance is used for boosting. Fig. 1 shows our proposed boosted 3T PMOS gain cell compared with other logic-compatible embedded memory structures including the 3T1D cell and 6T SRAM cell (layout comparisons are shown in Fig. 9). The proposed boosted 3T gain cell can provide a stronger coupling effect with only 3 transistors, enhancing the Read Bit-Line (RBL) margin and improving read performance. By connecting the source of the storage transistor to the Read Word-Line (RWL) signal, the activated cell node voltage can be preferentially amplified using the RWL coupling. The proposed cell can provide ~2X larger current than conventional 3T gain cells when the RBL swing is small. When the RBL discharges to GND however, the RBL current decreases significantly because of the V_{TP} drop. To utilize the large boosted read current while the RBL level is close to VDD, we use a hybrid current/voltage sense amplification technique to limit the RBL swing [3]. Fig. 2 shows the array structure with the proposed cell and Fig. 3 shows the schematic and timing diagram of the bit-line Sense Amplifier (S/A) consisting of a hybrid current/voltage S/A and drivers for writeback and write. During read, the RBL signals to the current S/A are amplified and converted to voltage signals through a cross-coupled PMOS pair while a load PMOS pair keeps the RBL swing small. After amplifying the input differential current, the cross-coupled PMOS pair, along with the cross-coupled NMOS pair, also acts as a voltage S/A for full CMOS swing. Dedicated timing control circuits are implemented for the equalizer to ensure stable current S/A operation. The writeback operation

follows the read cycle to refresh the cell data. Monte-Carlo simulation results in Fig. 4 show that the 3T boosted gain cell can enhance the read speed by 41% compared with a conventional 3T gain cell.

Regulated BL Write Scheme and PVT-tracking Read Bias
When data '1' is written to a cell, the data '0' levels in the unselected cells on the same Write Bit-Line (WBL) are pulled up by the large sub-threshold leakage in the write access PMOS devices (Fig. 5(left)). Previously, a boosted supply was used for the WWL to prevent the signal loss in the unselected cells by applying a negative Vgs in the write access devices. However, this method incurs significant area and power penalty at sub-0.9V due to the large charge pump capacitors and/or poor pumping efficiency. In this work, we propose a regulated bit-line write scheme which can eliminate the data '1' disturbance issue without having to introduce a boosted supply. As shown in Fig. 5(center), without a refresh, the cell node voltage converges to a steady-state level close to VDD regardless of the initial data. We use this voltage level for writing data '1' (VWR in Fig. 2) as it will produce a negative Vgs in all unselected cells without affecting the retention time of the selected cell. A steady-state storage node voltage monitor shown in Fig. 5(right) is implemented with replica cells in hold mode, followed by a voltage down converter to drive the large WBL load. The speed loss due to the regulated bit-line write voltage is eliminated by precharging the WBL to VWR using the negative supply, VBB, which is already present in the chip for the WWL underdrive.

An optimal reference bias voltage (VDUM in Fig. 2) is applied to the reference cells to maximize the read operating margin. VDUM must be carefully chosen as it affects both the data retention time and read speed; a higher VDUM level improves the data retention time at the cost of lower read speed. Fig. 6 shows the proposed temperature-dependent and die-to-die adjustable read reference bias generator to cope with large PVT variations. This circuit can achieve a target retention time without sacrificing read speed by adaptively reducing the VDUM level at low leakage PVT conditions.

EDRAM Test Chip Measurements
A 64kb eDRAM test chip was implemented in a 1.2V, 65nm low-leakage logic CMOS process to demonstrate the proposed circuit techniques. To fully verify the proposed techniques against the existing ones, each sub-array has a different combination of cell structure (boosted 3T vs. conventional 3T) and reference scheme (proposed PVT-tracking vs. cell averaging [2]). Fig. 10 shows the die microphotograph and key features of the fabricated chip. Fig. 7 shows the VWR measured at different supply voltages. The data retention characteristics between the data '1' disturbance case and the data hold mode case becomes indistinguishable using the proposed regulated bit-line write scheme. Fig. 8 shows the measured data retention characteristics including its cell-to-cell variation. The proposed boosted design achieves a data retention time of 1.25msec at 0.9V, 85ºC, which is a 10X improvement compared with that of the conventional 3T cell measured from the same silicon die. The refresh power consumption is 91.3µW per Mb at 1.0V, 85ºC.

References
[1] W. Luk et al., VLSI Circuits Symp., pp. 184-185, 2006.
[2] D. Somasekhar et al., ISSCC, pp. 274-275, 2008.
[3] J. Sim et al., JSCC, vol. 38, no. 4, pp. 631-639, 2003.

	CONV 3T (2T [2])	3T1D [1]	Proposed 3T	6T SRAM
*Cell schematic	(schematic)	(schematic)	(schematic)	(schematic)
Features	Small size	Partial cell node amplification	Full cell node amplification	Fast
Issues	Short retention time	Additional device	RWL noise	Large size, low noise margin
**Cell size (ratio)	0.54x1.02= 0.551μm² (1.0X)	0.64x1.14= 0.73μm² (1.32X)	0.615x1.02= 0.627μm² (1.14X)	0.575x2.05= 1.178μm² (2.14X)
***RWL-BL delay (0.9V, Δ=100mV)	1.07ns	0.86ns	0.63ns	0.40ns
Retention time	110μsec (measured)	***200μsec	1.25msec (measured)	-
Static power	Large due to short retention time	Medium	Small	Large due to transistor leakage

* PMOS cells for low I_{gate}, ** 65nm logic design rule, *** Monte-carlo 3σ simulation results

Fig. 1. Comparison of logic-compatible embedded memories.

Fig. 2. Array structure for the proposed boosted 3T gain cell. VWR and VDUM generation circuits are shown in Figs 5 and 6.

Fig. 3. Hybrid bit-line current/voltage Sense Amplifier (S/A) with writeback and write drivers (left). Read-writeback timing diagram of the proposed S/A (right).
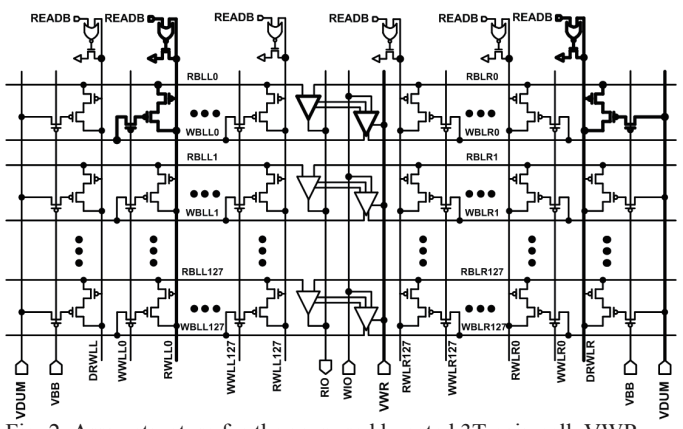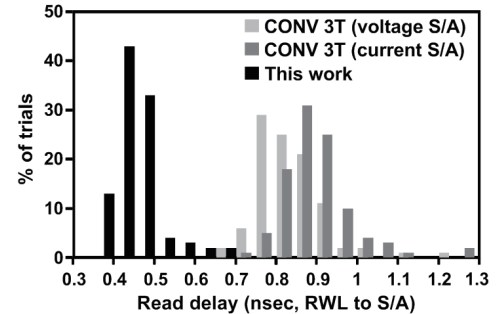

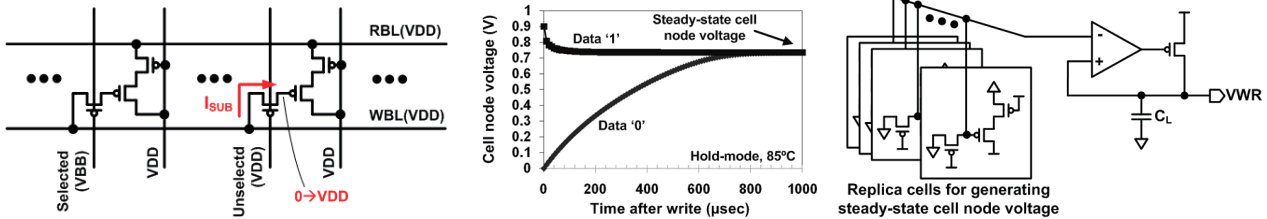Fig. 4. Monte-carlo simulation results of read speed for proposed and conventional cells.

Fig. 5. Cell disturbance problem when writing '1' to other cells on the same bit-line (left). Data retention simulations showing the steady-state cell node voltage (center). Proposed regulated bit-line write bias generator based on replica cells (right).
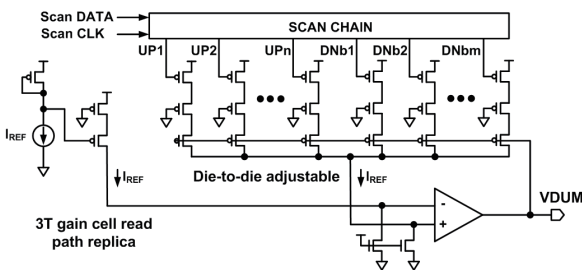

Fig. 6. Temperature-dependent and die-to-die adjustable read reference generator for PVT-tracking.
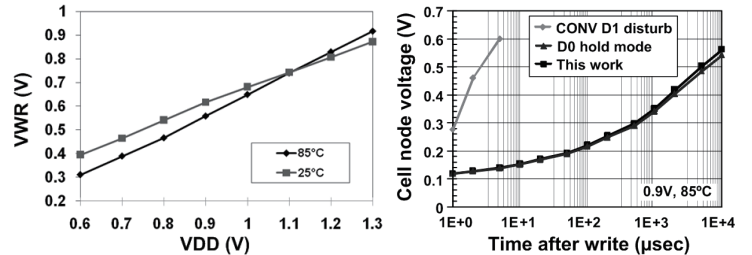

Fig. 7. Measurement results of VWR level (left) and cell node voltage of the proposed regulated write scheme compared with the conventional 3T gain cell under data '1' disturbance condition (right).
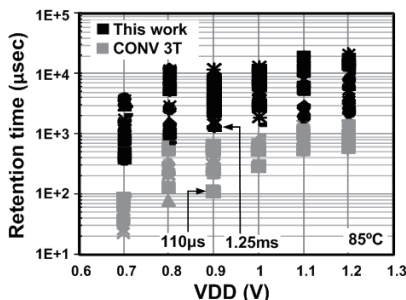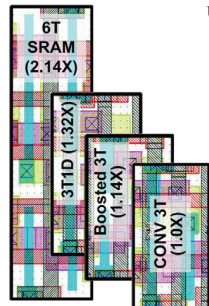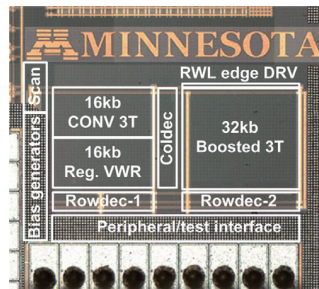

Fig. 8. Measured retention time statistics.

Fig. 9. Comparison of cell layouts in 65nm.

Process	65nm LP CMOS (7-MET)
Circuit dimension	250.7x129.9μm²
Cell size	53% of 6T SRAM
Retention time	> 1.25ms @ 0.9V, 85ºC
Operating voltage	1.2V - 0.7V
Preferential cell boosting @ 1.0ms	0.27V for data '0' 0.14V for data '1'
Cycle time	2.0ns @ 0.9V (simulation)
Refresh power	91.3μW per Mb @ 1V, 85ºC, 1.0msec refresh rate

Fig. 10. Die photo and key features of the eDRAM test chip.