Design and Implementation of Active Decoupling Capacitor Circuits for Power Supply Regulation in Digital ICs

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***Abstract*—Control of on-chip power supply noise has become a major challenge for continuous scaling of CMOS technology. Conventional passive decoupling capacitors (decaps) exhibit significant area and leakage penalties. To improve the efficiency of power supply regulation, this paper proposes a distributed active decap circuit for use in digital integrated circuits (ICs). The proposed design uses an operational amplifier to boost the performance of conventional decaps. Simulations proved its enhanced decoupling effect in comparison with passive decaps. The proposed active decap also shows advantages in providing additional damping to the on-chip resonant noise. To verify the performance from the proposed circuit, a 0.18-μm test chip with on-chip noise generators and sensors has been fabricated. Measurements show a 4-11$\times$ boost in decap value over conventional passive decaps for frequencies up to 1 GHz with a total area saving of 40%. Local supply noise distribution and decap gating capability were also examined from the test chip.**

***Index Terms*—Circuit modeling, integrated circuit (IC) design, power supply noise.**

I. Introduction

As TRANSISTOR dimensions scale beyond the 45-nm technology node, the control of power supply noise becomes one of the major challenges in modern VLSI circuit design [1]. The higher device density and lower operating voltage have inevitably caused an increase in operating current which can reach 100 A + in high-end microprocessors. On the other hand, the on-chip power supply network impedance has not been able to scale accordingly due to limited wire resources and near-constant resistance–capacitance (*RC*) product for interconnects. As a result, on-chip power supply noise which is the product of the operating current and the power supply network (PSN) impedance has increased to a point where it can jeopardize the functionality of digital circuits [1]. Furthermore, the supply voltage has dropped below 1 V which exacerbates the supply noise impact on the circuit performance, reliability, and noise margin. The detrimental impact caused by the noisy power supply include the following: 1) speed of digital circuits will significantly suffer from the large supply voltage droop [2]; 2) the timing constraints and noise margin requirements can be violated from the supply variations [3], [4]; 3) supply voltage overshoot causes reliability issues such as hot carrier injection (HCI) and negative bias temperature instability (NBTI) [5], [6]; and 4) power supply noise in digital domain can propagate through the substrate leading to performance degradation in analog circuits [7]. In order to continue the historical rate of progress towards the ultimate limit of CMOS scaling, Moore's law calls for the most efficient and intelligent way of power delivery.

Conventionally, passive decoupling capacitors (decaps) are used to suppress the power supply noise which is typically maintained within 10%–15% of the nominal supply voltage [8]. However, two major constraints limit the usage of passive decaps in scaled technologies. First, adding on-chip decaps consumes a large amount of die area. Usually, a total on-chip decap of $\sim$100 s of nFs or more have to be deployed on a microprocessor die to keep the supply noise within the target range [9]. As a result, in some high-end microprocessor chips more than 20% of the total area has been occupied by decaps leading to a significant waste of active die area [10]. Second, adding on-chip decaps introduce large amount of gate tunneling leakage that eats into the power budget. Gate capacitance of MOS devices are predominantly used for decaps. The thin oxide offers a higher capacitance per area compared to other types of capacitors such as metal-insulator-metal (MIM) structures. However, the scaling of oxide thickness to control the short channel effect has introduced a large amount of gate tunneling leakage which is becoming one of the major power components in modern VLSI chips. The dramatic increase in gate tunneling leakage is due to the exponential relationship between the tunneling current and the gate-oxide thickness [11]. Fig. 1 shows the contribution of each power component including the decap leakage in a modern IC [12]. As shown in the figure, decap leakage already constitutes 10% of the total power during normal operation for certain high-speed microprocessors. During burn-in conditions where an elevated temperature and higher supply voltage are applied, the decap leakage can become more than 20% of the total power consumption. Thus conventional passive decaps are becoming less and less efficient in controlling power supply noise with device scaling due to the area and power loss.

Several different capacitor boosting techniques have been developed previously to effectively improve the performance of on-chip decaps. An on-chip voltage regulator using switched decap circuit was proposed in [13] to regulate the power supply noise. When a large supply undershoot is sensed by the regulator circuit, the two parallel-connected decaps are switched

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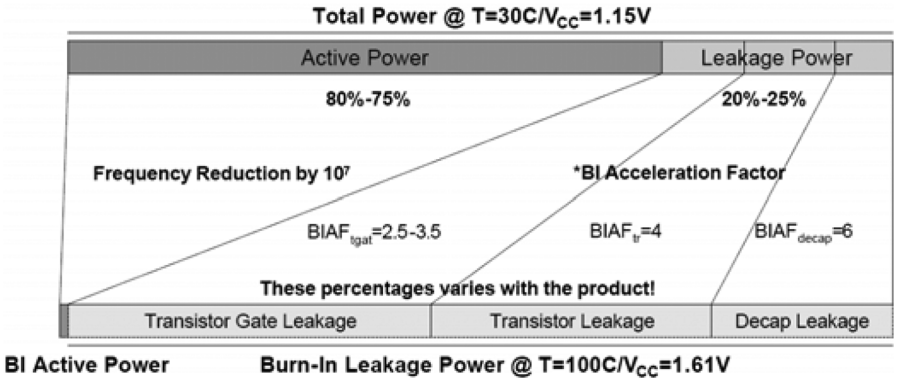

Fig. 1. Contributions of various on-chip power components as percentages of total power in both normal condition and burn-in condition. The on-chip decaps are shown to introduce a significant amount of tunneling leakage in scaled technologies [12].

into a series connection and thus a large amount of charge can be dumped into the supply network to cancel the undershoot. During supply overshoot or idle state, the capacitors remain in a parallel configuration to restore the charge in the decaps. Compared with conventional passive decaps, a 13× boost in decap performance has been reported using the switched decap circuits [13]. Although this work effectively boosts the decap value, the regulation frequency was limited below 200 MHz due to bandwidth limitations of the operational amplifier (opamp) used in the regulator circuit. Thus, this circuit was only used to regulate the mid-frequency on-chip resonant noise below 100 MHz. Recently an active decap circuit was introduced in [14] to suppress the substrate noise in mixed-signal integrated circuits (ICs). The concept was based on the Miller effect using the gain of an active opamp to boost the effective capacitance value. Limitations on this design include: 1) the requirement of several bias voltages which makes the design hard to be implemented in a digital IC; 2) the limited output swing due to the use of a pMOS source follower which leads to an insufficient noise regulation range especially during the supply undershoot; and 3) large area consumption from the input coupling capacitors ($\sim$ 10 pF).

This paper describes an active decoupling capacitor circuit for power supply noise cancellation for general digital ICs. Unlike the previous designs, this circuit is self-biased without any extra bias voltages and thus can be easily implemented in a digital chip. The output swing has been maximized to increase the regulation range. The performance of the proposed circuits was verified from a test chip in a 0.18-μm CMOS technology. Measurement results are shown to confirm the effectiveness of the proposed active decap circuits. For saving of quiescent power consumption, the gating capability of the decap circuits has been tested. Layout comparison between the conventional and proposed active decap circuits is also shown to evaluate the total area saving.

II. Active Decap Circuit Design and Simulation Results

To boost the effective decap value, an active decap circuit based on Miller effect is developed in this paper. Miller compensation technique has been widely used to improve the stability of a two-stage operational amplifier in analog circuits [15]. Fig. 2 shows the principle of using Miller effect for decap boosting. Connecting a conventional passive decap $C_{\rm load}$ between the

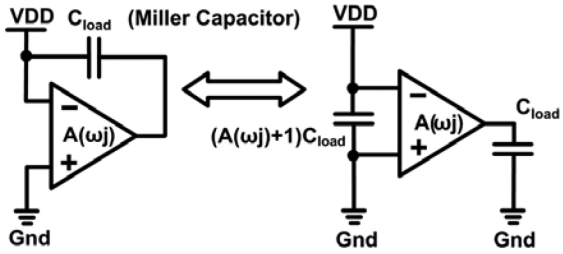

Fig. 2. Principle of decap boosting based on Miller effect. The decap value seen from the power supply has been boosted by a factor of $(1 + A(\omega j))$.

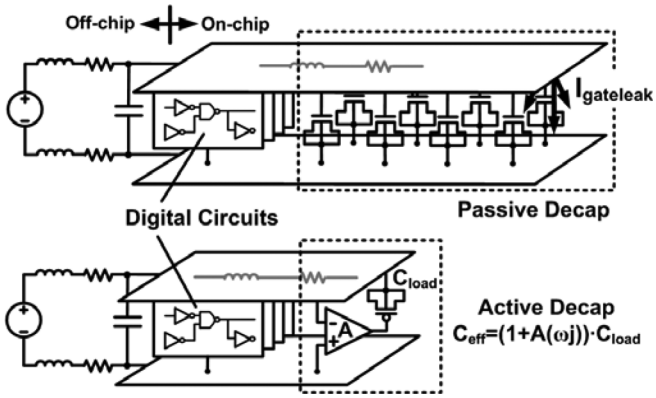

Fig. 3. Comparison of power supply network with conventional passive decaps and proposed active decaps.

output of the opamp and an input of the opamp, i.e., the supply voltage $V_{\rm DD}$ in this case, the effective decap value $C_{\rm eff}$ looking from the supply rails will be boosted by a factor of $(1+A(\omega j))$, where $A(\omega j)$ represents the gain of the opamp and is a function of the operating frequency ω. Equation (1) summarizes this effect

$$C_{\rm eff} = (1 + A(\omega j))C_{\rm load}. \tag{1}$$

Based on the previous equation, we propose to replace the conventional passive decap with the active decap circuit consisting of an opamp and a load capacitor. Fig. 3 compares the supply network configuration with the conventional passive decap and the proposed active decap for suppression of supply noise. By using active decap circuits, both decap area and the

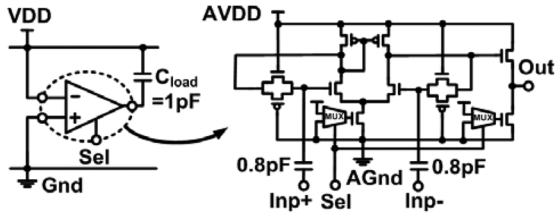

Fig. 4. Schematic of the proposed active decap circuit.

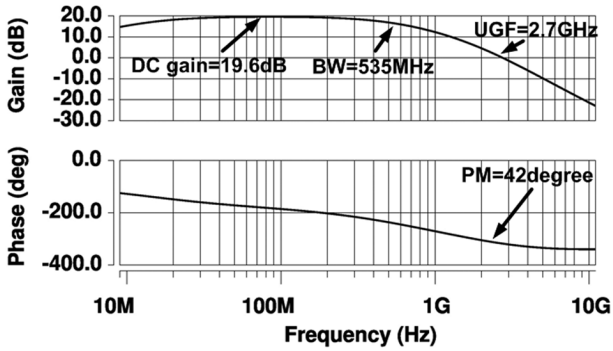

Fig. 5. Simulated bode plot of the active decap opamp.

leakage power can be reduced. Unlike in the passive counterpart where decap tunneling leakage is difficult to be gated when the power supply is on, the static power consumption of the active decap can be easily cut off by shutting down the operation of the opamp.

Fig. 4 shows the circuit schematics of the proposed active decap circuit. The two stage opamp contains a differential pair and a source follower stage. The differential pair senses the differential noise and provides the signal gain while the source follower stage serves as a driver for the capacitive load. The supply voltage variation, i.e., $V_{\rm DD}$ and $G_{\rm nd}$ noise, is capacitively coupled to the gate of the differential pairs which measure the differential noise $V_{\rm DD}$–$G_{\rm nd}$. For sufficient noise coupling, a 0.8 pF MOS capacitor is used to couple $V_{\rm DD}$ and $G_{\rm nd}$ noise. This coupling capacitance is significantly larger than the gate capacitance of the differential pair so that the signal loss due to capacitive coupling is minimized. Compared with [14] which use a 10-pF coupling capacitor, the area overhead in the proposed circuit is significantly reduced. Since the gate voltage of the differential pair is dc biased close to the middle of $V_{\rm DD}$ and $G_{\rm nd}$, the coupling capacitors are always operating in the inversion mode regardless of the supply variation. The dc bias of the differential pair is provided by two always-on transmission gates as shown in the figure. The resistance of the transmission gates is set high so that the transmission gate and the gate capacitance of the differential pair form a low-pass filter with a cutoff frequency of around 1 MHz which is below the targeting regulation frequency of our on-chip decap circuits. With such a biasing configuration, noise lower than 1 MHz will not be sensed by the opamp. This is totally acceptable for on-chip supply regulation because the low frequency supply noise usually comes from the off-chip components such as the package and motherboard traces and thus can be suppressed more efficiently using off-chip capacitors and voltage regulators [16]. The self-biasing scheme used in the active decap circuit avoids the use of biasing voltage and ensures the differential pair to operate in a saturation region.

Obtaining a large output swing in the source follower stage is important since an insufficient swing will lead to the degradation of decap gain in case of a large input noise magnitude. To maximize the output swing especially in case of a supply undershoot which is generally a bigger concern than an overshoot, an nMOS source follower stage is used instead of a pMOS one. This provides an output swing greater than 1 V for a supply undershoot and a swing greater than 400 mV for a supply overshoot. This large operation range ensures that under regular supply noise condition, maximum opamp gain can be maintained without being degraded by the limited output swing of the opamp.

In order to avoid the extra routing effort for the biasing signals, the bias voltages of the two current source transistors in the opamp are tied to $V_{\rm DD}$. Such a configuration saves the extra routing resources for the bias signals and makes it easier to implement the proposed circuit in a digital IC. The performance loss due to the coupled supply noise in the current source transistors has been simulated to be around 0.8 dB or 9% of the opamp gain compared to the case using an ideal bias voltage where transistors are biased in the saturation region. This minor performance degradation is acceptable considering the saving of routing effort. To cut off the static current during idle mode, multiplexers are used to dynamically switch off the bias voltages of the current source when the active decap circuit is not needed. Fig. 5 shows the simulated Bode plot of the opamp. The designed opamp had a dc gain of 18.9 dB, a bandwidth of 535 MHz, a unity gain frequency of 2.7 GHz, a phase margin of 42 degrees, and a static current of 3.8 mA.

The supply noise suppression using active decaps can be evaluated by using a simplified power supply network model in Fig. 6(a). The impedance seen by the on-chip current source $I_{\rm ac}$ can be derived using the on-chip decap components in parallel with a series-connected resistor *R* and inductor *L*. Here, we denote C_0 as on-chip intrinsic circuit capacitance and C_d as the added decap for noise suppression. *R* is parasitic resistance of the power supply network and *L* is the inductance mainly coming from the bonding wires. Note that the ac supply noise is simply the impedance multiplied by the exciting current $I_{\rm ac}$. The impedance at a particular frequency ω (radians per second) is found as follows based on the supply model in Fig. 6(a):

$$Z(\omega) = \frac{R + L\omega j}{1 - L\omega^2(C_0 + C_d) + R(C_0 + C_d)\omega j}. \quad (2)$$

In case of active decap, C_d can be replaced by $A(\omega j)\cdot C_d$, where $A(\omega j)$ is the gain of the amplifier and C_d is the capacitance load of the active decap. Assuming a single stage opamp with a dc gain of A and a dominant pole at ω_0, $A(\omega j)$ can be expressed as

$$A(\omega j) = \frac{A}{1 + \frac{\omega}{\omega_0} j}. \quad (3)$$

The impedance with an active decap is calculated as shown in (4) at the bottom of the next page.

This simple formula can be used to model and analyze the active decap circuits. Because a first-order system can be represented by a *RC* network, an active decap is modeled by a series

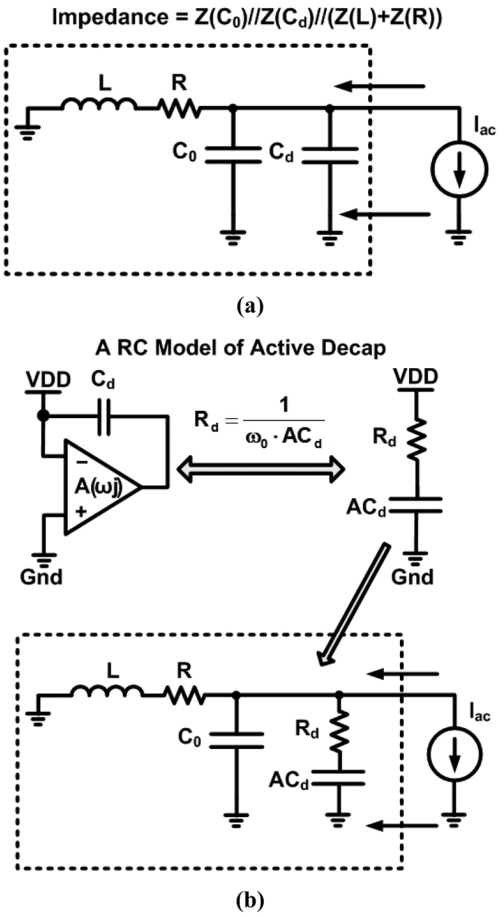

Fig. 6. Simplified *RLC* model for power supply impedance calculation. (a) Supply impedance with passive decaps; (b) supply impedance with active decaps modeled by an effective *R* and *C*.

connected resistor and capacitor. Fig. 6(b) shows the passive model of the active decap in a power supply network. The effective capacitance becomes $A \cdot C_d$ where C_d is the load capacitance of the opamp. The effective resistance R_d can be found by equating the impedance of $A(\omega j) \cdot C_d$ with the impedance of the series connected *R* and *C*

$$\begin{aligned} Z(A(\omega j) \cdot C_d) &= \frac{1}{\left(\frac{A}{1+\frac{\omega}{\omega_0} j} \cdot C_d \cdot \omega j\right)} \\ &= Z(R_d) + Z(A \cdot C_d) \\ &= R_d + \frac{1}{A \cdot C_d \cdot \omega j}. \end{aligned} \tag{5}$$

Thus the effective resistance is found to be

$$R_d = \frac{1}{\omega_0 \cdot A C_d}. \tag{6}$$

The *RC* model in Fig. 6(b) provides a straightforward method to estimate the decoupling performance of active decaps. As an example, for our test chip, ω_0 is at 500 MHz, A is 10, and C_d is between 1 to 20 pF. As a result, R_d varies between 2 to 30 Ω depending on the C_d value. In an ideal case when R_d is zero, the active decap performs the same as a capacitor with a value $A{\cdot}C_d$. This corresponds to an ideal opamp with the dominant pole $\omega_0 j$ at infinity, or in the other words, with a delay of zero. As the pole $\omega_0 j$ becomes smaller, or the delay of the opamp becomes larger, the effective resistance in (6) also becomes larger. As a result, the capacitor $A \cdot C_d$ is "isolated" by a larger resistance and its decoupling performance is therefore degraded. This simple passive model is useful for estimating full-chip level power supply noise where HSPICE cannot be used due to the long simulation time. Note that a small error exists in the simple *RC* model because a real opamp always contains multiple poles and zeros. Our studies show that the modeling accuracy can be further improved by including a second pole into (3). For simplicity, we also ignored the constant "1" in (1) assuming $A(\omega j)$ is much larger than 1 which is valid in most situations. A capacitor C_d can be simply added between $V_{\rm DD}$ and $G_{\rm ND}$ to model this ignored term if necessary. Equation (6) will still hold true in that case.

To verify the active decap's performance, we performed HSPICE simulation for the following different configurations: 1) no decap $(C_d = 0)$; 2) 100 pF passive decap; 3) a 200 pF passive decap; 4) a 10 pF active decap using 10 active decap circuits with 1 pF load each; 5) a 10 pF active decap using a single active decap circuit with a 10 pF load; 6) a 20 pF active decap using 20 active decap circuits with 1 pF load each. $R = 0.2\ \Omega$, $L = 4$ nH, and $C_0 = 200$ pF was used as the supply network parameters. The results in Fig. 7 show that a 10 pF active decaps performs consistently better than a 100 pF passive decap within the bandwidth of the opamp leading to an effectively 10× gain of the decap value. On the other hand, the performance gain of an active decap driving large load as in the test case (5) is limited to lower frequencies because of the smaller bandwidth of around 250 MHz. Fig. 7 also reveals a resonant noise with a large magnitude between 100 and 200 MHz. This resonant noise comes from the *LC* tank formed between bonding wire and on-chip capacitance. Resonant noise has posed a severe threat to circuit's performance because of

$$\begin{aligned} Z(\omega) &= \frac{R + L\omega j}{1 - L\omega^2\left(C_0 + C_d \cdot \frac{A}{1+\frac{\omega}{\omega_0} j}\right) + R\left(C_0 + C_d \cdot \frac{A}{1+\frac{\omega}{\omega_0} j}\right)\omega j} \\ &= \frac{R + \left(L + \frac{R}{\omega_0}\right) \cdot \omega j + \frac{L}{\omega_0} \cdot (\omega j)^2}{1 + \left(\frac{1}{\omega_0} + R(C_0 + AC_d) \cdot \omega j\right) + \left(\frac{RC_0}{\omega_0} + L \cdot AC_d + LC_0\right) \cdot (\omega j)^2 + \frac{LC_0}{\omega_0} \cdot (\omega j)^3}. \end{aligned} \tag{4}$$

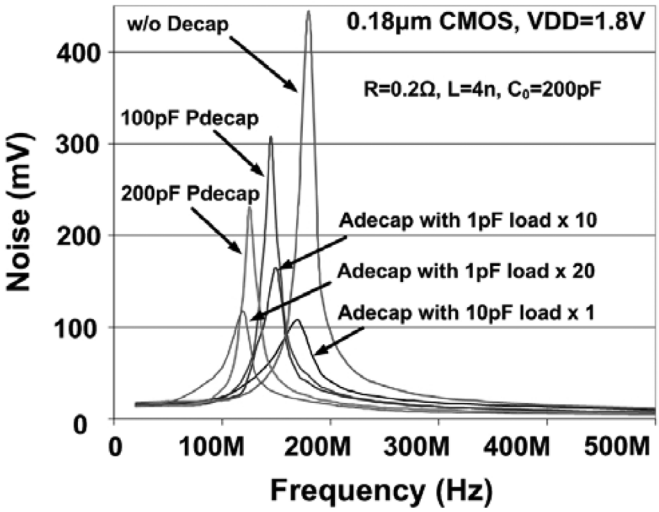

Fig. 7. Simulated noise suppression performance with various value of passive decaps (100 pF, 200 pF) and active decaps (10 pF, 20 pF).

its large magnitude and long duration. Circuit techniques have been previously proposed to suppress the resonant noise [17], [18]. The proposed active decap circuit that was targeted for supply noise regulation in a wide frequency band can also be adjusted to specifically reduce the low frequency resonant noise. As shown in Fig. 7, compared with the passive decaps, the resonant peak is further reduced by more than 50% with the proposed active decap circuit. Comparing the performance of 10 active decap circuits with 1 pF load each versus a single active decap circuit with a 10 pF load, we see that although both configurations significantly suppress the resonant noise, the resonant magnitude and frequency after applying each circuit are different. This is due to the difference in the ω_0 values in the two configurations. Equation (6) reveals that the smaller ω_0 of the 10 pF load active decap makes the effective resistance R_d larger. The larger resistance not only provides more damping but also shifts the resonant frequency higher because it degrades the effective decap value. Note that the resonant frequency is given by $1/\sqrt{LC}$, where L and C are the total inductance and capacitance in the network. Furthermore, the total static current dissipation of the active decap with a 10 pF load is $10\times$ smaller than that of 10 active decaps with 1 pF load. The two configurations are compared in Table I. The differences in decoupling performance and power with various load on the proposed circuits suggest that for applications where the mid-frequency noise is dominant, the active decap can be configured with a large capacitive load to reduce the power consumption while still maintaining a sufficient decoupling performance. As an example, if the proposed circuit is only targeted for resonant suppression, the power consumption can be further reduced by $10\times$ while the decoupling performance is even increased. Therefore the tradeoff between power and speed has to be carefully judged by designers based on the specific application of the active decap so that the best performance is achieved. It is also important to understand that the resonant noise not only can be excited by a repetitive current withdrawal at the resonant frequency but also can be excited by an abrupt current

TABLE I
COMPARISON OF ACTIVE DECAPS WITH LOAD OF 1 AND 10 pF

	Active decaps with 1pF load (x10)	Active decap with 10pF load (x1)
Opamp bandwidth	540MHz	250MHz
Total power consumption	38mA	3.8mA
Resonant noise suppression (~170MHz)	10.5dB	12.3dB
High-freq noise suppression (500MHz)	3.3dB	0.85dB

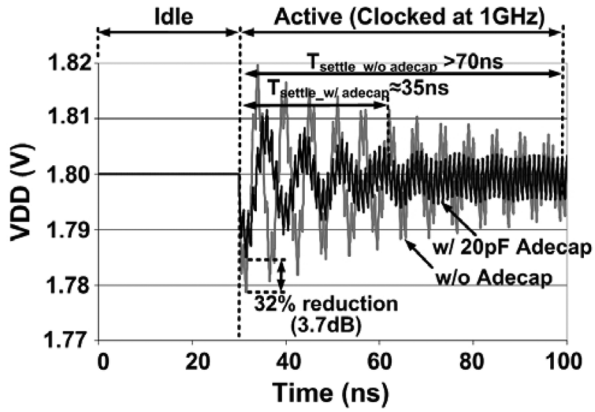

Fig. 8. Supply noise waveform during circuit startup showing 50%+ reduction in resonant period and 32% reduction in resonant noise magnitude.

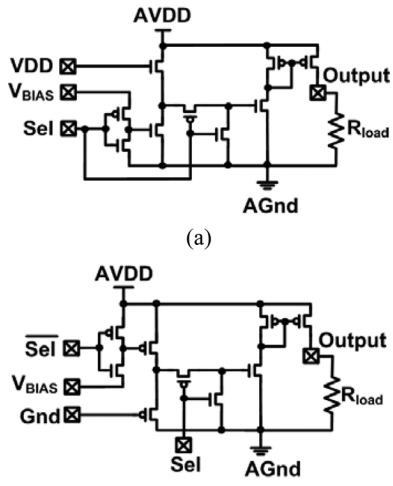

Fig. 9. Schematics of (a) $V_{\rm DD}$ sensor and (b) $G_{\rm nd}$ sensors.

change during circuit mode transitions [17]. Fig. 8 shows the comparison of noise waveforms during the circuit's startup. A 1-GHz clock is instantly activated after the circuit turns from idle mode to active mode. A resonant oscillation is excited due to the current spike. By using the active decap, an extra amount of damping has been provided achieving 50%+ reduction in oscillation duration and 32% reduction (or 3.7 dB) in oscillation magnitude.

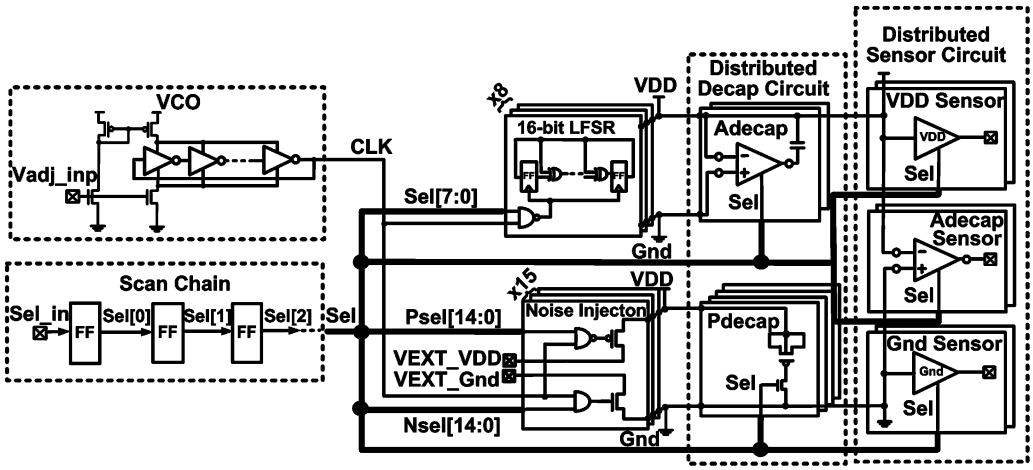

Fig. 10. Organization of the test chip.

III. Test Chip Implementation

To test the proposed active decap circuits, a 2.7 mm × 1.9 mm test chip was fabricated in a 0.18 μm, 1.8 V, 6-metal, triple-well CMOS technology. Two different types of sensors were used to measure the on-chip power supply noise. The first type of sensor reuses the active decap circuit itself with the load capacitance removed. The active decap sensor is capable of measuring differential supply noise $V_{\rm DD}$-$G_{\rm nd}$ directly with a gain of around 14 dB considering the capacitance of the output pin. Note that since we are only comparing the performance between the passive decap and active decap, the calibration of the active decap sensor is not crucial for analyzing the measurement results. A second type of sensor was used to measure the $V_{\rm DD}$ and $G_{\rm nd}$ noise separately [19]. Fig. 9 shows the schematics of the $V_{\rm DD}$ and $G_{\rm nd}$ sensor. A source follower stage brings the noise into the opamp where a current mirror transfers the noise signal into a shared output pad connected with an external resistive load. Because of the sharing of the output pad, only one pair of $V_{\rm DD}$ and $G_{\rm nd}$ sensor can be activated at a time and therefore a select signal is used to turn on a particular sensor on the chip. The $V_{\rm DD}$ and $G_{\rm nd}$ sensors have a gain of 0 dB, a bandwidth of 800 MHz, and a static current consumption of 12 mA. To measure the on-chip local supply noise, both types of sensors are distributed at four different locations on the chip with the select signals working as on-off switches.

Fig. 10 shows the organization of the test chip. To generate switching noise on the supplies, two types of noise generation circuits were implemented: 8 sets of 16-bit linear feedback shift register (LFSR) circuits and 15 sets of external noise injection circuits. Each noise generation circuit is capable of generating 4 mA current leading to a maximum load current of 60 mA. The LFSR circuits simulate the switching events of a real digital IC where random high frequency noise components exist even though the circuit is running at a fixed clock frequency. On the other hand, the noise injection circuits are capable of generating supply noise concentrated at a particular clock frequency and thus making it easier to analyze the active decap effectiveness in frequency domain. Furthermore, unlike the LFSR circuits, the noise injection circuits can generate noise on the $V_{\rm DD}$ or $G_{\rm nd}$ either separately or simultaneously bringing a higher level of flexibility for the testing. An on-chip voltage controlled oscillator with a tunable frequency up to 1.3 GHz is used as the clock source for both noise generation circuits. By turning on different numbers of LFSR circuits or noise injection circuits, the magnitude of supply noise can be adjusted. Finally, different numbers of passive and active decaps are distributed around the noise generation circuits with select signals used to turn on or off different decap values for performance comparison.

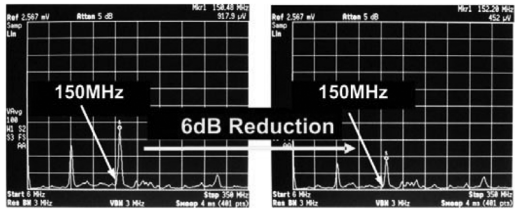

Fig. 11. Supply noise suppression results measured by a spectrum analyzer. (left) The noise spectrum before turning on the active decap circuits. (right) The noise spectrum after turning on the active decap circuits. The noise amplitude has been reduced by 6 dB.

IV. Experimental Results

Fig. 11 shows the noise measurement results captured from an Agilent E4407B ESA-E spectrum analyzer. The noise spectrums while the active decaps are on and off are shown respectfully. Noise injection circuits clocked at 150 MHz were used to generate the supply noise. The result shows that the active decap circuits suppressed the supply noise by around 6 dB.

Fig. 12 shows the measured decoupling effects in comparison between the passive and active decaps. The decoupling effect is defined as the supply noise ratio between the two cases where the active decap circuit is on and off. Both LFSR circuits and noise injection circuits were used to generate the noise. The result shows that a 10 pF active decap suppresses more supply noise than an 80 pF passive decap within the bandwidth of the opamp. The measurement results are consistent with the analytical results which predicted a decap boost of around 11×. At higher frequencies, the decoupling performance of the active decap degrades to a decap boost of 4× at 1 GHz according to the

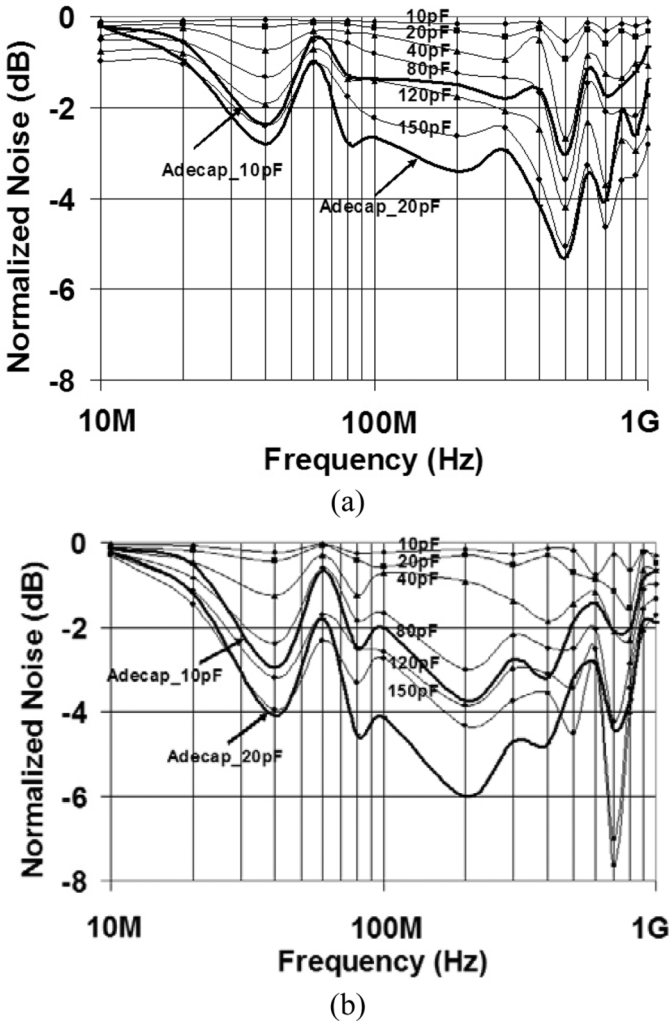

Fig. 12. Measured decoupling effect for noise generated by (a) LFSR circuits and (b) noise injection circuits. Differential noise $V_{\rm DD}$-$G_{\rm nd}$ was measured.

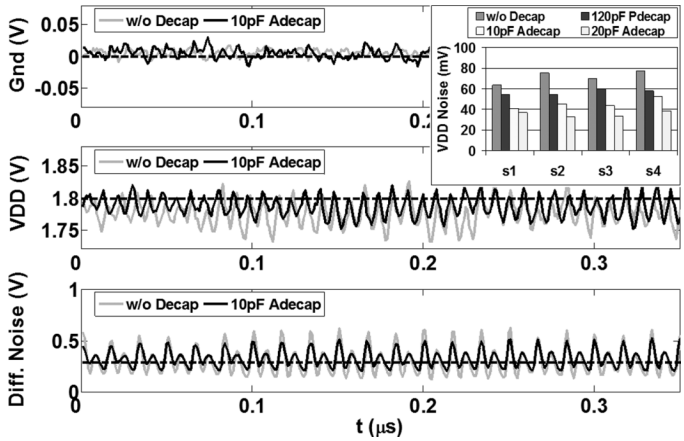

Fig. 13. Measured $V_{\rm DD}$, $G_{\rm nd}$, and $V_{\rm DD}$-$G_{\rm nd}$ waveforms with LFSR circuits operating at 120 MHz. The inset shows the measured $V_{\rm DD}$ noise value at four different sensor locations s1, s2, s3, s4 as illustrated in Fig. 14.

measurement result. Fig. 12 also shows that the decoupling effect for both passive and active decaps increase with frequency up to 700 MHz. At higher frequencies, the decrease of decoupling effects is due to the parasitic resistance in the passive decaps as well as the decrease of the amplifier gain in the active decaps.

Fig. 13 shows the measured supply noise waveforms from the $V_{\rm DD}$, $G_{\rm nd}$ sensors and active decap sensors. LFSR circuits clocked at 120 MHz were used to generate noise in the power supply rails. As seen in the figure, the noises on $V_{\rm DD}$, $G_{\rm nd}$ and the differential noise $V_{\rm DD}$-$G_{\rm nd}$ have all been reduced when active decaps were used. Note that the $G_{\rm nd}$ noise was measured to be less than 50% of the $V_{\rm DD}$ noise. This observation has also been mentioned in [20] and is known to come from the substrate resistance mesh which is connected in parallel to the $G_{\rm nd}$ mesh via the nMOS body contacts. The inset of Fig. 13 shows the $V_{\rm DD}$ noise measured at different sensor locations as indicated in Fig. 14. Similar decoupling effects can be observed from all four sensors.

Fig. 14 (left) shows the floorplan of the test chip. A decap array including both passive decaps and active decaps were placed around the noise generation circuits located at the center of the chip. Sensors were deployed at four different locations to measure the on-chip noise distribution. To test the local supply noise variation, eight LFSR circuits were grouped into blocks A, B, C, and D, as shown in Fig. 14. We activated each block of the LFSR circuits and measured the change in noise magnitude at a particular sensor location, i.e., s2 and s3. Due to the change in distance from the noise source to the sensor location, the noise magnitude varied. Fig. 14 (right) shows the measured local noise. As the noise source moved closer to the sensors s2 and s3, the noise consistently increased, which confirms that a larger noise occurs at a location closer to the noise source. The results in the figure also verifies that a 20 pF active decap works significantly better than a 150 pF passive decap which is the maximum decap amount put in our test chip.

To save the static power consumption of the opamps during idle mode, it is very important to be able to turn off the decap circuits. In this case, the switching speed of the decaps become crucial to achieve the maximum power saving and minimum wake-up performance loss. A test on gating capability of the proposed active decap circuits was performed. An external select signal toggling at 200 kHz with rising and falling time of less than 10 ns was used for decap gating. Fig. 15 shows the measured waveforms of the $V_{\rm DD}$ noise and active decap output during the switching events. It can be seen that the supply noise has been greatly reduced when the active decap circuits are operating. By monitoring the switching of the output node of the active decap circuits, we were able to measure the activation and deactivation delay of these circuits. Measurements show that the active decap can be turned off in less than 10 ns because the select signal cuts off the current source of the opamp leading to an immediate deactivation of the circuit. However, the wake-up time is measured to be around 200 ns. The slow wake-up is due to the large charging period of the differential pair through the high resistive transmission gate as shown in Fig. 4. Fig. 16 shows an improved design with a pulse generator circuit to instantaneously charge up the input transistors during startup. The conductance of the nMOS in the transmission gate has been increased to enable an instant current flow during pulse period. Simulation in Fig. 17 shows the wake-up time for circuits with

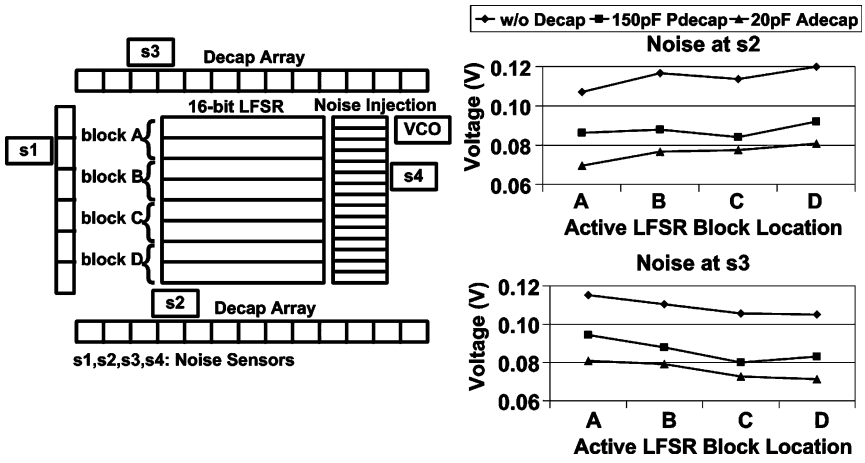

Fig. 14. (left) Floorplan of the test chip and (right) measured noise from sensor 2 and 3 with various active LFSR block location. Each LFSR block contains two 16-bit LFSR circuits.

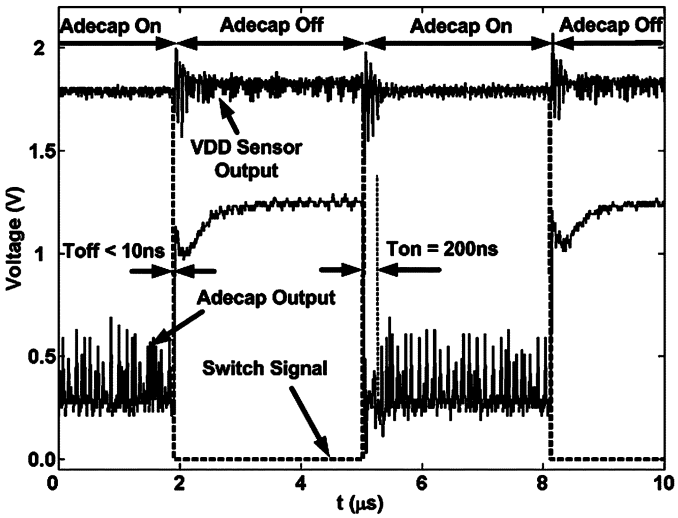

Fig. 15. Measured waveforms of V_{DD} noise and active decap output when turning on and off the active decap circuits.

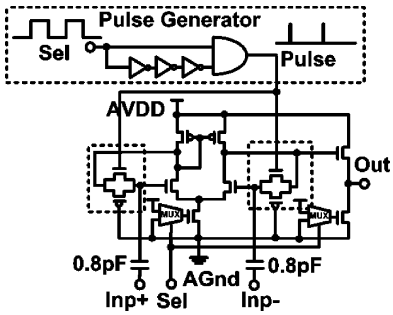

Fig. 16. Schematic of an improved active decap design with pulse generator to reduce the startup time.

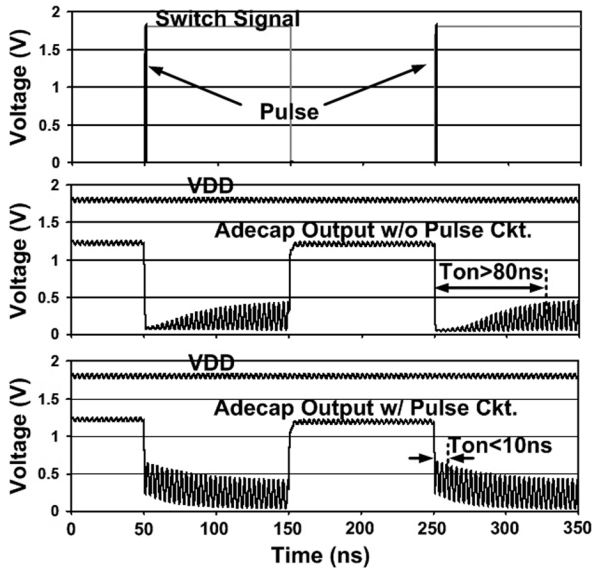

Fig. 17. Simulation results on wake-up time of the active decap circuits with and without the pulse generator circuit. The time for the output node to reach full swing is shortened with the instant pulse.

and without the pulse generator. Compared with the original circuit, it takes much less time for the output of the modified circuit to reach a full swing which is necessary for an effective regulation. Result shows that the wake-up time can be shortened to less than 10 ns by using the improved active decap design.

Fig. 18 shows the die photo of the test chip. The layout of a 10 pF passive decap and an equivalent active decap are also compared. A 40% area reduction has been achieved by using the proposed active decap circuits.

Table II provides a comparison between several previous active techniques. Although the switched decap circuit in [13] has the largest unit area and quiescent current, it has the best area and current efficiency considering the large load capacitance it drives. However, the switched decap circuit is much limited by its regulation frequency of less than 200 MHz while the other two work up to gigahertz range. The active decap reported in [14] has similar circuit specs with the proposed one. However, because it targets at suppressing substrate noise which has less noise magnitude, the active decap in [14] has disadvantages of low output swing, separate biasing scheme and large area overhead for use of supply regulation. Note that the large area overhead from [14] comes from the 10 pF input coupling capacitor which significantly increases the regulator's area consumption.

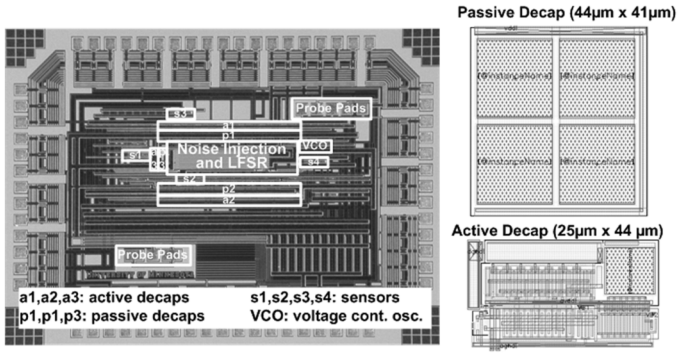

Fig. 18. Micrograph of the test chip (2.7 mm × 1.9 mm) and layout comparison between active decap and equivalent 10 pF passive decap.

TABLE II
COMPARISON OF CIRCUIT SPECS BETWEEN EXISTING ACTIVE REGULATION TECHNIQUES

	Switched decap [13]	Active decap [14]	Proposed one
Application	Resonant power supply noise suppression	Substrate noise decoupling	Mid-freq to high-freq power supply noise suppression
Technology	0.15μm	0.13μm	0.18μm
Bandwidth	N/A	640MHz	500MHz
Cut-off frequency	200MHz	~2.5GHz	2.7GHz
Quiescent current	5mA*	2.6mA	3.8mA
Max. decap gain	12X	9X	11X
Output swing	1.5V	<0.3V	1.0V
Opamp Area	1000x200μm^2*	more than 10pF equiv. decap area*	25x44μm^2 (less than 6pF equiv. decap area)

*** The capacitive load in [13] is about 1000X larger than the other two.**

*** No area information was reported by [14]. However, it has an input coupling capacitor of 10pF which would dominate the total regulator area.**

V. CONCLUSION

Power supply noise poses a serious threat to the scaling of modern VLSI circuits. Conventionally used passive decaps consume large amount of area and leakage power. This paper proposes to use an active decoupling capacitor circuit to improve the efficiency of noise suppression. Based on the Miller effect, an opamp is used to boost the passive decap value. The proposed circuit is designed suitable for digital implementation by using self-biasing schemes and has maximized its output swing to obtain sufficient noise regulation range. Simulations are performed to exam the decap boosting performance under various capacitive load conditions. Results show that the proposed circuit not only can boost the decap value by more than 10× but also exhibits significant advantage of suppressing the dominant resonant noise in an IC chip. To verify the performance of the proposed circuit, a test chip was built in a 0.18-μm CMOS technology. Different types of noise generation circuits and noise sensors were distributed across the chip to generate and measure the power supply noise. Test results confirm a 4-11× boost of decap value up to 1 GHz. Local supply noise measurements show a larger noise at a location closer to the noise source. To reduce the static power consumption, decap gating tests were performed showing that the decap circuits can be switched off within 10 ns and can be restarted within 200 ns. An improved active decap design with a pulse generator is proposed in order to reduce the wake-up time to within 10 ns. Layout comparison shows a total decap area saving of 40% compared with the conventional passive decaps.

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