On-Chip Supply Noise Regulation Using a Low-Power Digital Switched Decoupling Capacitor Circuit

Jie Gu, *Member, IEEE*, Hanyong Eom, and Chris H. Kim, *Member, IEEE*

***Abstract*—On-chip resonant supply noise in the mid-frequency range (i.e., 50–300 MHz) has been identified as the dominant supply noise component in modern microprocessors. To overcome the limited efficiency of conventional decoupling capacitors in reducing the resonant supply noise, this paper proposes a low-power digital switched decoupling capacitor circuit. By adaptively switching the connectivity of decaps according to the measured supply noise, the amount of charge provided by the decaps is dramatically boosted leading to an increased damping of the on-chip supply network. Analysis on the charge transfer during the switching events shows a 6-13X boost of effective decap value. Simulations verify the enhanced noise decoupling performance as well as the effective suppression of the first-droop noise. A 0.13 μm test chip including an on-chip resonance generation circuit and on-chip supply noise sensors was built to demonstrate the proposed switched decap circuit. Measurements confirm an 11X boost in effective decap value and a 9.8 dB suppression in supply noise using the proposed circuit. Compared with previous analog techniques, the proposed digital implementation achieves a 91% reduction in quiescent power consumption with improved tolerance to process-voltage-temperature (PVT) variation and tuning capability for obtaining the optimal switching threshold.**

***Index Terms*—Decoupling capacitor, microprocessor, on-chip regulator, power supply noise, resonance, switched capacitor.**

I. Introduction

ON-CHIP power supply noise has continued to worsen in modern CMOS technologies because the device density and operating current have been increasing rapidly while the supply network impedance has not been able to scale accordingly due to the limited wire resources and constant RC per length [1], [2]. The increased power supply noise causes a larger variation in operating speed leading to a setup or hold time violation as well as an increased clock skew or jitter. It has been shown that the degradation of operating speed due to the supply droop has increased from 6% in a 130 nm process to 9% in a 60 nm technology [3], [4]. Meanwhile, the supply noise overshoot causes reliability issues such as reduced oxide lifetime, aggravated hot carrier injection (HCI) and accelerated negative bias temperature instability (NBTI) effect [5]–[7]. Consequently, reducing power supply noise has become a critical issue for the continuous scaling of CMOS technologies.

One of the dominant supply noise components is the on-chip resonant supply noise which is typically located in the mid-frequency range between 50 and 300 MHz. The resonance of the on-chip supply network is formed by the package inductance and the on-chip decoupling capacitors. Fig. 1 shows a simplified on-chip supply network model and the simulated supply network impedance plotted against the frequency. The supply impedance is measured between the on-chip supply rails as indicated in Fig. 1(a). Note that logic circuits can be modeled as a resistor between $\mathrm{V_{dd}}$ and Gnd for the medium frequency range [8]. A resonant peak in the supply impedance is observed at around 100 MHz. From the frequency response, it can be seen that the resonant supply noise once excited can become an order of magnitude larger than the noise at other frequencies causing severe impact on the circuit performance. In addition to the large magnitude, the following two aspects make the resonant noise the most serious noise component in a power supply network. First, the resonant oscillation typically lasts for tens of clock cycles in a modern gigahertz microprocessor. The long duration of the resonant noise is more likely to cause timing violation compared with high frequency noise which can be shorter than a single clock cycle. Second, because it is formed between the package inductance and the die capacitance, the resonant noise is a global noise which impacts the timing of all the critical paths on a chip. Note that the high-frequency noise is mainly determined by local impedance and is only seen by circuits in the vicinity of the noise source. Thus, the high frequency noise has a very limited timing impact compared with the global resonant noise. For the above reasons, the resonant noise including the so-called first-droop noise caused by a sudden current surge has been considered to be the most devastating supply noise component in modern microprocessors [9], [10].

Conventionally, passive resistance or capacitance has been added to the supply network to damp the mid-frequency supply noise. For example, adding decaps on a chip can reduce the Q-factor of the supply network leading to a reduced resonant noise. Note that the Q-factor of the supply network is given by $1/R\sqrt{L/C}$ where R and L are the series resistance and inductance on the supply paths and C is the total capacitance from on-chip decaps and circuits. However, the large consumption of die area and gate leakage has limited the total amount of decaps that can be deployed on a chip for noise reduction [11]–[13]. Alternatively, passive resistors can also be used to reduce the

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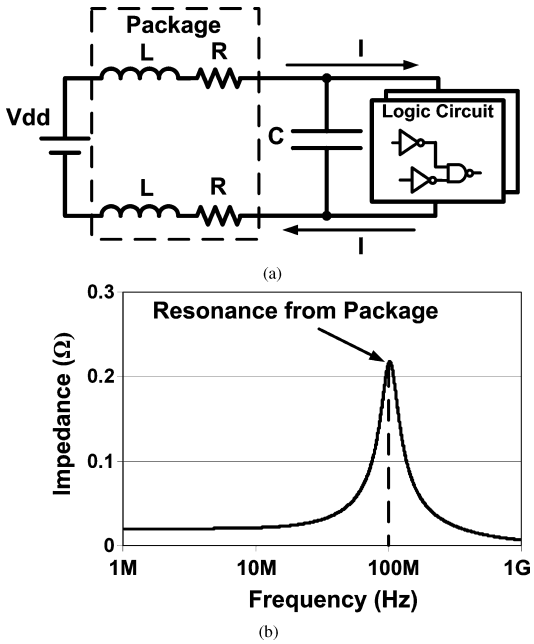


Fig. 1. (a) A simplified on-chip supply network model. (b) Simulated supply network impedance in the frequency domain ($R = 0.01\ \Omega$, $L = 0.05$ nH, $C = 24$ nF).

Q-factor and increase the damping of the supply network. For example, Larsson proposed to place a parasitic resistor in series with a decap to reduce the resonant fluctuation [14]. A mathematical model was provided to estimate the amount of resistance required to provide sufficient damping. However, this technique degrades the performance of decaps especially for the regulation of high-frequency noise. Similarly, Gang proposed to increase the wire resistance of supply network [15]. It was shown that by increasing the supply resistance from 0.01 Ω to 0.06 Ω, the resonant impedance can be reduced from 1.1 Ω to 0.4 Ω which offers a 64% reduction in resonant noise. However, the increased IR droop limits the usefulness of this technique.

In recent years, a number of circuit techniques have been introduced to reduce the resonant supply noise. Hailu proposed a slow clock-ramping technique to reduce the large resonant oscillation when the circuit's operating mode is switched [16]. It uses a frequency divider circuit to gradually raise the clock frequency so as to avoid a sudden frequency transition triggering the resonant oscillation. This technique, however, provides no solution for resonant suppression during normal operation. Rahal-Arabi proposed a clock/data compensation scenario which shows that under the influence of a resonant noise, extra timing margin may actually be obtained by carefully matching the clock delay with the critical path delay based on a signal propagation model [17]. Although the idea is intriguing and shows a potential for reducing the supply noise impact, it is extremely difficult to implement this scheme due to the large number of critical paths in a circuit block. More recently, Xu demonstrated an active damping circuit which monitors and suppresses the resonant noise by clamping the supply overshoot [18]. Although the proposed circuit achieves a 12 dB reduction of the resonant noise, it can only respond to the supply overshoot which limits its use for regulating the first-droop noise. Besides, the analog opamp used for noise detection consumes large quiescent current and

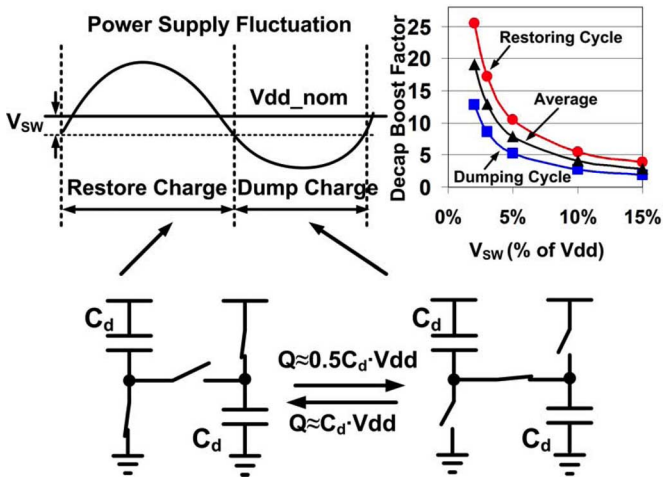


Fig. 2. Principle of resonant noise suppression using switched decaps.

makes the design more susceptible to process-voltage-temperature (PVT) variation.

This work follows the principle of the switched decap circuit proposed by Ang *et al.* to boost decap performance for resonant regulation [19]. Unlike this previous analog implementation, our proposed circuit uses a digital regulation scheme which achieves a significant reduction in power consumption and a high tolerance to PVT variations. The rest of the paper is organized as follows. First, the principle of the proposed circuit is explained with an analytical model for charge transfer to show the theoretical advantages and limits of the proposed circuit. Simulation results will then be provided to show the effectiveness in resonant suppression. Implementation of a 0.13 μm test chip with a resonance generation circuit and on-chip supply sensors will be described followed by measurement results verifying the benefits of the proposed circuit.

II. Principle and Analysis of Switched Decaps

Fig. 2 shows the principle of using switched decaps to boost the amount of charge that is delivered by the conventional decaps. Two passive decaps are connected in parallel during normal condition and serve as conventional decaps. When a supply noise undershoot reaches a switching trigger threshold $\mathrm{V_{SW}}$, the decaps are switched into a series connection where charge is dumped into the supply network. In the supply overshoot cycle, the capacitors are switched back into parallel and charge is restored to the capacitors from the supply network. As a result, the supply oscillation during both undershoot cycle and overshoot cycle can be regulated.

The effectiveness of switched decaps for resonance suppression can be calculated by observing the charge delivered during both the supply undershoot and overshoot periods. Assume that both decaps have a physical capacitance of C_d. The charge delivered during the dumping cycle can be calculated according to the following steps. First, assuming the decaps switch from parallel to series at a voltage of $\mathrm{V_{dd}} - \Delta\mathrm{V_{dd}}$ which is close to the switching threshold $\mathrm{V_{SW}}$, the charge stored in each decap before they switch to a series connection is

$$\mathrm{Q_{swdecap\_before\_dump}} = C_d \cdot (\mathrm{V_{dd}} - \Delta\mathrm{V_{dd}}). \quad (1)$$

After the parallel-to-series switching occurs, the voltage across the two series-connected decaps becomes $V_{dd} - \Delta V_{dd}$. The voltages across each decap become $(V_{dd} - \Delta V_{dd})/2$, which causes the charge stored in each decap to be

$$Q_{swdecap\_after\_dump} = \frac{C_d}{2} \cdot (V_{dd} - \Delta V_{dd}). \quad (2)$$

Note that the amount of charge on two series-connected decaps is the same as the charge on a single decap. Because the two decaps are connected in series, the charge that is delivered into the system during the switching is equal to the change of charge stored on each of the decaps as given from (1) and (2). As a result, the charge delivered into the system from the pair of decaps during the dumping cycle is

$$\begin{aligned} \Delta Q_{swdecap\_dump} &= Q_{swdecap\_before\_dump} \\ &\quad - Q_{swdecap\_after\_dump} \\ &= \frac{C_d}{2} \cdot V_{dd} - \frac{C_d}{2} \cdot \Delta V_{dd}. \end{aligned} \quad (3)$$

Similarly, we can calculate the charge transferred from the supply network to the decaps during the restoring cycle. Assuming that the initial voltage of the series-connected decap is $V_{dd} - \Delta V_{dd}$, the voltage across each decap is $(V_{dd} - \Delta V_{dd})/2$. The charge stored in each decaps before switching is

$$Q_{swdecap\_before\_restore} = \frac{C_d}{2} \cdot (V_{dd} - \Delta V_{dd}). \quad (4)$$

After the series-to-parallel switching, the voltage on each decap is charged back to the initial voltage $V_{dd} - \Delta V_{dd}$. Therefore, the charge stored in each decap becomes

$$Q_{swdecap\_after\_restore} = C_d \cdot (V_{dd} - \Delta V_{dd}). \quad (5)$$

Note that during this process, both decaps are charged up from $(V_{dd} - \Delta V_{dd})/2$ to $V_{dd} - \Delta V_{dd}$ and thus the total charge acquired from the supply network is the sum of the charge gains of the two decaps. This is different from the dumping cycle where the charge delivered into the system equals the charge loss of a single decap. Therefore, the charge acquired from the system from the pair of decaps during the restoring cycle is

$$\begin{aligned} \Delta Q_{swdecap\_restore} &= 2 \cdot (Q_{swdecap\_after\_restore} \\ &\quad - Q_{swdecap\_before\_restore}) \\ &= C_d \cdot V_{dd} - C_d \cdot \Delta V_{dd}. \end{aligned} \quad (6)$$

Note that the above analysis assumes the switching in either direction happens immediately at voltage droop of ΔV_{dd} ($\approx V_{SW}$). In reality, the delay of supply noise sensor will lead to a minor difference in the switching voltages between both directions depending on the noise magnitude and delay of the noise sensor. Thus, the theoretical analysis above needs to be further adjusted based on the real circuit conditions. Comparing (3) and (6), we find that the charges delivered to and from the supply network during the dumping and restoring cycles are different. The charge acquired during the restoring cycle is twice the charge delivered during the dumping cycle. The loss of charge comes from the neutralization of charges in the two series-connected capacitors during the switching. As a result, in each dumping and restoring cycle, the switched decap takes away more charge than it dumps into the supply network, which leads to a loss of energy when supply noise is absent or at a very low level. However, if the switching is set to occur only when a significant enough noise is observed, all the switching power will be used for supply regulation and thus the switching energy loss will be recovered by the excessive energy stored in supply network during the supply overshoot cycle. This indicates that the switching threshold of the switched decap regulator has to be set high enough to minimize a switching power loss while still low enough to perform sufficient noise suppression.

As a comparison, we also calculated the charge delivered by conventional passive decaps. Assuming a supply droop of ΔV_{dd} and two decaps with capacitance of C_d, the amount of charge delivered by two passive decaps is calculated as

$$\Delta Q_{passive} = 2C_d \cdot \Delta V_{dd}. \quad (7)$$

Fig. 2 shows the decap boost factor, i.e.,

$$\Delta Q_{swdecap\_dump}/\Delta Q_{passive} \text{ and } \Delta Q_{swdecap\_restore}/\Delta Q_{passive},$$

as a function of ΔV_{dd} according to (3), (6), and (7). Because the charge delivered by the switched decaps are different in the dumping and restoring cycles, we plot the boost factors during each respective cycle as well as the average boost factor of the two cycles. Results show that for a ΔV_{dd} of 40 mV (3% of V_{dd}), the effective decap boost is 9X in the dumping cycle, 18X in the restoring cycle and 13.5X on average. The figure also shows that the boost factor increases as the supply noise decreases. This is because the charge delivered from conventional decaps ($= 2C_d \cdot \Delta V_{dd}$) is proportional to the supply noise ΔV_{dd} while the charge delivered from switched decaps ($= C_d \cdot V_{dd}/2 + C_d \cdot \Delta V_{dd}/2$) is almost constant, leading to a larger boost factor for a smaller noise. This implies that to achieve a smaller supply noise, a much larger conventional decap has to be deployed compared with the switched decap. In other words, the switched decap technique becomes more effective at lower supply noise levels. Fig. 2 shows that for a supply noise level of 3% (or 8%) of V_{dd}, a decap boost of 14X (or 5X) can be expected.

The maximum variation from nominal load current that the switched decaps are capable of suppressing can be derived from the amount of charge delivered in the dumping and the restoring cycles in (3) and (6)

$$\begin{aligned} Q_{swdecap\_total} &= Q_{swdecap\_dump} + Q_{swdecap\_restore} \\ &= \frac{3}{2} C_d \cdot V_{dd} + \frac{3}{2} C_d \cdot \Delta V_{dd}. \end{aligned} \quad (8)$$

By equating the total charge in (8) to the charge drawn by the circuit in a single cycle, the maximum amount of suppressible resonant current can be determined. Assuming the load current has a sinusoidal waveform with an amplitude of I_{load} and a period of T, the total variation from the nominal amount of charge drawn by the circuit can be calculated as

$$Q_{load} = \frac{2I_{load} \cdot T}{\pi}. \quad (9)$$

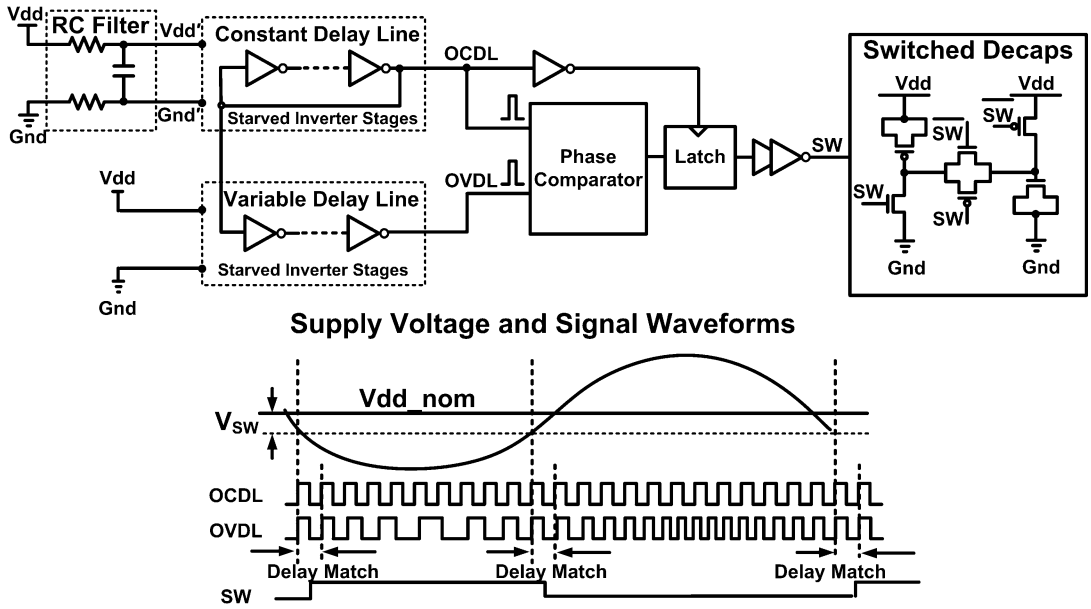


Fig. 3. Schematic of the proposed switched decap circuit with digital resonant detection.

Equating (8) and (9), we can find the amount of load current variation that the switched decap can suppress is

$$\mathrm{I_{load}} = \frac{3\pi C_d \cdot \mathrm{V_{dd}} + 3\pi C_d \cdot \Delta \mathrm{V_{dd}}}{4T}. \tag{10}$$

For example, the maximum load current that the switched decap can suppress for $C_d = 50$ pF and $T = 10$ ns (i.e., 100 MHz resonant frequency) is calculated to be around 14 mA. Equation (10) shows that the maximum load current increases as the frequency goes up because the total charge that the switched decap can deliver is constant while the charge required by the circuit decreases with increased frequency. Note that the decap boost factor in Fig. 2 does not change with frequency because a similar trend also applies to the passive decaps. Equation (10) implies that when designing the switched decap regulator, the load current variation has to be first determined so that the switched decap C_d can be chosen accordingly to provide sufficient regulation.

III. Proposed Digital Switched Decap Regulator

Fig. 3 shows the schematic of the proposed switched decap regulator with a digital resonant detection scheme. The noise detection is realized by comparing the delay of a constant delay line (CDL) and a variable delay line (VDL). The CDL forms a ring oscillator with a frequency of 2 GHz to continuously trigger the comparison. The supply of the CDL $(\mathrm{V_{dd}}')$ is low-pass filtered so that the delay is insensitive to supply noise above 10 MHz which is the low cut-off frequency of our resonant regulation. The supply of VDL is directly connected to the noisy $\mathrm{V_{dd}}$ so its delay varies with supply fluctuations. Layouts of CDL and VDL are identical to minimize any systematic mismatches due to layout differences. In the absence of supply noise, the CDL runs slower than the VDL due to the DC supply droop through the RC filter of the CDL. When the supply droop on VDL is equal to the DC supply droop $\mathrm{V_{SW}}$ $(= R \cdot \mathrm{I_{DC}})$ of the CDL, both circuits run at the same speed and a switch signal SW is issued by the phase comparator to trigger the switching of the decaps. When supply voltage rises above $\mathrm{V_{dd}} - \mathrm{V_{SW}}$, the switched decaps return to a parallel configuration to restore charge. Fig. 3 also shows the signal waveforms for the above operation. It is worth pointing out that similar noise monitoring schemes using inverter chains or ring oscillators have been used in previous publications. For example, Fischer *et al.* implemented voltage sensitive delay lines to track the critical path delay variation within the die. The delay line output is phase- compared with a reference clock signal to issue a frequency adjustment signal for a dynamic frequency scaling system [20]. Sato *et al.* proposed a supply noise measurement scheme which converts the supply voltage droop into ring oscillator frequency for easy detection and better indication of noise impact [21]. Both previous works require external references (either a reference clock or an ideal power supply) while in our proposed work, the reference delay line CDL is self-contained using a built-in RC filter leading to a simple standalone implementation for "drop-in" decap replacements.

Fig. 4 shows the design of the resistors in the RC filter and the delay stages in the delay lines. The delay elements were implemented using starved inverters to increase their sensitivity to supply noise. A special biasing scheme is used as shown in Fig. 4 to improve tolerance to process variation. Threshold voltages $\mathrm{V_{Tp}}$ and $\mathrm{V_{Tn}}$ are generated from a simple bias circuit and are connected to the gates of the MOS resistors in the RC filter and the footer/header transistors in starved inverters. The overdrive voltages of the MOS resistors in both the RC filter and the starved transistors become $\mathrm{V_{dd}} - \mathrm{V_{Tp}} - \mathrm{V_{Tn}}$. The change of R value $(\propto 1/(\mathrm{V_{dd}} - \mathrm{V_{Tp}} - \mathrm{V_{Tn}}))$ cancels out the change of $\mathrm{I_{DC}}(\propto \mathrm{V_{dd}} - \mathrm{V_{Tp}} - \mathrm{V_{Tn}})$ under variation of threshold voltages $\mathrm{V_{Tp}}$ and $\mathrm{V_{Tp}}$, which leads to a process insensitive $\mathrm{V_{SW}}(= \mathrm{I_{DC}} \cdot R)$. Simulation results in Fig. 5 confirm

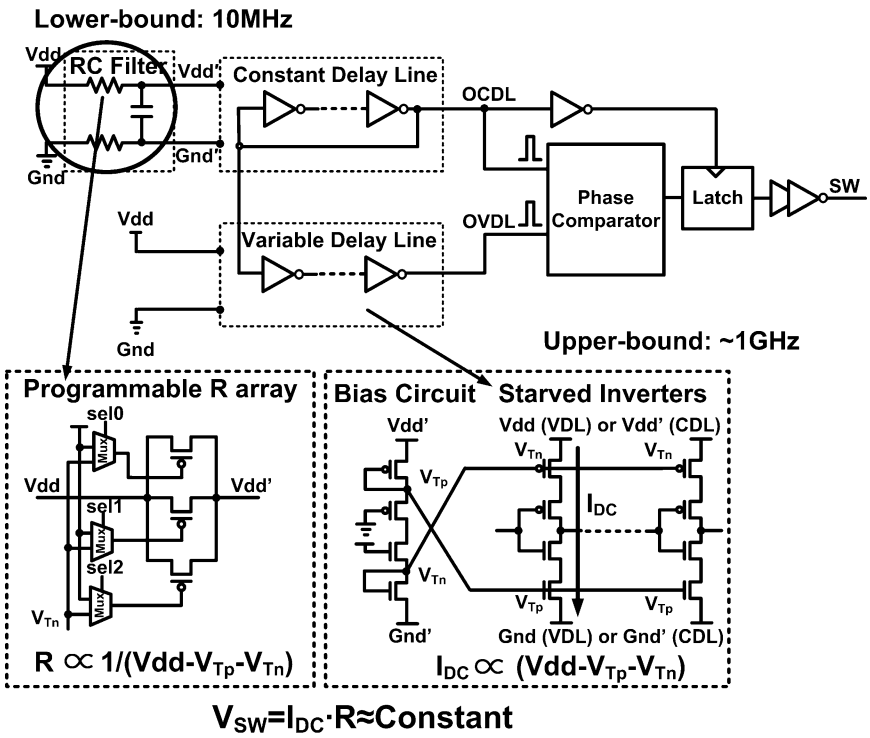


Fig. 4. Schematics of programmable R array for V_{SW} tuning and starved delay element with improved PVT tolerance.

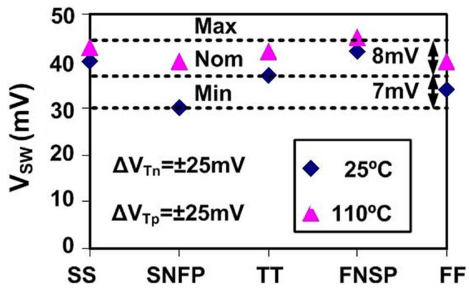


Fig. 5. Simulated V_{SW} change due to process and temperature variations.

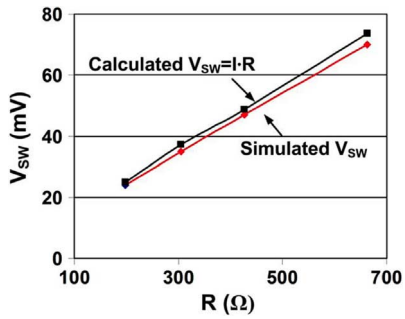


Fig. 6. Simulated and calculated V_{SW} as a function of resistance in the RC filter circuit.

a V_{SW} variation less than 8 mV across different process corners (± 25 mV of V_T) and temperatures (25–110°C).

V_{SW} can be adjusted by changing the number of linear mode PMOS devices that are turned on in the RC filter and changing the resistance value R. The programmable MOS resistor array shown in Fig. 4 enables tuning of the switching threshold. Fig. 6 shows the change of switching threshold V_{SW} when the resistance in the RC filter is adjusted by the programmable R array in Fig. 4. V_{SW} is almost in linear with the R value due to the relationship $V_{SW} = I_{DC} \cdot R$. Although using different number of MOS resistors also changes the I_{DC} slightly due to the small change of IR drop across the inverters, simulations show less than 10% change in I_{DC} even when the R value is doubled. Therefore, by turning on different numbers of MOSFET transistors in the R array, we are able to fine tune the switching threshold of the regulator to achieve the desired regulation performance. Note that reducing the R will raise the lower bound of the detection frequency and therefore should be limited to the extent that it will not degrade the sensitivity of supply noise inside the passband.

The high cut-off frequency of the resonant detection circuit is determined by the delay of VDL and the low-pass filter formed from the header/footer transistors and the junction and parasitic capacitance connected to the header/footer transistors in each delay stage. The high cut-off frequency is simulated to be around 1 GHz. This value can be further reduced by adding a small capacitor between the footer and header transistors on the starved inverters to filter out the high frequency noise. Simulations show that using a 0.15 pF capacitor can bring the upper cut-off frequency further down to 500 MHz. It is also important to mention that the switch sizes in the switched decaps need to be carefully selected. Too large switch sizes can lead to an instantaneous delivery of large current causing a supply overshoot. In essence, the switches and decaps form another low pass filter which constrains the response of the regulator within its target frequency range. Therefore, the switch size should be matched with the decap values to provide an upper bound of frequency response of the regulator.

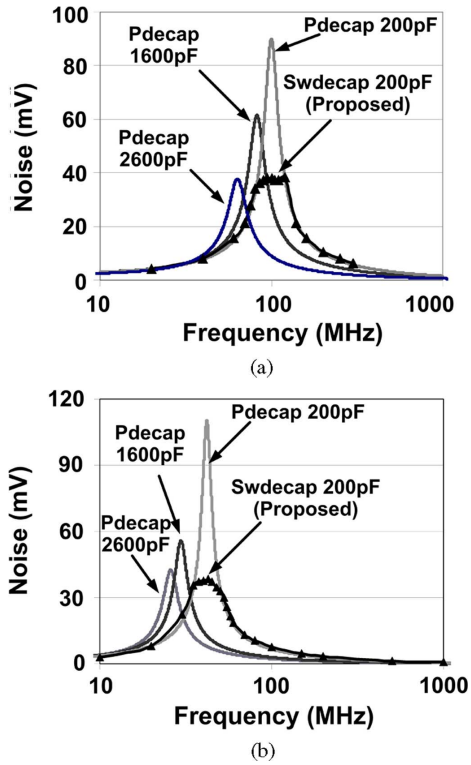


Fig. 7. Simulated decap performance for conventional and proposed schemes.

Fig. 7(a) and (b) show the simulated noise suppression performance of the conventional passive decap and the proposed switched decap at two different supply configurations with resonance at 100 MHz and 40 MHz, respectively. The configuration in Fig. 7(a) has $L = 1.5$ nH, $C = 1.69$ nF, $R = 0.28\ \Omega$ and represents a more typical supply impedance found in high performance chips. The configuration in Fig. 7(b) has $L = 9$ nH, $C = 1.69$ nF, $R = 0.28\ \Omega$ and represents the supply impedance in our test chip. Note that the L, R and C values above are for the total supply path including $\mathrm{V_{dd}}$ and GND paths (i.e., 2L, 2R and C in Fig. 1(a)). The large inductance in our test chip is due to the limited number of pins assigned for power supply and a larger-than-expected package inductance. Both Fig. 7(a) and (b) show similar decoupling performance using the proposed switched decap circuit. For example, at 40 MHz, a 200 pF switched decap offers a 62% (or 8.4 dB) reduction of resonant noise compared with that for a 200 pF passive decap and a 28% reduction of resonant noise compared with that for a 1600 pF passive decap. Fig. 7 also shows that a 2600 pF passive decap has to be deployed to the supply network to obtain the a similar level of resonant suppression as a 200 pF switched decap, rendering a 13X boost of decap value which is consistent with the theoretical analysis in Section II. The noise at high frequencies is larger for the proposed circuit compared with the equivalent conventional decaps because of the less effectiveness of the proposed circuit at non-resonant frequency range. As a solution, a combination of switched decaps and passive decaps can be used to regulate supply noise in a wide frequency band.

Fig. 8 shows the simulated damping performance for the first-droop noise during a circuit's start-up using the same setup as

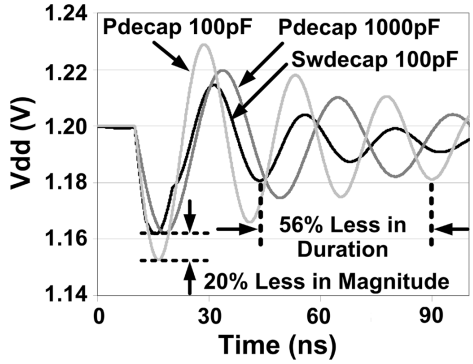


Fig. 8. Simulated first-droop regulation during circuit's wakeup. Noise magnitude and duration are both reduced using the proposed switched decap circuit.

Fig. 7. A 1 GHz clock was instantly activated to emulate a circuit wakeup from sleep mode. The sudden spike in on-chip current triggered a resonant oscillation. Similar to previous results, the switched decap outperforms passive decaps in regulating the first-droop noise.[1] A 10X boost in decap value from the switched decap is observed with a 20% reduction in noise magnitude and 56% reduction in resonant duration compared to that without the switched decaps.

The stability of the regulated power supply system was analyzed using the feedback control system model shown in Fig. 9(a). We assume that the switched decap regulator and the power supply system form a linear timing invariant (LTI) system, in which Nyquist criterion or Bode Plot can be used for stability verification [22]. However, it is important to understand that the proposed regulator is in principle non-linear and thus satisfying the Nyquist criterion does not fully guarantee the stability of the system but only serves as an approximate analysis. In Fig. 9(a), the summation of the excitation current and regulation current is fed into the power supply network to generate the supply noise. The supply noise passes through a bandpass filter and the detection circuit within the switched decap regulator to conditionally generate the regulation current. Assuming the supply noise is always larger than the $\mathrm{V_{SW}}$, which is the condition that the regulator is triggered, as frequency moves away from resonant frequency, the exciting current $\mathrm{I_{excite}}$ must increase proportionally to $\mathrm{Z_{res}/Z}$ to maintain the significant noise level $\mathrm{V_{SW}}$ where $\mathrm{Z_{res}}$ is the impedance at resonant frequency and Z is the impedance at the measured frequency. Thus the exciting current has to increase more than a decade to maintain the noise level higher than $\mathrm{V_{SW}}$. Since the regulation current $\mathrm{I_{reg}}$, which is relatively constant, is set to be approximately equal to $\mathrm{I_{excite}}$ at resonant frequency, $\mathrm{I_{reg}}$ can become a decade smaller than $\mathrm{I_{excite}}$ at higher frequencies. In other words, the open loop gain of the feedback system is much smaller than 1 at higher frequencies than resonant frequency leading to a stable condition for the system. Note a sinusoidal

[1]Although the proposed regulator is capable of regulating overshoot noise in a continuous supply oscillation, it does not respond to the "first-overshoot" noise which may be triggered by a sudden decrease in circuit activity. This is because the switched decaps are already connected in parallel which inhibits them to draw additional charge from the supply network. In cases where the "first-overshoot" noise is critical, a separate switched decap regulator could be deployed just to respond to the excess overshoot noise. This is beyond the scope of our work and would require a separate investigation.

excitation current is assumed in this analysis. A more complex waveform can be decomposed into sinusoidal signals with various frequency components and can be analyzed in the same way given our assumption of LTI system. Fig. 9(b) and (c) provide a computational current gain and phase margin using Matlab based on the transfer function models of each functional block including power supply network, band-pass filter and switch decap regulators. The current gain quickly drops from 1 to less than 0.1 as the frequency moves away from resonance. The phase degradation comes from three main resources, i.e., band-pass filters, noise detection sensor delay from regulator, and phase lag from the power supply network. Each of the phase lag component has been modeled in the transfer function of the corresponding block. As a result, the phase margin becomes 60 degree at 400 MHz where the gain has dropped to 0.03. Hence, according to Nyquist criterion, the system is stable. As mentioned previously, a more advanced analysis using non-linear control theory may be necessary to provide a complete theoretical proof of the system's stability. However, the following observation and assumption can make the Nyquist criterion method viable for our stability analysis. Since the current delivered by the proposed regulator is only enough to compensate the excitation current at the resonant frequency, which is typically orders of magnitude smaller than the current at higher frequencies, disturbance from incorrect switching of the proposed regulator at higher frequencies will not bring the power supply system into an unstable condition. Note that the change in supply impedance from the decap switching has been ignored in the stability analysis because the maximum switched decap is 300pF while the intrinsic decap on the chip is more than 1.7 nF.

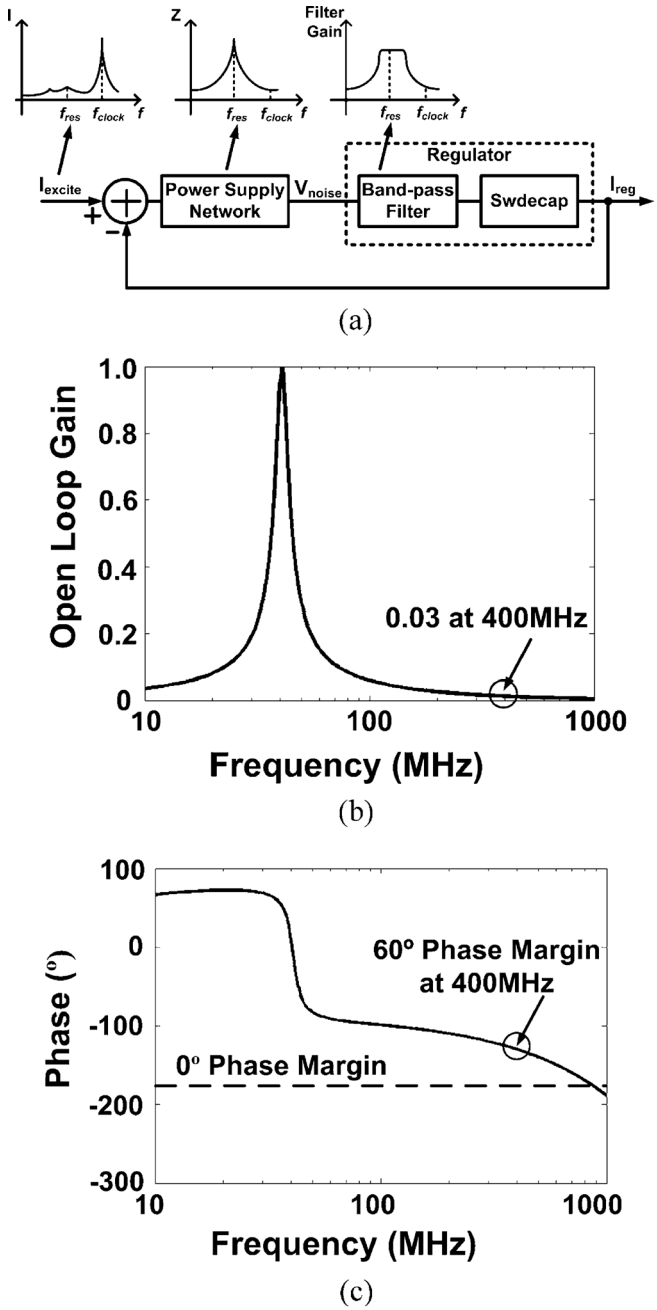


Fig. 9. Stability analysis of the regulator. (a) Block diagram of the feedback control loop of the power supply system with the proposed regulator; (b) Open loop gain of the system; (c) Open loop phase of the system.

IV. Test Chip Implementation

A test chip was fabricated in a 1.2 V, 0.13 μm CMOS process to demonstrate the proposed switched decap circuit. Fig. 10 shows the test chip organization. Two types of noise generation circuits are deployed on the test chip; a resonance generation circuit and a noise injection circuit. The resonance generation circuit is designed to emulate the resonant excitation during the operation of a realistic microprocessor block. It contains four 16-bit multipliers and a clock pattern generator. The clock pattern generator can produce a gated clock which contains noise components at frequencies lower than the fundamental clock frequency to induce the resonant supply noise. A 16-bit clock code is scanned into the shift register to set the gated clock pattern. A '1' passes a clock pulse while a '0' masks the clock pulse. When a clock is passed to the multipliers, one of the inputs of the multipliers toggles between input data A and input data B which leads to the execution of the multiplication operation. Each of the four multipliers draws about 25 mA current and can be selectively turned on so as to adjust the generated noise magnitude. Fig. 11 shows the simulated power spectral density for different gated clock patterns. A '0101010101010101' produces a sub-harmonic noise at 1/2 of the original clock frequency while a '0000111100001111' produces sub-harmonic at 1/8 of the clock frequency. When a sub-harmonic hits on the resonant frequency, the resonant noise will be excited. To test the noise reduction effect at different noise frequencies, we also implemented a simple noise injection circuit which has transistors connected between the $\mathrm{V_{dd}}$ and Gnd to generate supply noise at a given clock frequency. The switched decap is implemented using MOS capacitors. Three 50 pF decap pairs are deployed rendering a total of 300 pF switched decaps. Each pair of decaps can be activated for switching or deactivated as normal passive decaps. The effective switched decap values can be selected between 100 pF, 200 pF and 300 pF to evaluate the impact of load decap on noise reduction. Note that using distributed switched decaps with smaller granularity helps reduce the charge loss in the long interconnects between the decaps. However, the area

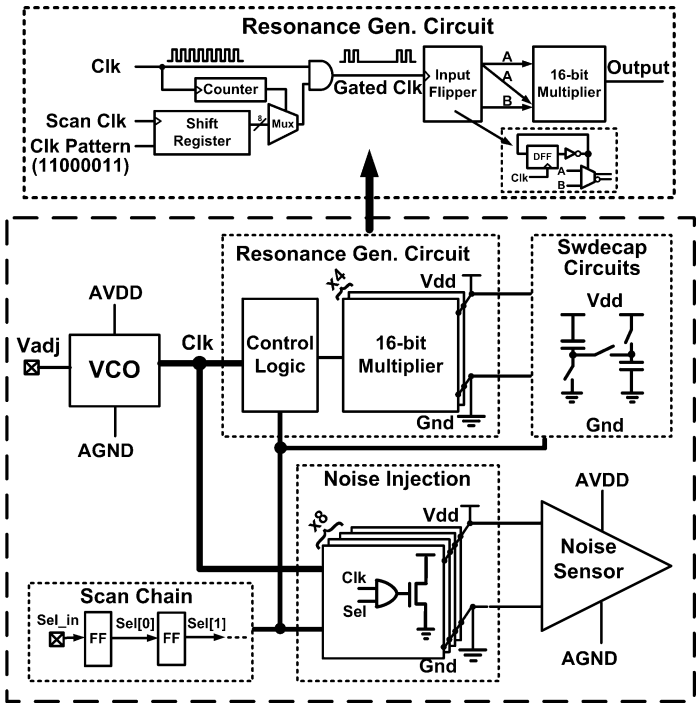


Fig. 10. 0.13 μm switched decap test chip organization.

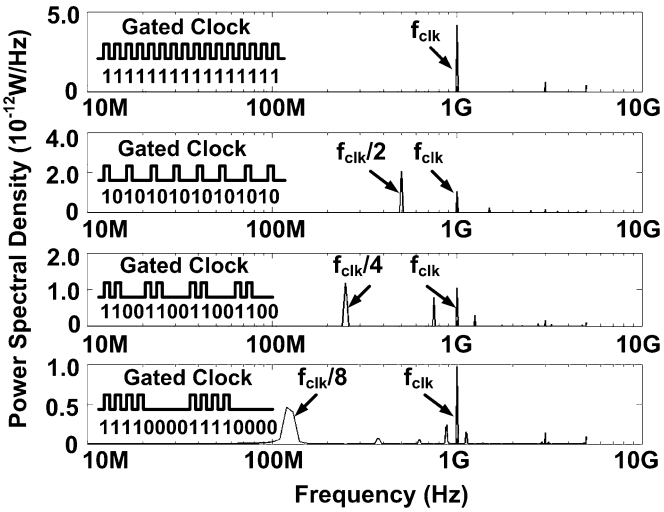


Fig. 11. Simulated power spectrum density from different clock patterns generated by the resonance generation circuit.

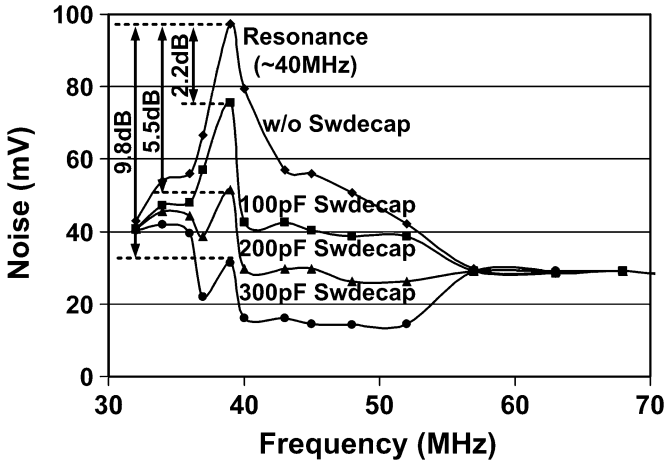


Fig. 12. Measured supply noise in frequency domain near resonant frequency.

overhead for routing the switch signals becomes larger in this case. Because the switching of decaps happens at a relative low speed, a large decap granularity has been chosen in our test chip to alleviate the routing complexity of the switching signal. The decap switches have a dimension of 80 μm/0.12 μm for PMOS and 40 μm/0.12 μm for NMOS. To measure the local differential supply noise $\mathrm{V_{dd}}$-Gnd, an on-chip supply noise sensor with a 4 dB gain and 900 MHz bandwidth was implemented using a differential operational amplifier [23]. The noise sensor and an on-chip VCO share a clean supply voltage AVdd and AGnd for testing purposes while all other circuits use a common noisy digital $\mathrm{V_{dd}}$ and Gnd.

V. Experimental Results

Fig. 12 shows the measured noise magnitude in the frequency domain for switched decaps with different load values. A resonant noise is observed at around 40 MHz which is lower than the resonant frequency in a typical microprocessor due to the larger than expected inductance coming from the package and limited pins assigned for the power supply. Despite the lowering in the resonant frequency, the noise is still effectively reduced because of the sufficiently low cut-off frequency ($\sim$10 MHz) of the switched decap circuit. The results in Fig. 12 show a 2.2–9.8 dB reduction of resonant supply noise using 100–300 pF switched decaps compared with the situation without switched decap regulation, in which case, all the 300 pF switched decaps serve as conventional passive decaps. Table I summarizes the measured

TABLE I
SUMMARY OF MEASURED DECOUPLING PERFORMANCE

Swdecap Value	Resonant Suppression	Equiv. Passive Decap	Decap Boost	Equiv. Damp. Resistance
100pF	2.2dB	500pF	5X	0.1Ω
200pF	5.5dB	1500pF	7.5X	0.4Ω
300pF	9.8dB	3500pF	11X	1Ω

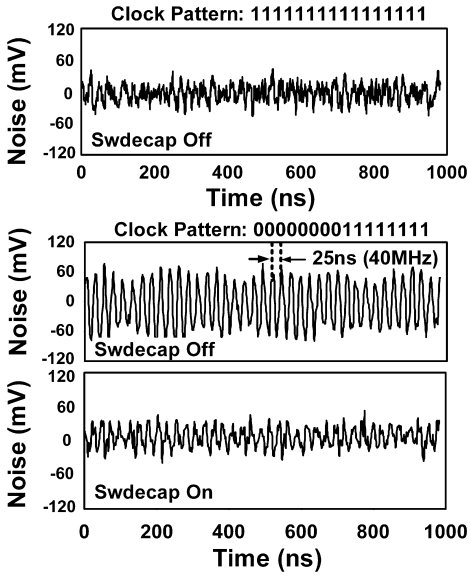


Fig. 13. Measured supply noise waveforms for two clock patterns.

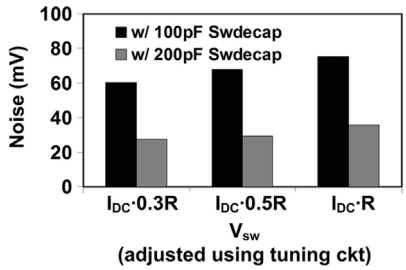
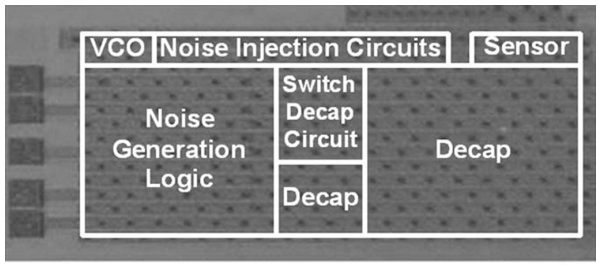


Fig. 14. Measured resonant supply noise for different switching thresholds.



Technology	0.13μm CMOS
Quiescent Current	0.54mA
Regulator Area (w/o decap)	100μmx70μm
Regulator Area (w/ 300pF decap)	190μmx220μm
Area of Noise Generation Logic	320μmx360μm
Total Die Area	0.9mmx1.8mm

Fig. 15. Test chip die photograph and a summary of circuit specs.

performance of the proposed switched decap circuit. For comparison, simulations are performed to find out the amount of conventional passive decaps and damping resistance which can achieve the same noise suppression effect. A 5–11X decap boost has been achieved using the proposed circuit leading up to 89% decap area saving when compared to a passive decap having the same noise suppression effect. The decap boost factor also improves with a larger switched decap value because the smaller supply noise with a larger decap makes the decap boost factor go up as shown in Fig. 2. A 1 Ω (or 0.1 Ω) damping resistor is needed to offer the same damping effect as a 300 pF (or 100 pF) switched decap. It is clear that the excessive IR droop penalty from the large damping resistor is not imposed in the proposed switched decap circuit. Note that the measurements reveal that the Q factor in our test chip is a little larger than that in a typical microprocessor due to a larger inductance in our test chip. However, the conclusion on the effective decap boost from the proposed switched decap regulator will not change under a different Q factor because the boost only depends on the charge stored on the switched decap and is independent of the Q. Therefore, our conclusion of 5X to 11X decap boost will still be valid with different power supply configurations.

Fig. 13 shows the measured noise waveforms when a single 16-bit multiplier was operated at 625 MHz. A clock pattern of '1111111111111111' only contains noise at the fundamental clock frequency and thus only produced a small noise magnitude without any resonant component. A clock pattern of '0000000011111111' however, excited the resonance at around 40 MHz ($\approx$ 625 MHz/16) and thus produced a much larger noise magnitude as shown in the figure. With a 200 pF switched decap activated, the resonance noise was reduced by 44% (i.e., 5.5 dB suppression).

Fig. 14 shows the measured resonant noise magnitude by varying the R value in the RC filter circuit. As we turned on more resistors in the RC filter circuit, the noise suppression performance was improved because of the reduced switching threshold. Measurements also show that the resultant noise magnitude is not directly proportional to the R value or V_{SW}. This is because the noise suppression performance is mainly determined by the value of the deployed switched decaps rather than the switching threshold V_{SW}.

Fig. 15 shows the die photo and chip specifications. Owing to the digital implementation, the measured quiescent power consumption was only 0.65 mW (0.54 mA $\times$ 1.2 V) leading to a

TABLE II
COMPARISON BETWEEN PROPOSED SWITCHED DECAP CIRCUIT AND A PREVIOUS ACTIVE DAMPING TECHNIQUE

	Active Damping Technique [18]	**This Work**
Technology	90nm	130nm
Nominal Supply Voltage	1.2V	1.2V
Quiescent Current	2.42mA	0.54mA
Suppressible Load Current (evaluated at 100MHz)	8.71mA (3X the quiescent current)	33mA (61X the quiescent current)
Regulator Area	59x20μm^2	190x220μm^2 (w/ 300pF swdecap)
First Droop Regulation	No	Yes
Analog Opamp	Yes	No

91% power saving compared to the previous analog design in [19] which consumed 7.5 mW (5 mA $\times$ 1.5 V). The dynamic power consumption of the proposed regulator is simulated by spice to be 1.1 mW at 40 MHz for a 100 pF load capacitance and 4.4 mA load current. This power consumption is simulated when the switched decap operates continuously at each switched cycle and is calculated by measuring the difference between the charge withdrawn from the power supply system and the charge delivered from the decaps. For smaller load currents, the dynamic power consumption will become less due to less switching activities and switched time. Hence the dynamic power is directly related to the load current, operating frequency and the amount of decaps in use. Simulation on dynamic power consumption needs to be performed under different usage scenarios of a particular design. The area of the proposed circuit including the switched decaps was only 11% of a passive decap with equivalent noise suppression. Table II shows a comparison between the proposed circuit and the previous active damping circuit in [18]. A 5X reduction in quiescent power consumption and a 4X larger suppressible load current was achieved while the digital noise detection provides higher tolerance to PVT variations. In addition, our proposed schemes were able to regulate the first-droop noise generated during circuit wakeups. Although the area of the proposed circuit is significantly larger, 90% of the area overhead comes from the load decap which anyways serves as a conventional decap during normal condition to suppress noise.

VI. CONCLUSION

This paper presents a digital switched decap circuit for the suppression of on-chip resonant supply noise. By switching the connectivity of the decoupling capacitors, a boost in effective decap value can be achieved. Measurements from a 0.13 μm test chip confirm an effective decap boost up to 11X which translates into an 89% saving of passive decap area. Owing to the digital implementation, the proposed circuit consumes 91% less quiescent power with a better tolerance to PVT variation compared with the previous analog scheme. The proposed circuit also shows an effective regulation for the first-droop noise and a switching threshold tuning capability to help achieve an optimum tradeoff between performance and switching power.

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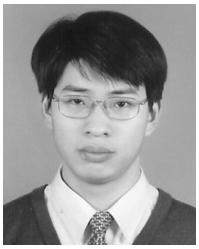

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