# An SRAM Reliability Test Macro for Fully-Automated Statistical Measurements of $V_{min}$ Degradation

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***Abstract*- An SRAM reliability test macro is designed in a 1.2V, 65nm CMOS process for statistical measurements of $V_{min}$ degradation. An automated test program efficiently collects statistical $V_{min}$ data and reduces test time. The proposed test structure enables $V_{min}$ degradation measurements for different SRAM failure modes such as the SNM-limited case and the access-time-limited case. The impact of voltage stress on the time to cell data flip was measured.**

## I. Introduction

Degradation in SRAM minimum operating voltage ($V_{min}$) is becoming a major reliability concern in deeply scaled process technologies. $V_{min}$ of an SRAM cell is limited by several factors such as static noise margin (SNM), writability, and operation frequency that are determined by the relative strengths of all the devices in an SRAM cell. Negative Bias Temperature Instability (NBTI) and Time Dependent Dielectric Breakdown (TDDB), coupled with parametric device mismatch, have attracted attention as major reliability issues conspiring to worsen SRAM $V_{min}$ [1][2][3][4].

NBTI occurs due to the traps at the *Si-SiO₂* interface that release *H* atoms to diffuse into gate oxide, effectively degrading the drive current of PMOS transistors. NBTI is characterized by the increase in the PMOS threshold voltage when the device is stressed, and the degraded threshold voltage partially recovers when the stress is removed. TDDB generates a conduction path through a gate dielectric layer placed under electric stress, heading to parametric or functional failure. TDDB has been a significant concern since voltages are not scaled as gate dielectric thickness, leading to stronger electric fields across gate dielectric layers.

A number of previous literatures have dealt with the impact of NBTI on SRAM $V_{min}$ [3][5][6][7][8]. Li et al. [3] presented the impact of NBTI on device lifetime and SRAM cell operation. It is claimed that NBTI has stronger impact on SRAM cell transition speed than on SNM. Krishnan et al. [5] showed that each transistor in an SRAM cell has different impact on $V_{min}$ degradation. $V_{min}$ sensitivity on NBTI is highest for a strong NMOS and weak PMOS combination. Rosa et al. [6] proposed a methodology for determining tolerable NBTI in PMOS for SRAM cell design. They measured the impact of NBTI on SRAM stability by using "N Curve" method [7]. Device parameters of an SRAM cell are influenced by the layout pattern. Fischer et al. [8] devised a test cell with slight modification from the conventional SRAM cell to minimize the layout pattern dependency of device parameters. The test cell facilitates the direct NBTI measurement in PMOS loads with the marginal pattern dependency. An on-the-fly circuit technique for estimating threshold voltage degradation was proposed [9]. Measured results from individual stressed transistors were used to predict the median value of the threshold voltage shift due to NBTI.

Most of the previous works characterize $V_{min}$ based upon simulation or single SRAM cell measurements. However, a single cell test through manual probing is impractical for obtaining statistical $V_{min}$ data when a large number of cells have to be measured. Array-based structures and automated measurements are indispensible for efficiently and accurately gathering the $V_{min}$ degradation statistics.

In this paper, we present a test macro for fully-automated statistical measurements of SRAM $V_{min}$ degradation induced by NBTI. An automated test sequence collects $V_{min}$ data for statistical analysis and reduces measurement time. Various test strategies were proposed for $V_{min}$ measurements to identify different SRAM fail metrics such as SNM failure and access time failure. The proposed transient measurements also evaluate the speed of cell data flip affected by NBTI.

## II. Impact Of NBTI and TDDB on SRAM $V_{min}$

Two major reliability concerns pertaining to a 6T SRAM cell, namely NBTI and TDDB, and the cell butterfly curves are shown in Fig. 1. The node storing '0' (Q) stresses the PMOS load (M5) causing NBTI that increases the threshold voltage. This lowers the trip point of the right inverter formed with M4 and M5, degrading the cell read stability. Similarly, the node storing '1' (QB) causes TDDB in the NMOS driver (M1) generating a current path through the gate dielectrics. This can be simply modeled by a resistor between the gate and the source as shown in Fig. 1. TDDB in M1 prevents QB from being raised up to VDD due to the pull-down current path. This also pushes down the transfer curve of the right inverter combined with the NMOS driver reducing the cell read stability. As the cell read stability declines, the cell data becomes more likely to flip which leads to an increase in supply voltage with stress.

$V_{min}$ is defined as the minimum supply voltage where an SRAM is operating without failure. Several components such

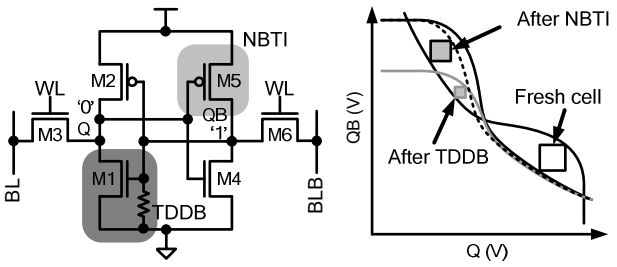


Fig. 1. Impact of NBTI and TDDB on read static noise margin of a 6T SRAM cell

as read stability, writability, and operational frequency restrict the $V_{min}$ of an SRAM cell. $V_{min}$ can be found when one of these becomes lower than a failure threshold. NBTI has different effect on the SNM and the writability. It reduces the read stability, but improves the writability. If the SRAM cell is limited by the read stability, NBTI increases the $V_{min}$. However, if the writability is the limiter for $V_{min}$, NBTI will improve $V_{min}$ due to the better writability after stress. In DC analysis, the failure threshold is set to the point where the SNM becomes zero. However, at a higher clock frequency, the $V_{min}$ can be limited by the access time failure which may happen at a higher supply voltage than the SNM failure point.

## III. Test Macro Design And Measurement Strategy

### A. SRAM Test Macro Design

The simplified architecture of the SRAM test macro is illustrated in Fig. 2. The 2k bit SRAM array consists of 128 rows and 16 columns. The test chip is divided into four test units and each test unit is composed of a mini sub-array (128 rows × 4 columns), power switches, sense amplifiers, and write drivers. Four test units share control circuits, row circuits, output multiplexers, level converters, and output drivers.

Fig. 3 illustrates the core SRAM macro circuits for $V_{min}$ degradation measurements. During a measurement, only the supply of the selected test unit is enabled for stress and a $V_{min}$ test. SRAM cells in the rest sub-arrays are in a fresh mode where all supply levels are grounded to keep SRAM cells free of stress for later evaluations. In the selected array, stress voltage ($V_{STRESS}$) or measurement voltage ($V_{MEAS}$) is connected to the cell supply ($V_{CELL}$) based upon the SRAM $V_{min}$ test modes. $V_{STRESS}$ accelerates NBTI in the stress mode, and $V_{MEAS}$ is used as cell supply voltage during the $V_{min}$ measurement period. To avoid the impact of the supply change on other circuits, $V_{MEAS}$ is only used in SRAM sub-arrays, last stages of wordline drivers, write drivers, and sense amplifiers. The rest SRAM circuits use the nominal supply voltage, $V_{DD\_NOM}$ for reliable operations. Level converters are used for interfacing $V_{MEAS}$ and $V_{DD\_NOM}$.

A $V_{min}$ measurement is executed through regular SRAM write and read operations, decrementing the cell supply voltage from the highest $V_{MEAS}$ level ($V_{MIN\_HIGH}$) to the lowest $V_{MEAS}$ level ($V_{MIN\_LOW}$). The measurement starts by writing

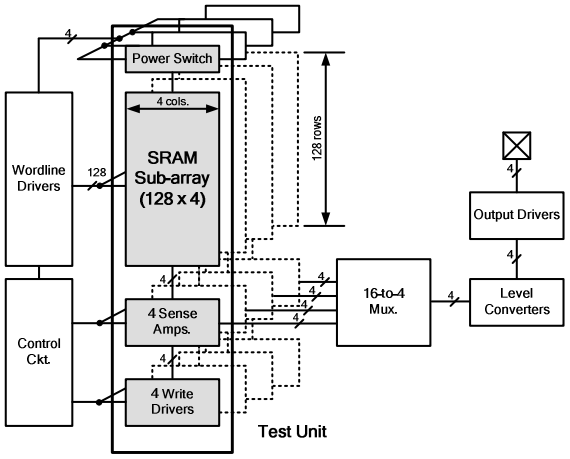


Fig. 2. Test macro architecture.

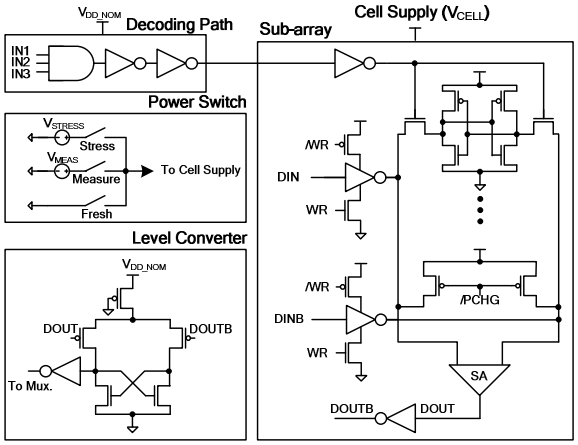


Fig. 3. Core SRAM circuits and different power supply domains for fast transient $V_{min}$ measurements.

data to the selected mini SRAM sub-array. After finishing write operations, stress is applied to accelerate the NBTI by raising the cell supply voltage. During $V_{min}$ measurement interrupts, stress is removed and reading operations are performed with $V_{MEAS}$ controlled by a test program whose sequences will be discussed in section II-B. $V_{min}$ of an SRAM cell is found when the read data is different from the original write data.

### B. Test Sequence for $V_{min}$ Degradation Measurements

Automated measurements effectively gather statistical $V_{min}$ data and reduce test time. Fig. 4 illustrates the fully-automated test sequence for a $V_{min}$ degradation measurement. Each measurement sequence consists of three sub-sequences: an initialization sequence, a stress sequence, and a $V_{min}$ measurement sequence. Before applying stress, write operations are performed as the initialization sequence. The initialization is required to select the devices to be stressed in SRAM cells. After the initialization, the power switches apply $V_{STRESS}$ to the cell supply to stress the devices selected in the initialization sequence. Note that no stress period is needed at the initial fresh $V_{min}$ measurement. After the stress sequence, the $V_{min}$ degradation measurement starts setting the cell supply voltage to $V_{MIN\_HIGH}$. Delay should be inserted after the stress and before the beginning of read operations to wait for the cell supply to settle down. After this delay, the read (or read after write to detect $V_{min}$ for both data) operations are executed sweeping addresses until all the SRAM cells in the selected test unit are accessed. These read operations are repeated decrementing the cell supply voltage from $V_{MIN\_HIGH}$ to $V_{MIN\_LOW}$.

Since stress is removed during the $V_{min}$ measurement sequence, the total measurement time should be kept short for an accurate $V_{min}$ degradation measurement without NBTI recovery. The number of read operations is calculated by multiplying the number of the cell supply levels and the number of addresses as shown in Fig. 4. Raising the clock frequency increases the number of cells that can be measured without NBTI recovery. However, SNM-limited $V_{min}$ usually occurs at a lower supply voltage where the number of measurable cells at a time should be reduced compared to that

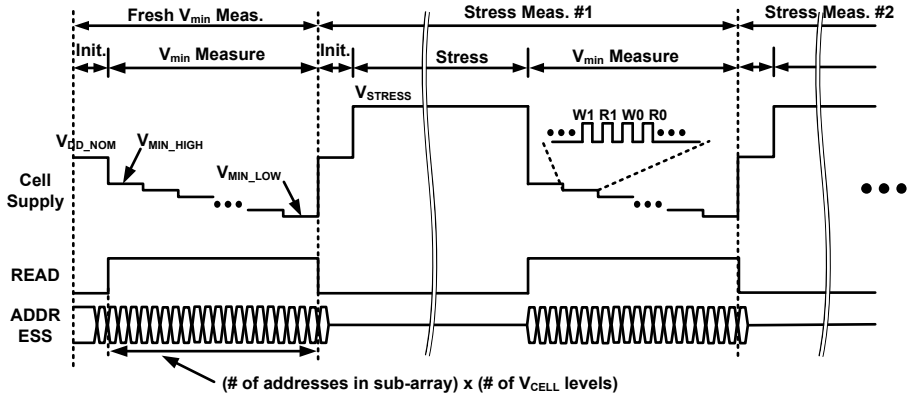


Fig. 4. Automated test sequence for large-scale SRAM stress measurements

in the measurement using a higher frequency clock. If $V_{min}$ is too low enough to slow down SRAM operations below the minimum allowable frequency, the experimental results will include NBTI recovery. Utilizing this frequency dependency of $V_{min}$, the test macro allows $V_{min}$ measurements for different SRAM failure modes.

## IV. $V_{MIN}$ Degradation Measurements

When measuring $V_{min}$ degradation of a single SRAM cell, the initial device parametric mismatch should be considered in measurements. The initial parametric mismatch generates two cell types: a weak '0' cell which has a higher $V_{min}$ for data '0' and a weak '1' cell which has a higher $V_{min}$ for data '1'. In addition to the device mismatch, the direction of $V_{min}$ change should also be deliberated. Stressing a cell storing data '1' increases the $V_{min}$ for data '1' while that of data '0' declines since the weaker strength of the stressed device improves the SNM of data '0'. Fig. 5 demonstrates the measured $V_{min}$ degradation of single SRAM cell with mismatch and data dependency. When stressing a weak '0' cell storing '1', $V_{min}$ improves until the $V_{min}$ values of both data become equal (Fig. 5 (a, b)). $V_{min}$ worsens after this point (Fig. 5 (b)). Obtaining the worst case $V_{min}$ degradation would require a weak '1' cell to be stressed while storing '1'and vice versa for a weak '0' cell (Fig. 5 (c)). For statistical measurements however, the above steps can be omitted since $V_{min}$ distribution for data '1' will be identical to that of data '0' following a Gaussian distribution as device mismatches does. All SRAM cells are stressed with data '1' in our statistical measurements.

When stress is removed, $V_{min}$ quickly drops due to the fast recovering nature of NBTI. Fig. 6 shows the measured $V_{min}$

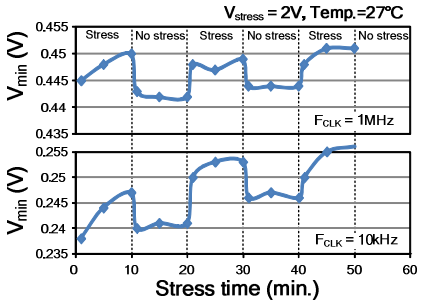


Fig. 6. Measured $V_{min}$ for alternating stress and recovery periods.

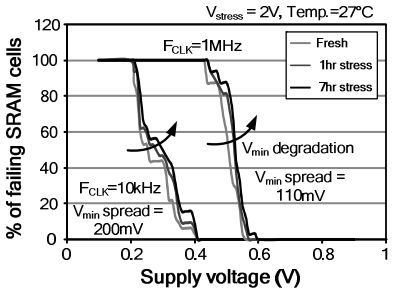


Fig. 7. Measured cumulative $V_{min}$ distribution for two clock frequencies.

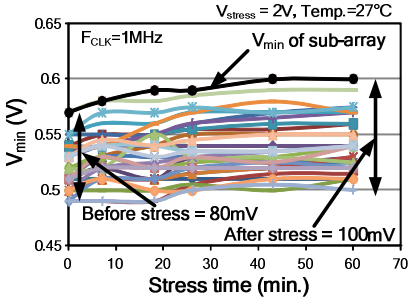


Fig. 8. Measured $V_{min}$ degradation versus stress time for multiple SRAM cells.

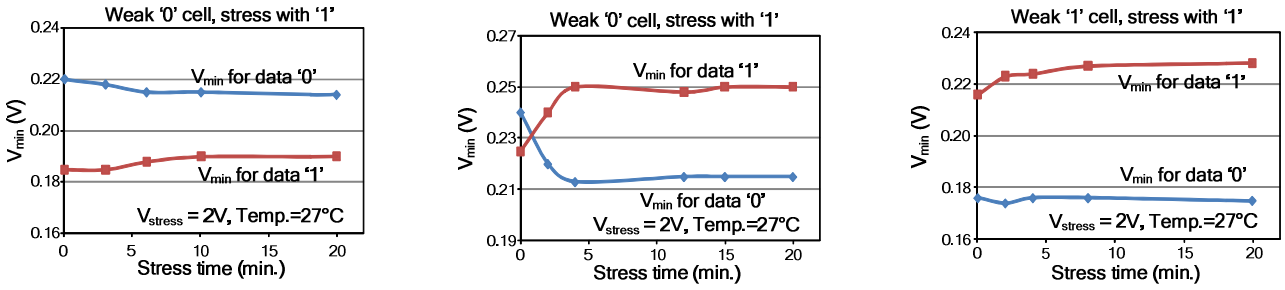


Fig. 5. Single cell $V_{min}$ degradation when stressed with data '1'. If a cell storing data '1' is stressed, $V_{min}$ for data '1' worsens while $V_{min}$ for data '0' improves. The change in $V_{min}$ depends on the initial parametric mismatch as well as the stress mode data: (a) - (b) Weak '0' cells. (c) Weak '1'cell.

for repetitive stress and no stress periods at two different clock frequencies. It can be seen that $V_{min}$ is more sensitive to NBTI at a lower supply voltage where transistor current follows an exponential function of device threshold voltage. $V_{min}$ also depends on clock frequency; $V_{min}$ at 1 MHz is higher than that at 10 kHz. At a higher clock frequency, access time failure happens before an SNM failure does. $V_{min}$ of a single cell can be sampled within a few microseconds so the measurement results in Fig. 5 and 6(top) are free of unwanted NBTI recovery.

Fig. 7 illustrates the cumulative distribution function (CDF) of the measured SRAM failures. The $V_{min}$ distribution using a 10 kHz clock frequency is 90 mV wider than that of 1MHz clock frequency since the SRAM is operating in the sub-threshold region where device current is an exponential function of threshold voltage. Fig. 8 shows the $V_{min}$ degradation measured from 32 SRAM cells. For a 2.0 V stress voltage, a 30 mV degradation in $V_{min}$ was measured after one hour of stress. The $V_{min}$ spread is 80mV prior to stress and 100mV after stress.

The SNM failure determines $V_{min}$ at a low input clock frequency. Since the SNM failure flips the SRAM cell data, the original data does not recover by increasing the cell supply level. Fig. 9 (left) shows waveforms when the SNM failure occurs. However, access time can also limit $V_{min}$ at a higher clock frequency. In this case, cell data survives even though a SRAM operation fails. The original cell data is observed by increasing the cell supply level (Fig. 9 (right)).

Measuring the speed of data flip is informative in estimating the amount of NBTI. This information can also be used to prevent the data flip and improve $V_{min}$ by controlling the wordline activation time [5]. Fig. 10 demonstrates the speed of data flip affected by NBTI and its measurement results. When a wordline is enabled, the cell node storing data '0' (Q) ascends pulling down the level of QB. This pulls up the level of Q further by strengthening the pull-up and weakening the pull-down of the inverter whose output was storing data '0'. Longer stress decreases the time to the data flip since the level of Q rises more declining the level of QB further when the wordline is activated (Fig. 10 (left)). Fig. 10 (right) shows the measured speed of data flip through stress/measurement test. It demonstrates that the data flip points happens earlier as NBTI gets larger. The test chip microphotograph is shown in Fig. 11.

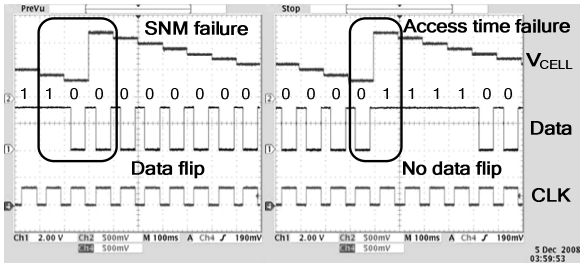


Fig. 9. SNM failure scenario causes a cell data to flip (left). Access time failure scenario causes a transient delay fault (right).

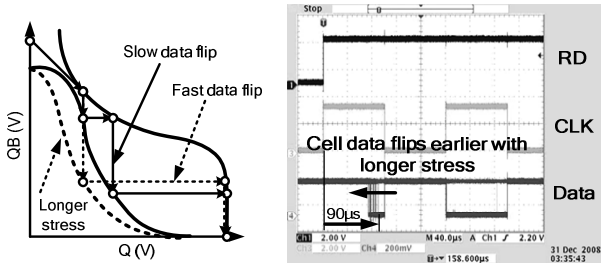


Fig. 10. A longer stress time reduces the time for the cell data to flip which is caused by an SNM failure.

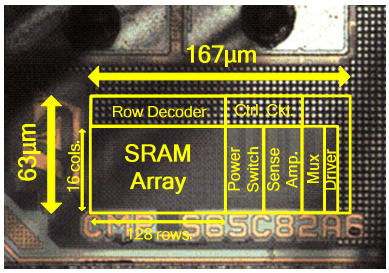


Fig. 11. Microphotograph of the 65nm SRAM reliability test macro.

## V. Conclusions

We have presented an SRAM test macro for fully-automated characterization of $V_{min}$ degradation due to NBTI. An automated test program facilitates large-scale measurements of $V_{min}$ degradation and reduces test time. The proposed test structure can also measure $V_{min}$ degradation from different SRAM failure modes: (a) the SNM-limited case and (b) the access-time-limited case. The impact of NBTI on the time to cell data flip has been measured, which can be used to model the temporal impact of NBTI on SRAM operation. A test chip was implemented in a 1.2V, 65nm CMOS process technology.

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