Circuit Techniques for Enhancing the Clock Data Compensation Effect under Resonant Supply Noise

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Outline

• Resonant Noise and Circuit Timing

• Inherent Timing Compensation Between Clock and Data

• Phase-Shifted Clock Distribution with Proposed Clock Buffer Design

• 65nm Test Chip Measurement Results

• Conclusions
Power Supply Noise

- **IR and Ldi/dt noise:**
  - Typically around 10-15% of nominal $V_{dd}$
- **Lower $V_{dd}$, larger $I_{dd}$, higher $f_{clk}$:**
  - Worsens supply noise with scaling
- **Problems due to supply noise:**
  - Timing, noise margin, reliability, etc
Resonant Supply Noise

Caused by the resonance between package/bonding inductance and die capacitance

Typical resonant frequency is 100-300MHz

Excited by current spike or processor loop operation

Large magnitude, long duration, affects the whole chip
Passive Resonance Suppression

Increase on-chip decap

Increase on-chip resistance

\[ Q = \frac{1}{R} \sqrt{\frac{L}{C}} \]

- Q factor signifies impedance peak
- Penalty for bringing down Q factor:
  - \( \uparrow R \): Extra \( IR \) drop and power
  - \( \uparrow C \): Decap area and leakage overhead

- Can resonant noise be utilized to improve circuit timing?

G. Ji, T. Adv. Packaging, 2005
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Timing Slack in Datapath

- Indicates the timing margin between clock period and datapath delay
- Positive slack means correct operation

\[ \text{Slack} = T_{\text{CLK}} - T_{\text{data}} \]
**Beneficial Jitter Effect: Inherent Timing Compensation Between Clock and Data**

- Traditional analysis considers datapath delay only
- In reality, both datapath delay and clock period vary with supply noise [K.L. Wang, JSSC’06]
**Beneficial Jitter Effect Simulation**

- Inherent timing compensation between clock and data
- 25ps (or 5% $T_{clk}$) slack improvement when considering **beneficial jitter** effect

\[ f_{res} = 200\text{MHz}, f_{cp} = 1\text{GHz}, f_{clk} = 2\text{GHz}, s_{clk} : s_{data} = 0.7:1 \]

65nm, 25°C, 1.2V $V_{dd}$, 12% $V_{dd}$ noise
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Enhancing *Beneficial Jitter* Effect Using Phase-Shifted Clock Distribution

- Datapath delay depends on instantaneous $V_{dd}$ value
- Clock period depends on $V_{dd}$ value *difference* seen by two consecutive clock edges
- Shift the phase of supply noise seen by the clock path
Existing Phase-Shifted Clock Distribution Design

Clock path

- Used in Pentium® 4 processors [N. Kurd, JSSC, 2001]
- Optimize RC value to maximize beneficial jitter effect
- IR drop should be <50mV
  - Requires small R \(\rightarrow\) large C
Proposed Clock Buffer Design

- Proposed buffers also contain built-in \( RC \) filters
- Use phase-shifted supply noise to control header and footer devices
- Current no longer flows through \( R \)
  - Allowing larger resistance to save capacitor area
65nm Test Chip Organization

Clock path block
- Conventional
- RC filtered
- Stacked LVT
- Stacked HVT

5 to 1 MUX

CLKin

Noise injection block
- Noise VCO
- \( N < 31:0 \) to VDD

Clock VCO

VDD

VBIAS

Monitor
Freq. divider

Datapath

CLK

Data counter

Reference counter

Control logic

EXCLK

MODE

2nd MSB

Parallel-to-serial shift-register

P/S

OUT
• 65nm CMOS process, 1.2V supply voltage
• Clock distribution uses H-tree structure
• Long metal wires in clock paths are folded to fit in small die area
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Example Read-Out Waveforms

- Shift-register stores the number of correct samples
- Output of the shift-register is averaged over 512 measurements
Performance with Different Clock Buffer Designs

- Error observed beyond maximum operating frequencies
- 10% performance improvement with phase-shifted clock distribution design

65nm, 118MHz noise, 1.2V, room temp.
Performance versus Noise Amplitude

• Consistent performance improvement with different number of noise injection devices turned-on
• 8-15% performance improvement when 8 or more noise injection devices are turned on

65nm, 118MHz noise, 1.2V, room temp.
Performance versus Noise Frequency

- 8-27% performance improvement for typical resonant noise band (i.e. 100-300MHz)
- Similar improvement with different clock buffer designs
Alternative Clock Modulation Scheme

- Clock generation block is designed to be sensitive to supply noise
- Adaptive clock compensates the datapath delay variation
- Used in Intel® Nehalem processors
Comparison of Different Clock Modulation Schemes

- 17-39ps slack improvement for resonant noise band with adaptive clocking technique alone
- Extra 30-62ps slack improvement by applying the phase-shifted clock distribution design
Conclusions

• Resonant noise is an important concern in power supply network designs

• Inherent timing compensation between clock and data improves timing slack

• Phase-shifted clock buffer designs demonstrated in 65nm silicon
  – Enhance *beneficial jitter* effect
  – 8-27% performance improvement for typical resonant noise band (100-300MHz)
  – 85% area saving compared with existing phase-shifted clock buffer designs