design can be easily expanded to a hierarchical 64-bit adder such that the result will be attained in four cycles.

ACKNOWLEDGMENT

The authors would like to thank National Chip Implementation Center (CIC) for providing the service of the chip fabrication.

REFERENCES

[1] R. X. Gu and M. I. Elmasry, "All-N-logic high-speed true-single-phase dynamic CMOS logic," *IEEE J. Solid-State Circuits*, vol. 31, no. 2, pp. 221–229, Feb. 1996.

[2] J. T. Kao and A. P. Chandrakasan, "Dual-threshold voltage techniques for low-power digital circuits," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1009–1018, Jul. 2000.

[3] V. Kursun and E. G. Friedman, "Sleep switch dual threshold voltage domino logic with reduced standby leakage current," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 5, pp. 485–496, May 2004.

[4] R. Rogenmoser and Q. Huang, "An 800-MHz 1 mm CMOS pipelined 8-b adder using true phase clocked logic-flip-flops," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 401–409, Mar. 1996.

[5] Z. Wang, G. A. Jullien, W. C. Miller, J. Wang, and S. S. Bizzan, "Fast adders using enhanced multiple-output domino logic," *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 206–214, Feb. 1997.

[6] C.-C. Wang, C.-J. Huang, and K.-C. Tsai, "A 1.0 GHz 0.6- μm 8-bit carry lookahead adder using PLA-styled all-N-transistor logic," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 2, pp. 133–135, Feb. 2000.

[7] C.-C. Wang, C.-L. Lee, and P.-L. Liu, "Power-aware design of an 8-bit pipelining asynchronous ANT-based CLA using data transition detection," in *Proc. IEEE Asia-Pacific Conf. Circuits Syst. (APCCAS)*, Dec. 2004, vol. 1, pp. 29–32.

[8] C.-C. Wang, Y.-L. Tseng, P.-M. Lee, R.-C. Lee, and C.-J. Huang, "A 1.25 GHz 32-bit tree-structured carry lookahead adder using modified ANT logic," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 50, no. 9, pp. 1208–1216, Sep. 2003.

[9] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw Hill, 2002.

[10] C.-C. Wang, C.-F. Wu, and K.-C. Tsai, "A 1.0 GHz 64-bit high-speed comparators using ANT dynamic logic with two-phase clocking," *IEE Proc.—Comput. Digit. Techn.*, vol. 140, no. 6, pp. 433–436, Nov. 1998.

[11] J. Lim, D.-G. Kim, and S.-I. Chae, "A 16-bit carry-lookahead adder using reversible energy recovery logic for ultra-low-energy systems," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 898–903, Jun. 1999.

[12] G. Yang, S.-O. Jung, K.-H. Baek, S. H. Kim, S. Kim, and S.-M. Kang, "A 32-bit carry lookahead adder using dual-path all-N logic," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 8, pp. 992–996, Aug. 2005.

Stack Sizing for Optimal Current Drivability in Subthreshold Circuits

John Keane, Hanyong Eom, Tae-Hyoung Kim, Sachin Sapatnekar, and Chris Kim

***Abstract*—Subthreshold circuit designs have been demonstrated to be a successful alternative when ultra-low power consumption is paramount. However, the characteristics of MOS transistors in the subthreshold region are significantly different from those in strong inversion. This presents new challenges in design optimization, particularly in complex gates with stacks of transistors. In this paper, we present a framework for choosing the optimal transistor stack sizing factors in terms of current drivability for subthreshold designs. We derive a closed-form solution for the correct sizing of transistors in a stack, both in relation to other transistors in the stack, and to a single device with equivalent current drivability. Simulation results show that our framework provides a performance benefit ranging up to more than 10% in certain critical paths.**

***Index Terms*—Logical effort, subthreshold logic, ultra low power design.**

I. INTRODUCTION

Due to the robust nature of static CMOS logic, circuits in this technology family can operate with supply voltages below the transistor threshold voltage ($V_{\rm th}$), while consuming orders of magnitude less power than in the normal strong-inversion region. The operating frequency of subthreshold logic is much lower than that of regular strong inversion circuits ($V_{\rm dd} > V_{\rm th}$) due to the small transistor current, which consists entirely of leakage current. The low operating frequency and low supply voltage combine to reduce both dynamic and leakage power, leading to the significant power savings seen in subthreshold designs.

Subthreshold logic holds promise for the growing number of applications in which minimal power consumption is the primary design constraint. Such circuits have received much attention in recent research, and a number of successful designs have been demonstrated. A multiplexer-based SRAM was proposed for subthreshold operation by Wang and Chandrakasan [1]. They also introduced new tiny-XOR circuits and demonstrated their performance in a fast Fourier transform (FFT) processor running at a supply voltage of 180 mV. Kim *et al.* [2] presented a new high-density SRAM system operating down to 200 mV at the ISSCC'07. In [3], Kim *et al.* built an ultra-low-power adaptive filter for hearing aid applications using subthreshold logic. Subthreshold friendly logic styles and massively parallel digital signal processing (DSP) architectures were used in that work to achieve low-voltage operation.

The characteristics of MOS transistors in the subthreshold region are significantly different from those in the strong inversion region. The saturation current, which was a near-linear function of the gate and threshold voltages in the strong inversion region, becomes an exponential function of those values in the subthreshold regime [4]. In this paper, we show that the sizing methods used to obtain maximum performance must be reformulated for use in subthreshold designs due to these different characteristics. In particular, we present a framework

Manuscript received October 22, 2006; revised May 16, 2007.

The authors are with the Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN 55455 USA (e-mail: jkeane@ece.umn.edu; eomxx001@ece.umn.edu; thkim@ece.umn.edu; sachin@ece.umn.edu; chriskim@ece.umn.edu).

Digital Object Identifier 10.1109/TVLSI.2008.917571

for choosing the optimal transistor stack sizing factors in terms of current drivability for subthreshold circuits. A closed-form solution for the optimal sizing of stacked transistors is derived and shown to match simulation results. Our theoretical sizing values closely match those found in simulations with predictive technology model (PTM) [5], [6] devices ranging from 130-nm technology down to the 45-nm node. This sizing method is shown to provide a clear benefit in logic paths containing a large number of stacks where the nodal capacitance is not dominated by the increased device sizes used in our method.

II. Optimal Two-Stack Sizing

A. Optimal Ratio Between Two Stacked Devices

The first step we take in developing the subthreshold stack sizing framework is finding the optimal width ratio between transistors in a stack for maximum drive current. Here, we will present a closed-form expression for the relative sizing of two transistors in a stack, showing that it is beneficial to size up the transistor nearest to the supply rail ($V_{\rm dd}$ for PMOS, ground for NMOS). The starting point is the following pair of current equations for upper and lower transistors as situated in an NMOS stack (so the lower device is connected to ground), excluding the common factors that will cancel out when they are equated:

$$I_U = W_U e^{\frac{(V_{\rm dd}-V_X)-(V_{t0}+\gamma V_X+\lambda_d(V_{\rm dd}-V_X))}{mV_T}}\left(1-e^{\frac{-(V_{\rm dd}-V_X)}{V_T}}\right)$$
$$\approx W_U e^{\frac{(V_{\rm dd}-V_X)-(V_{t0}+\gamma V_X+\lambda_d(V_{\rm dd}-V_X))}{mV_T}} \quad (1)$$
$$I_L = W_L e^{\frac{V_{dd}-(V_{t0}+\lambda_d V_X)}{mV_T}}\left(1-e^{\frac{-V_X}{V_T}}\right). \quad (2)$$

Here, W_U and W_L denote the upper and lower transistor widths, respectively, and V_X denotes the voltage at the node between those devices. The drain-induced barrier lowering (DIBL) coefficient (a negative number) is represented by λ_d and γ is the body effect coefficient. The thermal voltage is represented by V_T, while V_{t0} stands for the nominal threshold voltage. According to simulation results, $V_X \approx 10\%$ of $V_{\rm dd}$. Each V_X term multiplied by the small DIBL coefficient (ranging from roughly -0.01 to -0.2 in current bulk technologies) can then be approximated as $\sim$0. Moreover, note that $e^{-(V_{\rm dd}-V_X)/V_T} \approx 0$. We use the symbol

$$\alpha = e^{\frac{-\lambda_d V_{\rm dd}}{mV_T}} \quad (3)$$

as well as the fact that $m = 1+\gamma$, to further simplify calculations. Rewriting the two current equations and equating them yields the following relationship:

$$\alpha W_U e^{\frac{-V_X}{V_T}} = W_L\left(1-e^{\frac{-V_X}{V_T}}\right). \quad (4)$$

Solving for V_X and using the definition $V_T = kT/q$ gives us

$$V_X = \frac{kT}{q}\ln\left(1+\frac{\alpha W_U}{W_L}\right). \quad (5)$$

We then define $W_T = W_U + W_L$ to eliminate W_L, which results in the following current equation:

$$I_U = I_L = \frac{\alpha W_U(W_T-W_U)}{\alpha W_U + W_T - W_U} e^{\frac{V_{\rm dd}-V_{t0}}{mV_T}}. \quad (6)$$

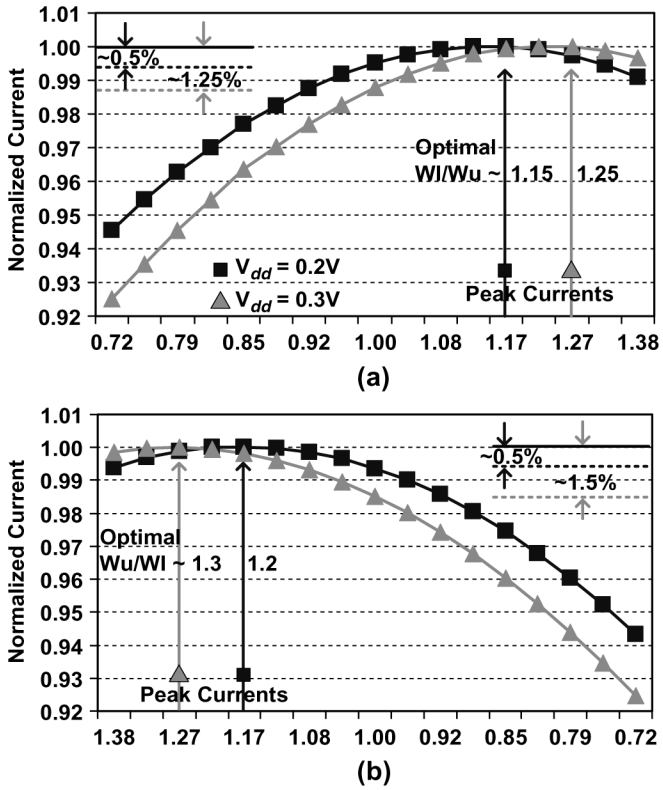

Fig. 1. DC current in stacks of two devices for a range of $\boldsymbol{W_U}$: $\boldsymbol{W_L}$ sizing ratios. The total width of the stacked devices is held constant at 1 $\boldsymbol{\mu}$m. The small benefits derived by using skewed stack sizing are indicated in the upper corners of the plots. (a) NMOS Wl/Wu ratio. (b) PMOS Wu/Wl ratio.

We find the optimal size for W_U by setting $(\partial I_U/\partial W_U)$ equal to zero. Again, using our definition of W_T, we then find the optimal size for W_L. This derivation results in the following equations:

$$W_U = \frac{W_T}{1+\sqrt{\alpha}} \quad (7)$$
$$W_L = \frac{W_T}{1+\sqrt{\alpha}}\sqrt{\alpha}. \quad (8)$$

According to these results, we expect to drive a higher current through the two-transistor stack when the lower device is larger than the upper transistor by a factor of $\sqrt{\alpha}$. For example, with an NMOS stack in 90-nm PTM technology, when using a W_U of 1 μm, the optimal W_L would be 1.23 μm at $V_{\rm dd} = 0.2$ V, and 1.30 μm at $V_{\rm dd} = 0.3$ V. As shown in (3), α is a function of $V_{\rm dd}$, resulting in the different optimal width ratios for different $V_{\rm dd}$ values.

HSPICE simulations using 45–130 nm PTM technology files closely match the results of our derivation and verify that the benefit of using the $\sqrt{\alpha}$ sizing ratio is more pronounced for larger α values (i.e., when the supply voltage is larger). PMOS transistor stacks exhibited the same sizing trends—optimal sizing requires the upper transistor (adjacent to the power supply) to be sized up by a factor of $\sim \sqrt{\alpha}$. Results for 90-nm technology are displayed in Fig. 1, and indicate optimal ratios that are roughly 4% to 6.5% smaller than the theoretical $\sqrt{\alpha}$ factors stated earlier. Due to the small difference in current with the skewed sizing ($\sim$0.5% to 1.5% improvement), we will use a 1:1 width ratio in stacks. This reduces the design complexity for a negligibly small performance penalty.

TABLE I
NMOS STACK SIZING FACTORS

Vdd	Sizing Method	130nm	90nm	65nm	45nm
0.2V	simulation	2.19	2.30	2.42	2.66
	theory	2.39	2.52	2.67	3.04
0.3V	simulation	2.27	2.44	2.64	3.11
	theory	2.50	2.70	2.93	3.57
1.2V	simulation	1.58	1.60	1.63	1.69

TABLE II
PMOS STACK SIZING FACTORS

Vdd	Sizing Method	130nm	90nm	65nm	45nm
0.2V	simulation	2.33	2.48	2.68	3.00
	theory	2.45	2.66	2.90	3.34
0.3V	simulation	2.60	2.85	3.20	3.95
	theory	2.57	2.88	3.28	4.13
1.2V	simulation	1.98	2.08	2.05	2.15

B. Optimal Two-Stack Sizing Factor

After deciding to use a 1:1 ratio for the two devices in a stack, we must find the amount by which they should be sized up to drive the same current as a single transistor. Defining $W = W_U = W_L$ as the size of each transistor in the stack, we can modify (6) as follows:

$$I_U = I_L = \frac{\alpha W^2}{\alpha W + W} e^{\frac{V_{\rm dd} - V_{t0}}{mV_T}} = \frac{\alpha}{1+\alpha} W e^{\frac{V_{\rm dd} - V_{t0}}{mV_T}}. \quad (9)$$

For a single transistor, the current equation is

$$I = W_{\rm eff} e^{\frac{V_{\rm dd} - (V_{t0} + \lambda_d V_{\rm dd})}{mV_T}} = \alpha W_{\rm eff} e^{\frac{V_{\rm dd} - V_{t0}}{mV_T}} \quad (10)$$

where $W_{\rm eff}$ stands for the effective width of this device. From (9) and (10), we have the following relationship:

$$\alpha W_{\rm eff} = \frac{\alpha}{1+\alpha} W \rightarrow W_{\rm eff} = \frac{1}{1+\alpha} W. \quad (11)$$

According to this equation, two stacked transistors should be sized up by a factor of $(1+\alpha)$ in relation to a single device for the same current drivability. Tables I and II display $(1+\alpha)$ stack sizing values from this theory and from simulation results, demonstrating the validity of (11). DC simulations were performed to find the correct sizing for transistors in a stack which is capable of conducting the same amount of current as a single unit-sized device. Sizing factors found in simulations were slightly smaller than those predicted by the theory derived above due to effects not captured by current (1), but the trend with technology scaling is nearly identical in both cases.

Results indicate that stacks need to be sized up by a larger amount in the subthreshold region compared to the strong inversion region. Also note that NMOS stack sizing factors are significantly smaller in strong inversion due to velocity saturation.

III. ARBITRARY STACK SIZES

A. Proof of the Symmetry of the Lowest $n-1$ Device Widths in an n-Stack

Building an extensive cell library based on this stack sizing framework requires an extension of our work to stacks of three or more devices. The derivation for the current equation of a three-stack, which follows a similar method as the derivation in Section II-A gives us the following result:

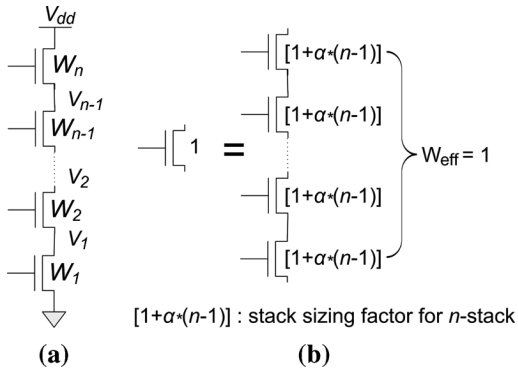

Fig. 2. NMOS n-stack. (a) n-stack notation. (b) n-stack sizing for equivalent width.

$$I = \alpha \left[\frac{(W_T - W_1 - W_2) W_1 W_2}{\alpha (W_T - W_1 - W_2)(W_2 + W_1) + W_1 W_2} \right] e^{\frac{V_{\rm dd} - V_{t0}}{mV_T}}. \quad (12)$$

W_1 and W_2 stand for the widths of the two lower transistors in the stack of NMOS devices (see notation in Fig. 2). W_T is defined as $W_T = W_1 + W_2 + W_3$ and is used to eliminate W_3, the width of the upper device. This equation is symmetric with respect to the widths of the W_1 and W_2 transistors, indicating that the optimal sizes for the lower two devices in the stack are equal. We now extend this finding through a straightforward direct proof, which confirms the symmetry of the lower $n-1$ transistor widths in a general n-stack achieving maximum drive current.

The following equations hold for the drive-current through the transistors in an n-stack

$$I_n = \alpha W_n \beta e^{-V_{n-1}/V_T} = \alpha W_n \beta \nu_{n-1} \quad (13)$$

$$I_{n-1} = W_{n-1}\beta(e^{-V_{n-2}/V_T} - \nu_{n-1}) = W_{n-1}\beta(\nu_{n-2} - \nu_{n-1}) \quad (14)$$

$$\vdots \quad \vdots \quad \vdots$$

$$I_3 = W_3\beta(e^{-V_2/V_T} - \nu_3) = W_3\beta(\nu_2 - \nu_3) \quad (15)$$

$$I_2 = W_2\beta(e^{-V_1/V_T} - \nu_2) = W_2\beta(\nu_1 - \nu_2) \quad (16)$$

$$I_1 = W_1\beta(1 - \nu_1). \quad (17)$$

The v_i variables are shorthand for e^{-Vi/V_T} and β stands for $e^{(V_{\rm dd} - V_{t0})/V_T}$.

Step 1) By setting (16) equal to (17), we can show that

$$\nu_1 = \frac{W_1 + W_2\nu_2}{W_1 + W_2}. \quad (18)$$

Step 2) Next, by setting (15) equal to (16), and solving it for ν_2, we have

$$\nu_2 = \frac{W_3\nu_3 + W_{2\|1}}{W_3 + W_{2\|1}} \quad (19)$$

where $W_{2\|1} = W_2W_1/(W_2 + W_1)$ is called the parallel combination of W_1 and W_2. *Step 2)* is now repeated to move up through the stack until we reach the equation

$W_{n-1}(\nu_{n-2}-\nu_{n-1}) = W_{n-2}(\nu_{n-3}-\nu_{n-2})$. From this we find

$$\nu_{n-2} = \frac{\nu_{n-1}W_{n-1} + W_{\{n-2\|1\}}}{W_{n-1} + W_{\{n-2\|1\}}} \tag{20}$$

where $W_{\{n-2\|1\}}$ is the parallel combination of transistors 1 through $n-2$.

Step 3) Finally, setting (13) equal to (14), we can solve for ν_{n-1}

$$\nu_{n-1} = \frac{W_{\{n-1\|1\}}}{\alpha W_n + W_{\{n-1\|1\}}}. \tag{21}$$

We now have the following current equation:

$$I_n = \alpha W_n \beta \nu_{n-1} = \beta\left[\frac{(\alpha W_n)W_{\{n-1\|1\}}}{\alpha W_n + W_{\{n-1\|1\}}}\right]. \tag{22}$$

Defining $W_T = \sum_{i=1}^{n} W_i$ and substituting for W_n in (22), we get

$$I_n = \beta\left[\frac{\alpha\left\{W_T - \sum_{i=1}^{n-1} W_i\right\}W_{\{n-1\|1\}}}{\alpha\left\{W_T - \sum_{i=1}^{n-1} W_i\right\} + W_{\{n-1\|1\}}}\right]. \tag{23}$$

An examination of (23) shows that the variables W_1 through W_{n-1} appear symmetrically in the expression. Therefore, when I_n is optimized, W_1 through W_{n-1} must have identical values, since setting the partial derivative of I_n with respect to each W_i, for $i = 1$ to $n-1$, will result in a symmetric set of $n-1$ equations.

B. Optimal n-Stack Sizing Factor

Given the symmetry of the lower $n-1$ device sizes, i.e., $W_X = W_1 = W_2 = \cdots = W_{n-1}$, we have the following general form for I_n in an n-stack:

$$I_n = \beta\left[\frac{\alpha\{W_T - (n-1)W_X\}W_X}{\alpha\{W_T - (n-1)W_X\}(n-1) + W_X}\right]. \tag{24}$$

To optimize I_n, we set $\partial I_n/\partial W_x = 0$ to obtain

$$W_X = \frac{(\alpha n - \alpha - \sqrt{\alpha})}{(\alpha n^2 - 2\alpha n + \alpha - 1)}W_T. \tag{25}$$

Using the definition of W_T, i.e., $W_n = W_T - W_X(n-1)$, we get

$$\frac{W_X}{W_n} = \left[\left(\frac{\alpha n^2 - 2\alpha n + \alpha - 1}{\alpha n - \alpha - \sqrt{\alpha}}\right) - (n-1)\right]^{-1} = \sqrt{\alpha}. \tag{26}$$

Thus, we have proven that the $\sqrt{\alpha}$ sizing ratio holds for the general n-stack case.

As in the two-transistor stack case, the scaling factor of $\sqrt{\alpha}$ leads to a trivial performance benefit (e.g., a 0.3% increase in current through a PMOS or NMOS stack in 90-nm technology with a total stack width of 1 μm), so sizing all stacked transistors equally is the best choice in terms of overall design complexity. Using (24) and following the example of (11), we find that each device in an n-stack should then be scaled up by a factor of $[1+\alpha_*(n-1)]$ to set the effective width of the stack equal to that of a single unit transistor (see Fig. 2). Note that all work done here again applies to PMOS stacks in a similar manner. The discrepancies between the larger sizing factors predicted by this theory and those found with simulations become slightly more pronounced as the stack size grows. For PMOS three stacks, the difference stays within the ~4%–7% range, while for large alpha values, NMOS sizing factors are overestimated by up to ~15% due to second-order effects not captured in (1) and (2).

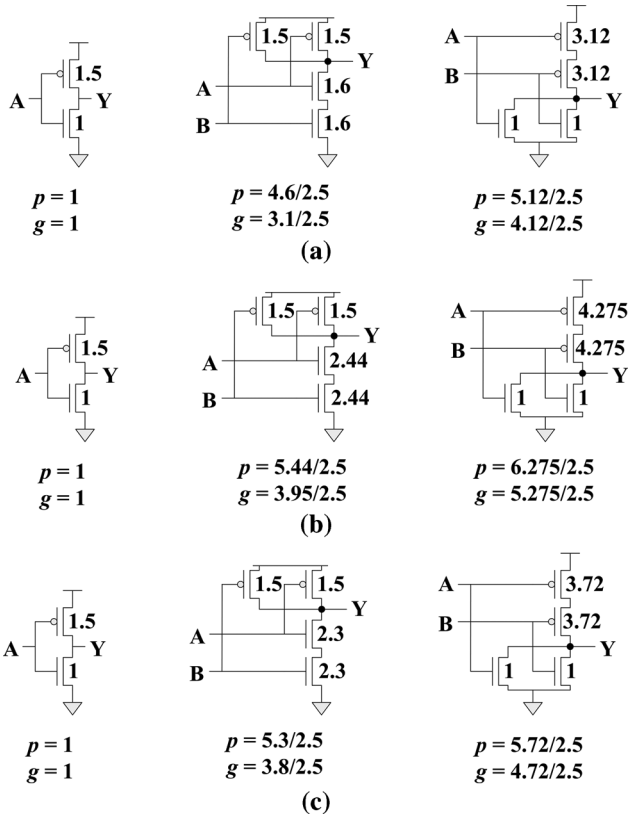

Fig. 3. Parasitic delay (p) and logical effort (g) values. (a) 1.2 V, 90-nm PTM. (b) 0.3 V, 90-nm PTM. (c) 0.2 V, 90-nm PTM.

IV. Simulation Results

A. Critical Path: A Chain of Stacks

We tested our sizing with 130-, 90-, 65-, and 45-nm PTM simulations using simple chains of logic gates that are representative of those that may be found in the critical path(s) of ultra low power circuits. In order to isolate the benefits of using the larger stack sizing in subthreshold operation, a consistent beta ratio (PMOS to NMOS width ratio) of 1.5 was employed across all simulations. This nominal value is close to that used in advanced CMOS processes. Stack sizing factors found with dc simulations as described in Section II-B were used. These experimentally determined numbers closely match our theoretical results, as stated earlier.

The logical effort sizing method was used as a straightforward means of quickly optimizing the delay though a logic path [7]. Logical effort is defined as the ratio of the input capacitance of a gate to that of an inverter driving the same amount of output current. Fig. 3 displays logical effort values based on our stack sizing parameters, as well as the corresponding parasitic delay values.

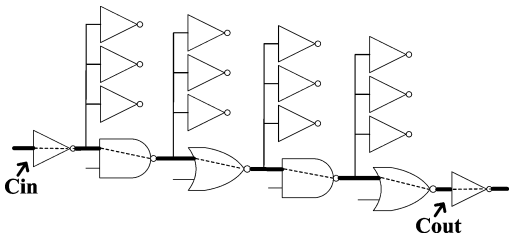

Fig. 4. Representative chain of logic gates with FO4 at each output.

TABLE III
CRITICAL PATH DELAY IMPROVEMENT FOR $V_{\rm dd} = 0.3$ V

Technology	Conventional 1.2V sizing		Subthreshold 0.3V sizing	
	Delay	Crit. Path	Speedup	Crit. Path
130nm	14.86n	Stacks	7.3%	Fast
90nm	14.10n	Stacks	6.0%	Fast
65nm	16.14n	Stacks	8.1%	Fast
45nm	24.23n	Stacks	4.6%	Fast

TABLE IV
CRITICAL PATH DELAY IMPROVEMENT FOR $V_{\rm dd} = 0.2$ V

Technology	Conventional 1.2V sizing		Subthreshold 0.2V sizing	
	Delay	Crit. Path	Speedup	Crit. Path
130nm	98.12n	Stacks	6.6%	Fast
90nm	96.25n	Stacks	6.2%	Fast
65nm	113.8n	Stacks	8.1%	Fast
45nm	174.6n	Stacks	10.4%	Fast

Parasitic delay represents the delay of a gate driving no load, and is set by the parasitic junction capacitance.

While the additional loading on previous stages created by the larger stack sizes here can degrade the performance of some logic chains, critical paths driving substantial fan-out capacitance, and particularly those containing paths dominated by stacks, do benefit from this sizing. The simple circuit illustrated in Fig. 4 is an example of a critical path whose delay is improved with our stack sizing framework. The fan-out inverter widths were kept constant across all experiments and their loading effect was taken into account through the branching factor [7]. The minimum width (i.e., the NMOS width in the unit-sized inverter) was held at 1 μm. The gate capacitance of the inverters indicated in Fig. 4 served as the input and output capacitance parameters for the logical effort calculations ($C_{\rm in}$ and $C_{\rm out}$, respectively).

Delays were found for both the path through this circuit consisting entirely of stacks (the "Stacks" path), and that containing no stacks (the "Fast" path), using the worst-case input pattern for each. Critical path delay results for $V_{\rm dd} = 0.3$ V and $V_{\rm dd} = 0.2$ V are shown in Tables III and IV, respectively. As indicated here, the critical path shifts from the stacks path to the Fast path when using the optimized subthreshold sizing, and the critical delay is consistently reduced. Also, note that the 1.2-V sizing scheme was optimal when operating in strong inversion, with improvements over subthreshold sizing performance ranging from $<1\%$ to 12.3%.

In logic paths where there are not chains of stacks driving each other in sequence, the larger subthreshold stack sizing becomes less beneficial, or even detrimental in terms of performance, due to its loading effect on the previous stage. For instance, if inverters are inserted between each NAND/NOR pair in the circuit in Fig. 4, improvements in subthreshold with our larger stack sizes are reduced to $\sim 1\%$. In a chain of just NAND gates, the smaller stack sizes used in superthreshold were generally better choices across all supply levels. In detailed optimization schemes, care must be taken to account for transient effects, including the variance of load capacitances as operating conditions change. DC sizing schemes such as the one presented here provide us with intuition about the devices we are constructing circuits with, and a starting point for thorough optimization procedures.

V. CONCLUSION

We have presented a new stack sizing framework for circuits operating in the subthreshold region. A closed-form solution for the optimal width ratio between different devices within a stack, as well as the sizing factor for stacked transistors was presented and shown to closely match experimental results. Our optimization scheme resulted in performance gains of up to 10+% in simulations of critical paths where internal node capacitance is not dominated by the increased stack sizing factors.

REFERENCES

[1] A. Wang and A. P. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 310–319, Jan. 2005.

[2] T.-H. Kim, J. Liu, J. Keane, and C. H. Kim, "A high-density subthreshold SRAM with data independent bitline leakage and virtual ground replica scheme," in *Proc. Int. Solid-State Circuits Conf.*, Feb. 2007, pp. 330–331.

[3] C. H.-I. Kim, H. Soeleman, and K. Roy, "Ultra-low-power DLMS adaptive filter for hearing aid applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 11, no. 6, pp. 1058–1067, Dec. 2003.

[4] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," *IEEE J. Solid-State Circuits*, vol. 12, no. 3, pp. 224–231, Jun. 1977.

[5] The Nanoscale Integration and Modeling Group, Tempe, AZ, "Predictive technology model," 2007 [Online]. Available: http://www.eas.asu.edu/~ptm/

[6] W. Zhao and Y. Cao, "New generation of predictive technology model for sub-45 nm design exploration," in *Proc. Int. Symp. Quality Electron. Des.*, 2006, pp. 585–590.

[7] D. Harris, R. F. Sproull, and I. E. Sutherland, *Logical Effort: Designing Fast CMOS Circuits*. San Francisco, CA: Morgan Kaufmann, 1999.