Modeling, Analysis, and Application of Leakage Induced Damping Effect for Power Supply Integrity

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***Abstract*—Leakage power is becoming the dominant component of chip power consumption with continued CMOS scaling. An important but commonly unnoticed fact is that leaky transistors act as resistors that help dampen the mid-frequency power supply noise. This paper focuses on the damping effect of various on-chip current components including the leakage current which becomes significant in scaled technologies. By developing physics-based damping models for active and leakage currents, we show that leakage, particularly gate tunneling leakage, provides more damping than strong-inversion current. The proposed models were validated in a 32-nm predictive CMOS technology under process–voltage–temperature (PVT) variations. Examples on large circuits such as SRAM caches are shown to illustrate the application of the proposed model. Simulation results show that the leakage induced damping effect can compensate the speed degradation at high temperatures by 7% or offer 61% saving in decap area and leakage power.**

***Index Terms*—Circuit modeling, integrated circuit (IC) design, leakage currents, power supply noise.**

I. Introduction

ON-CHIP power supply noise management has become a challenging task in nanoscale CMOS technologies due to the ever-increasing current density, higher switching speeds, and reduced operating voltages. Uncontrolled supply noise threatens circuits by causing problems, such as: 1) timing violations; 2) reduced noise margin; 3) substrate noise coupled into analog devices; and 4) reliability issues such as negative bias temperature instability (NBTI), hot carrier injection (HCI), and oxide breakdown [1]–[5].

In particular, on-chip supply noise at the resonant frequency determined by the package/bonding inductance and circuit capacitance [6] poses a severe threat to system performance because of its large magnitude and long duration. The resonant noise, typically in the 40–300 MHz band, can be excited by a microprocessor loop command or a large current surge during an abrupt startup or termination. Resonant supply noise can also be excited by weak sub-harmonics of the clock signal [7]. Without sufficient damping, this noise can result in a severe degradation of circuit performance due to the large impedance of the supply network at the resonant frequency. A common method for suppressing resonant noise is to lower the AC impedance of the supply network by adding large amount of decoupling capacitors (decaps) [8]. However, this approach has limitations such as significant increase in decap area and gate leakage [9]. Another commonly used method to suppress resonant noise is adding passive or active resistors in series or parallel to the supply and ground networks to provide more damping [10], [11]. Drawbacks of adding resistors include increased current–resistance (*IR*) droop and static power consumption. Circuit techniques have also been proposed to deal with the resonant supply noise issue. Ang *et al.* demonstrated a switched decoupling capacitor circuit to boost the effectiveness of decaps when resonant noise is excited [12]. Rahal-Arabi proposed a clock/data compensation scheme for resonant noise tolerance where extra timing margin is obtained by matching the clock delay with the circuit delay [13].

Leakage power consumption including both subthreshold leakage and gate leakage has become a major barrier for the continued scaling of CMOS devices. A commonly ignored fact is that a device conducting leakage current between $V_{\rm dd}$ and $G_{\rm nd}$ acts as a resistor (linear or nonlinear) that can help dampen the supply noise. It is important not to ignore this effect when designing on-chip power supply networks as leakage current provides a stronger damping effect compared to active current due to its exponential current-voltage relationship. In this paper, we model, analyze, and apply the damping effect induced by both the active and leakage current for power supply integrity. Physics-based damping models for active current, subthreshold leakage, and gate leakage are proposed and verified by simulations. The voltage dependent behavior and process–voltage–temperature (PVT) dependency of the leakage induced damping effect are also investigated. Based on the derived model, real design examples and design guidelines are provided to illustrate the application of this work. The model provided in this work provides an accurate and computationally efficient method for supply noise estimation. Benefits from the leakage induced damping effect, such as: 1) performance compensation at high temperatures and 2) decap area and leakage savings are also discussed in this paper. All simulations in this paper are based on a 32-nm Predictive Technology Model (PTM) with a supply voltage of 0.9 V [14].

II. Power Supply Network Modeling and Resonant Damping

Fig. 1 shows the resistance–inductance–capacitance (*RLC*) model of a power supply mesh with the corresponding supply noise spectrum. The frequency response in Fig. 1(b) indicates a resonant peak at $1/(2\pi\sqrt{LC})$, where L is the inductance of the package (and/or bonding wire) and C is the on-chip capacitance. Although on-chip wire inductance and circuit capacitance also introduces resonance peaks at higher frequencies as seen in

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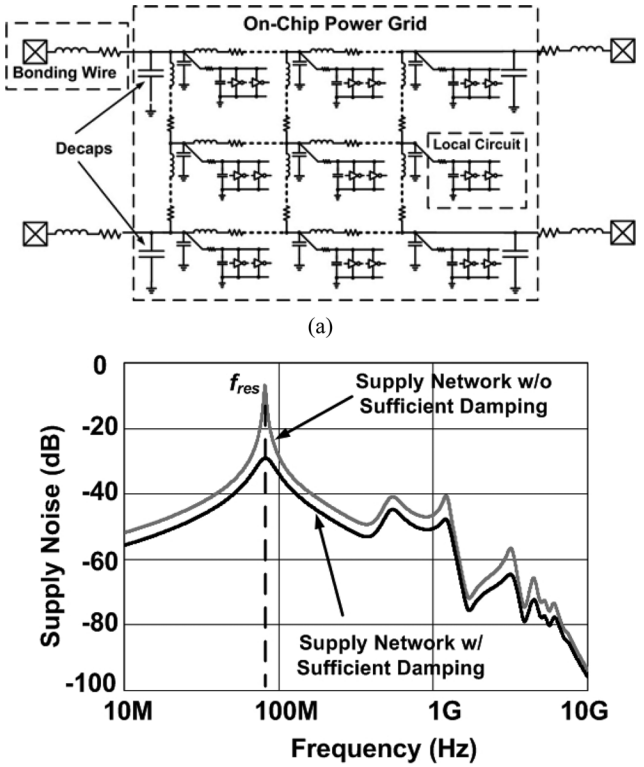


Fig. 1. (a) Power supply network model. (b) Supply noise spectrum of the supply network model in (a).

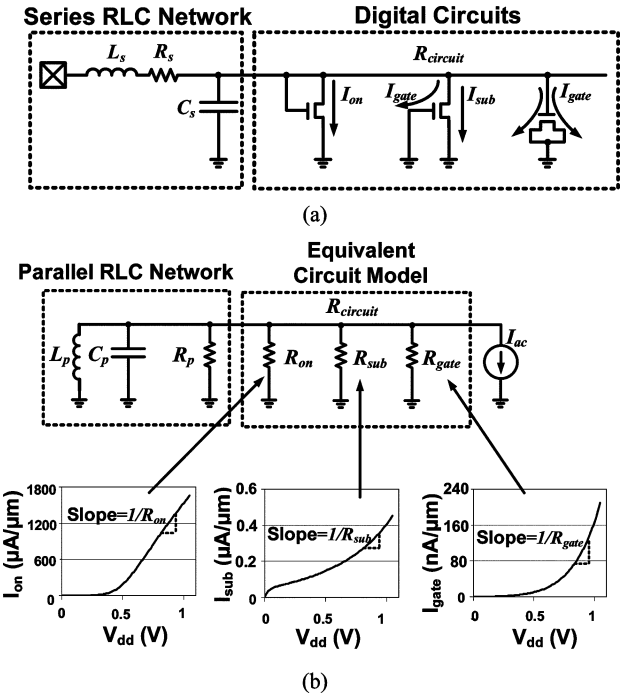


Fig. 2. (a) Simplified power supply network model. (b) Supply impedance model including the resistance of the circuit itself. Each current component has different damping effects due to the difference in equivalent resistance.

Fig. 1(b), the noise at $f_{\rm res}$ is typically a magnitude higher than the others. As a result, power supply network designs have been focused on suppressing the dominant supply noise at the resonant frequency $f_{\rm res}$. A common method to reduce the resonant noise is adding more resistance to the supply network to provide sufficient damping. Fig. 1(b) shows the noise level before and after adding a damping resistor to the power lines. The resonant noise is shown to be greatly reduced with the additional damping. As mentioned, the drawback of adding more damping is the increased *IR* droop and additional power consumption.

Fig. 2 shows a simplified supply network model with the corresponding impedance components, i.e., the package and bonding wire inductance L, the on-chip capacitance C, the series resistance R_s on the power supply network, and the equivalent resistance of the total circuit $R_{\rm circuit}$. Fig. 2(b) also shows an equivalent circuit resistance $R_{\rm circuit}$ which comes from the active current $I_{\rm on}$, subthreshold leakage $I_{\rm sub}$, and gate leakage $I_{\rm gate}$. The resistance of each current component is equivalent to the inverse of the slope of the I-V curves in Fig. 2(b) at the nominal operating point. Inspecting the I-V curves of each current component, we find that the leakage current is highly nonlinear to the supply voltage. Thus, the equivalent resistance value of leakage current cannot be treated as a constant. Furthermore, the fact that the gate leakage rises most rapidly as supply voltage increases indicates substantial damping resistance induced by gate leakage. The above observations tell us that the existence of $R_{\rm circuit}$ can no longer be ignored and a correct model of each resistance component will be important for designing efficient on-chip power supply networks.

To derive a mathematical expression for the resonant supply noise including the leakage damping effect, the series connected *RLC* network in Fig. 2(a) is transformed into a parallel connected *RLC* network in Fig. 2(b). The parallel resistance R_p, parallel inductance L_p, and parallel capacitance C_p can be calculated as

$$\begin{aligned} R_p &= R_s \cdot (1 + Q_s^2) \\ L_p &= L_s \cdot \left(1 + \frac{1}{Q_s^2}\right) \\ C_p &= C_s \end{aligned} \tag{1}$$

where Q_s is the Q factor of a series connected *RLC* network in Fig. 2(a) which can be expressed as

$$Q_s = \omega_0 \frac{L_s}{R_s} = \frac{1}{R_s} \cdot \sqrt{\frac{L_s}{C_s}}. \tag{2}$$

Here, $\omega_0 \approx 1/\sqrt{L_s C_s}$ for a high Q_s value.

The power supply noise at the resonant frequency can be calculated as the multiplication of the exciting current and the corresponding supply network impedance as shown in the following:

$$\begin{aligned} V_{\rm noise} &= I \cdot Z|_{\omega=\omega_{\rm res}} \\ &= I \cdot \left(j\omega_{\rm res} L_p \backslash\backslash \frac{1}{j\omega_{\rm res} C_p} \backslash\backslash R_p \backslash\backslash R_{\rm circuit}\right) \\ &= I \cdot (R_p \backslash\backslash R_{\rm circuit}) \end{aligned} \tag{3}$$

where I is the exciting current component at the resonant frequency. The impedance from *L* and *C* becomes infinite at $\omega_{\rm res}$ and thus the total impedance of the parallel *RLC* network is only determined by $R_p//R_{\rm circuit}$. Equation (3) shows that $R_{\rm circuit}$ will lower the supply network impedance and hence result in a lesser supply noise. Due to the small value of R_s (or large corresponding R_p), the original damping provided from the power supply network itself is usually not sufficient and additional damping has to be added with the penalty of increased *IR* droop and power consumption. However, the fact that $R_{\rm circuit}$ of the circuit itself can provide significant damping to the supply noise is typically ignored by circuit designers. The goal of this paper is to develop an accurate model for $R_{\rm circuit}$, examine its damping effect on supply noise, and investigate its variation under different circuit operating conditions. It is important to note that the damping effect provided by R_p and $R_{\rm circuit}$ are effective for *L di/dt* noise at all frequencies rather than just for that at $f_{\rm res}$. However, since the supply noise is most pronounced at the resonant frequency, we will mainly focus on the damping effect at $f_{\rm res}$ throughout this paper.

III. Modeling the Damping Effect for Active and Leakage Current

In this section, we discuss the modeling of equivalent resistance and conductance for active current $I_{\rm on}$, subthreshold leakage $I_{\rm sub}$, and gate leakage $I_{\rm gate}$. Because supply noise is typically controlled below 15% of the nominal $V_{\rm dd}$, the damping conductance will be calculated based on a small-signal analysis; i.e., the $dI/dV_{\rm dd}$ value will be derived at the nominal $V_{\rm dd}$ point, where I can be one of the following: $I_{\rm on}$, $I_{\rm sub}$, and $I_{\rm gate}$. The equivalent damping resistance is then simply the inverse of the calculated conductance.

A. Damping Model for Active Current

Active current of a saturation mode device can be modeled as

$$\begin{aligned} I_{\rm on} &= \mu_e \cdot C_{\rm ox} \cdot \frac{W}{L} \cdot (V_{\rm gs} - V_{\rm th})^{\alpha} \\ &\approx \mu_e \cdot C_{\rm ox} \cdot \frac{W}{L} \cdot (V_{\rm dd} - (V_{\rm th0} - \lambda V_{\rm dd})) \end{aligned} \tag{4}$$

using the alpha-power law current equation with $\alpha \approx 1$ [15]. In this equation, $V_{\rm th0}$ is the zero $-V_{\rm ds}$ threshold voltage, and λ is the drain induced barrier lowering (DIBL) coefficient. From (4), we can calculate the damping conductance as

$$\begin{aligned} \frac{dI_{\rm on}}{dV_{\rm dd}} &= \mu_e \cdot C_{\rm ox} \cdot \frac{W}{L} \cdot (1+\lambda) \\ &= \frac{\overline{I_{\rm on}}}{\overline{V_{\rm dd}} - (V_{\rm th0} - \lambda \overline{V_{\rm dd}})} \cdot (1+\lambda) \\ &= \frac{(1+\lambda)}{(1+\lambda)\overline{V_{\rm dd}} - V_{\rm th0}} \cdot \overline{I_{\rm on}} \end{aligned} \tag{5}$$

where $\overline{V_{\rm dd}}$ is the nominal supply voltage and $\overline{I_{\rm on}}$ is the nominal active current at $\overline{V_{\rm dd}}$. A parameter denoted with a bar in this paper refers to the dc bias value, i.e., the operating point for small signal analysis. The $V_{\rm gs}(= V_{\rm dd})$ term in the current equation and DIBL contributes to the damping conductance. Equation (5) indicates that the damping conductance of the active current is a constant determined by its operating points $\overline{V_{\rm dd}}$ and $\overline{I_{\rm on}}$.

B. Damping Model for Subthreshold Leakage Current

Subthreshold leakage current can be described as

$$\begin{aligned} I_{\rm sub} &= \mu_e \cdot C_{\rm ox} \cdot \frac{W}{L} \cdot \left(\frac{kT}{q}\right)^2 \cdot (m-1) \cdot e^{q(0-V_{\rm th})/mkT} \\ &= \mu_e \cdot C_{\rm ox} \cdot \frac{W}{L} \cdot \left(\frac{kT}{q}\right)^2 \cdot (m-1) \\ &\quad \cdot e^{-q(V_{\rm th0}-\lambda V_{\rm dd})/mkT} \end{aligned} \tag{6}$$

where m is the body effect coefficient and kT/q is the thermal voltage. The damping conductance of $I_{\rm sub}$ is then calculated as

$$\begin{aligned} \frac{dI_{\rm sub}}{dV_{\rm dd}} &= \frac{q\lambda}{mkT} \cdot I_{\rm sub} \\ &\approx \frac{q\lambda}{mkT} \cdot \left(1 + \frac{q\lambda}{mkT} \cdot \Delta V_{\rm dd}\right) \cdot \overline{I_{\rm sub}} \end{aligned} \tag{7}$$

where $\overline{I_{\rm sub}}$ is the nominal leakage current at $\overline{V_{\rm dd}}$ and $\Delta V_{\rm dd}$ is the power supply noise. The finite damping conductance for subthreshold leakage mainly comes from the DIBL effect. Unlike active current, $dI_{\rm sub}/dV_{\rm dd}$ has to be modeled as a function of supply noise $\Delta V_{\rm dd}$ because of the nonlinear exponential relationship between $I_{\rm sub}$ and $V_{\rm dd}$. The linearization of $I_{\rm sub}$ with respect to $\Delta V_{\rm dd}$ in (7) is performed using Taylor's expansion around the nominal supply voltage $\overline{V_{\rm dd}}$. Similar to the case for active current, (7) shows that the damping conductance from subthreshold leakage is proportional to the dc leakage current $\overline{I_{\rm sub}}$. However, the damping conductance of subthreshold leakage is also a linear function of $\Delta V_{\rm dd}$, so its value changes with supply noise. This voltage dependent resistance behavior provides additional damping performance as will be shown in Section III-E.

C. Damping Model For Gate Leakage Current

The gate leakage current can be expressed as

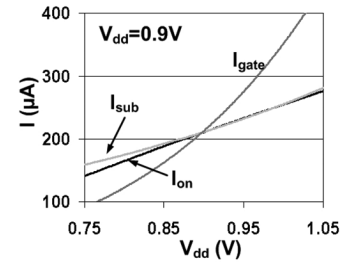
$$I_{\rm gate} = W \cdot L \cdot A \cdot \frac{V_{\rm dd}^2}{T_{\rm ox}^2} \cdot \exp\left(\frac{-B(1-(1-\frac{V_{\rm dd}}{\phi_{\rm ox}})^{3/2})}{\frac{V_{\rm dd}}{T_{\rm ox}}}\right) \tag{8}$$

where $T_{\rm ox}$ is the oxide thickness and $\phi_{\rm ox}$ is the barrier height for tunneling electrons or holes [16]. A and B are given as

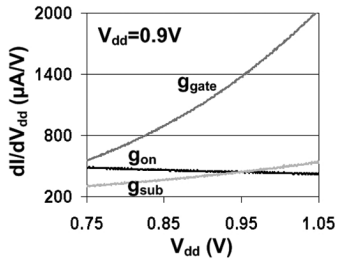
$$A = \frac{q^3}{16\pi^2\hbar\phi_{\rm ox}} \quad B = \frac{4\sqrt{2m^*}\phi_{\rm ox}^{3/2}}{3\hbar q}$$

where m^* is the effective mass of tunneling electrons or holes and $\hbar$ is the reduced form of Plank's constant. By performing a first-order Taylor's expansion on the derivative of $I_{\rm gate}$ and ignoring the higher order terms, we find the following equation:

$$\frac{dI_{\rm gate}}{dV_{\rm dd}} = \left(\frac{2}{\overline{V_{\rm dd}}} + C + (\frac{2}{\overline{V_{\rm dd}}^2} + \frac{4}{\overline{V_{\rm dd}}} \cdot C) \cdot \Delta V_{\rm dd}\right) \cdot \overline{I_{\rm gate}} \tag{9}$$



(a)



(b)

Fig. 3. (a) Simulated $I_{\rm on}$, $I_{\rm sub}$, and $I_{\rm gate}$ as functions of $V_{\rm dd}$. (b) Corresponding conductance of each current component.

where

$$C=\left(1-\sqrt{1-\overline{V_{\rm dd}}/\phi_{\rm ox}}\cdot\left(1+\overline{V_{\rm dd}}/2\phi_{\rm ox}\right)\right)\cdot T_{\rm ox}\cdot B/\overline{V_{\rm dd}}^{2}.$$

Although (9) requires a more involved calculation, the behavior of damping from gate leakage is similar to that of subthreshold leakage in the sense that it is proportional to the dc bias current and is dependent on the supply noise $\Delta V_{\rm dd}$.

D. Damping Effect Comparison Between $I_{\rm on}$, $I_{\rm sub}$, and $I_{\rm gate}$

Fig. 3 shows the current and damping conductance of each component ($I_{\rm on}$, $I_{\rm sub}$, and $I_{\rm gate}$) as a function of supply voltage. For comparison, results are shown when the three current values are set to be the same at the nominal condition (i.e., $V_{\rm dd}$ = 0.9 V). Fig. 3 shows that for an equal amount of current, gate leakage provides a much stronger damping effect than the other two current components. The effective conductance of subthreshold and gate leakage can be modeled as a linear function of $\Delta V_{\rm dd}$ as opposed to a constant value that was derived for the on-current. This is verified in Fig. 3(b) where the damping conductance increases almost linearly with supply voltage for both subthreshold and gate leakage.

Table I summarizes the effective damping conductance for each current component. The coefficients calculated using the developed models are compared with the coefficients obtained from HSPICE simulation. Our damping models using physical parameters show a good fit with simulation results, which indicate that the developed model is capable of accurately capturing the behavior of the current induced damping effect. Small discrepancies between our model and the simulation exist due to the following reasons: 1) the α parameter in (4) is actually between 1 and 1.2 which leads to a smaller $I_{\rm on}$ conductance value predicted by the model; 2) the source/drain series resistance in the MOSFET device accounts for the slight drop in $g_{\rm on}$ in Fig. 3(b) but is not modeled in our simplified current equation; 3) the modeling of gate tunneling leakage for an ultra-thin oxide device involves a more complex mathematical representation and therefore an error exists when using the simple equation in (9) to obtain the solution. The key advantage of our proposed model is that for a given leakage current and a set of technology parameters, the supply noise can be calculated without having to run exhaustive HSPICE simulations.

TABLE I
COMPARISON OF THE CURRENT INDUCED DAMPING CONDUCTANCE BETWEEN THE DERIVED MODELS AND HSPICE SIMULATIONS

	Derived Model	HSPICE Simulation
$g_{on}=1/R_{on}$	$1.80\cdot\overline{I_{on}}$	$2.13\cdot\overline{I_{on}}$
$g_{sub}=1/R_{sub}$	$(1.80+3.24\,\Delta V_{dd})\cdot\overline{I_{sub}}$	$(1.92+3.55\,\Delta V_{dd})\cdot\overline{I_{sub}}$
$g_{gate}=1/R_{gate}$	$(5.51+17.1\,\Delta V_{dd})\cdot\overline{I_{gate}}$	$(5.22+19.6\,\Delta V_{dd})\cdot\overline{I_{gate}}$

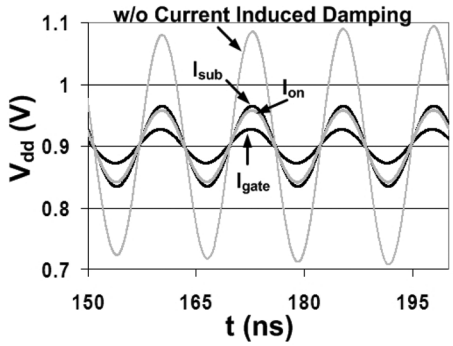


Fig. 4. Supply resonant noise damped by different current components. Gate leakage provides largest damping effect for the same amount of current. The label on each waveform denotes the current component that is used to damp the supply noise.

Fig. 4 shows the simulated transient damping performance at the resonant frequency for the different current components. A small wire resistance R_s is added to the *LC* supply network to prevent the resonance noise from becoming unrealistically large. Note that to test the subthreshold leakage damping, a small positive gate bias is applied to amplify the subthreshold leakage so that the gate leakage becomes negligible in proportion. The results in Fig. 4 are consistent with our resistive model given in Table I. Each current component provides significant damping effect with gate leakage being the strongest.

E. Effect of Voltage Dependant Damping From Leakage Currents

The effect of voltage dependent conductance can be evaluated as follows. Ignoring the resistance of the supply mesh, the supply noise at the resonant frequency $f_{\rm res}$ can be calculated as

$$\Delta V'_{\rm dd}=I_{\rm ac}\cdot R=\frac{I_{\rm ac}}{(g_0+g_1\cdot\Delta V'_{\rm dd})} \tag{10}$$

where $I_{\rm ac}$ is the exciting current at frequency f_{res}. g_0 and g_1 are the constant term and linear coefficient in our resistive model in Table I; i.e., $g=g_0+g_1\cdot\Delta V_{\rm dd}$. Note that the nominal currents

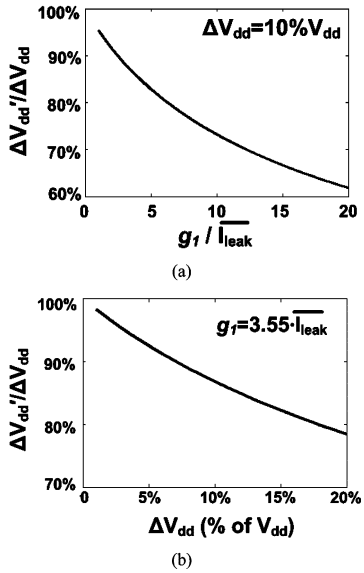


Fig. 5. Additional damping from the voltage dependent conductance of the leakage currents. (a) Damping effect as a function of g_1 (normalized to nominal leakage value). (b) Damping effect as a function of noise magnitude $\Delta V_{\rm dd}$.

$\overline{I_{\rm sub}}$ and $\overline{I_{\rm gate}}$ have been included in g_0 and g_1. Solving (10) for $\Delta V'_{\rm dd}$, we can calculate the supply noise as

$$\Delta V'_{\rm dd} = \frac{-g_0 + \sqrt{g_0^2 + 4g_1 I_{\rm ac}}}{2g_1}. \tag{11}$$

For comparison purposes, we can also calculate the supply noise while ignoring the voltage dependant term

$$\Delta V_{\rm dd} = I_{\rm ac} \cdot R = \frac{I_{\rm ac}}{g_0}. \tag{12}$$

To examine the voltage dependent conductance of leakage currents, we plot the $\Delta V'_{\rm dd}/\Delta V_{\rm dd}$ as a function of g_1 and $\Delta V_{\rm dd}(= I_{\rm ac}/g_0)$ in Fig. 5. $\Delta V'_{\rm dd}/\Delta V_{\rm dd}$ in the y-axis shows the amount of extra damping the voltage dependent term provides compared with the case without the voltage dependent term. Fig. 5 shows that as g_1 and the noise magnitude $\Delta V_{\rm dd}$ increase, the effect of the voltage dependent conductance from the leakage currents becomes more significant. For instance, for a $\Delta V_{\rm dd}$ of 0.1 V (11% of $V_{\rm dd}$), the voltage dependent term $g_1 \cdot \Delta V_{\rm dd}$ for subthreshold leakage $(g_1 = 3.55 \cdot \overline{I_{\rm sub}})$ provides an additional 14.5% reduction in power supply noise compared with a constant conductance g_0. Similarly, the voltage dependent term in gate leakage $(g_1 = 19.6\overline{I_{\rm gate}})$ provides an extra 22% reduction in supply noise for a $\Delta V_{\rm dd}$ of 0.1 V. This observation indicates that on-chip leakage components have a stronger damping effect than active current for equal amount of current because of a larger g_0 and the voltage dependent damping behavior. With the increase in leakage current with technology scaling, the damping induced by leakage current becomes significant and must be carefully characterized for optimal power supply network design.

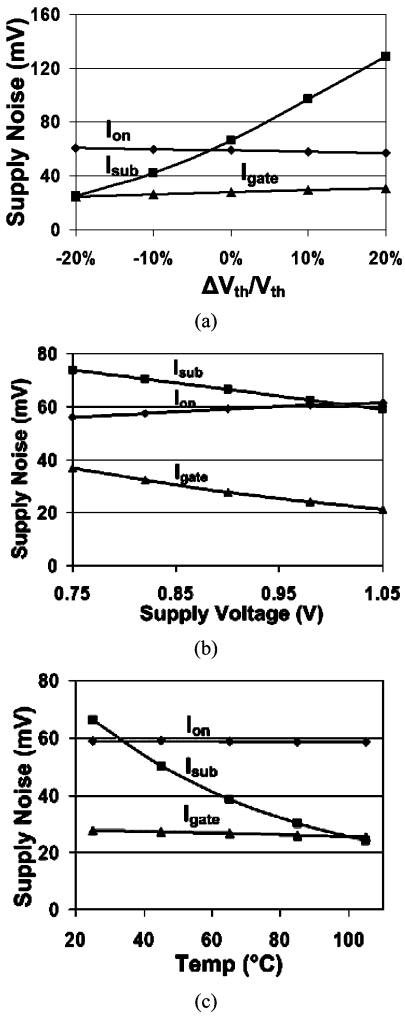


Fig. 6. Simulated damping effect under PVT variation. (a) Threshold voltage variation. (b) Supply voltage variation. (c) Temperature variation. Note that larger damping effect leads to smaller supply noise.

IV. Leakage Induced Damping Effect Under PVT Variations

PVT variation has become an increasingly critical issue in deeply scaled LSI circuits. Due to the fact that different leakage components have different sensitivities to PVT variation, it is necessary to examine the leakage induced damping effect under various PVT conditions.

Fig. 6 compares the resonant supply noise for each damping current component while varying the PVT parameters. All current components have equal current values at the nominal condition ($V_{\rm th}$ at typical corner, 0.9-V supply voltage, and room temperature). Fig. 6(a) shows the impact of threshold voltage variation on damping effects of each current component. It is shown that the damping effect of subthreshold leakage varies the most under $V_{\rm th}$ variation because of its exponential dependency on $V_{\rm th}$. This observation indicates that transistors in a fast corner die (lower $V_{\rm th}$) will introduce a larger damping effect, which in turn can compensate for the increased *IR* and *L di/dt* droop due to the larger transient currents. Fig. 6(b) shows the impact of supply voltage variations on damping effects. Both subthreshold

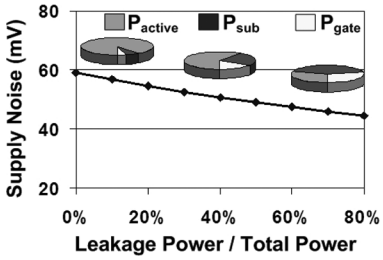


Fig. 7. Simulated resonant supply noise versus leakage power ratio.

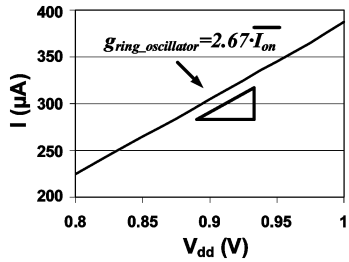


Fig. 8. Active current versus supply voltage of a ring oscillator circuit. The slope corresponds to the equivalent damping conductance of the circuit.

leakage and gate leakage show an increased damping performance as $V_{\rm dd}$ rises while damping from active current is slightly reduced. This observation is consistent with Fig. 3(b) and can be explained by the models developed in Section III. Fig. 6(c) shows the temperature dependency of the damping effects from each current component. With the increase in temperature, the damping from subthreshold leakage increases dramatically, resulting in a significantly reduced noise level as shown in the figure. By inspecting the subthreshold damping model in (7), we find that the damping coefficient actually decreases with temperature. However, the dc leakage current $\overline{I_{\rm sub}}$ increases exponentially with temperature, and therefore, the overall damping performance by subthreshold leakage improves. This positive temperature dependency can compensate the slow-down of circuits at high temperatures as will be discussed in Section VI-A.

Based on the previous discussion on current induced damping, the overall damping effect in a realistic VLSI system will depend on the ratio between leakage power and active power because different current components have different damping coefficients as seen in Table I. Fig. 7 displays how the resonant supply noise changes when varying the leakage versus active current ratio. For simplicity, we assumed a fixed ratio (60%:40%) between the subthreshold and gate leakage. Fig. 7 shows increased damping and less supply noise in leakier chips. For example, a chip with 70% leakage power has 19% less resonant noise compared to a chip with 10% leakage power, due to the leakage induced damping effect.

V. Applying the Current Induced Damping Effect in Large Scale Designs

A. Modeling of Active Current Damping in Real Circuits

There are certain considerations to take when applying the derived damping models in Section III on large scale circuits. The leakage damping equations for subthreshold current and gate current derived in Section III are still valid for real circuits because any leakage component in a real circuit can be represented by the leakage models given in Section III. However, for active current, the damping equation in (5) may not be accurate for the following two reasons. First, real circuits contain transistor stacks which have different damping resistance compared to single stacks. Second, during a switching transient, the transistors do not always stay in the saturation region and thus (5) which is based on the saturation current model may no longer be accurate. Obtaining an analytical resistive model for large scale circuits is challenging because of the various circuit types and different operating regions. To understand this issue better, we perform HSPICE simulations on a 21-stage ring oscillator circuit having a 5-GHz switching frequency. Fig. 8 shows the active current versus the supply voltage of the simulated ring oscillator circuit.

The simulation results provide us with the following important observations.

1) A high linearity is observed between the active current and supply voltage. This is consistent with our derived model in (5) and indicates that we can still use a similar expression as (5) to represent the damping resistance from real circuits.
2) The simulated conductance of the ring oscillator is $g_{\rm ring_oscillator} = 2.67 \cdot \overline{I_{\rm on}}$. Compared with the model shown in Table I ($g_{\rm on} = 2.13 \cdot \overline{I_{\rm on}}$), the error is not very significant. This is because most of the switching current corresponds to the saturation current in short channel devices due to the carrier velocity saturation. Simulation results in Section V-B show that the estimation error for supply noise is less than 6% using the models in Table I which is acceptable for most supply noise analysis methods. In fact, using the $g_{\rm on}$ derived in Section III gives an upper bound of the supply noise and therefore can be used to calculate the worst case supply noise damping of large scale designs.

B. Design Guideline for Modeling Supply Noise Damping

Fig. 9 shows the block diagram for modeling the current induced damping in larger circuits.

The modeling process follows a bottom-up design flow with the following steps.

1) *Technology Characterization:* Damping resistance/conductance models for various current components are derived based on device I-V characteristics;
2) *Top-Level Circuit Characterization:* Various current components are obtained for the large scale circuit and the damping resistance/conductance is calculated using the model derived in 1).
3) *Power Supply Network Design:* Decap assignment and supply mesh impedance optimization are performed.
4) *Supply Noise Estimation:* Damping models and supply network model are used to estimate the supply noise level. The supply network design can go through iterations in case the target supply noise is not met.

The advantage of using our proposed damping model and the characterization procedure shown before is that with the current

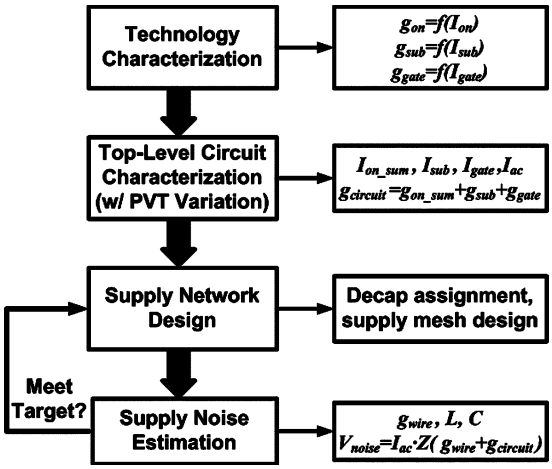


Fig. 9. Supply noise estimation of large scale circuits considering the current induced damping effect.

TABLE II
DAMPING EFFECT MODELING OF A 64-kB SRAM CIRCUIT

Technology	32nm	SRAM Size	64KByte
I_{on}	21mA	g_{on}	$0.045\Omega^{-1}$
I_{sub}	30mA	g_{sub}	$0.068\Omega^{-1}$
I_{gate}	23mA	g_{gate}	$0.165\Omega^{-1}$
I_{total}	74mA	g_{total}	$0.278\Omega^{-1}$
R_s	0.01Ω	L	0.5nH
C	6nF	Supply Noise w/o Leak. Damping (HSPICE)	145mV
Supply Noise w/ Leak. Damping (Proposed Model)	90mV	Supply Noise w/ Leak. Damping (HSPICE)	85mV
Noise Reduction Including Leak. Damping	38%	Modeling Error	6%

consumptions determined from the design of each circuit block, the damping resistance can be directly calculated and thus an exhaustive full-chip supply noise simulation can be avoided.

To verify the effectiveness of the proposed supply noise estimation approach, a 64-kB SRAM array without the peripheral circuits is built as a test vehicle. Table II lists the circuit specifications of the SRAM array. The wordlines are grounded for the unselected SRAM cells and thus they only provide leakage current. Periodic wordline and bitline signals are asserted to the selected cells to generate the access current. From the active and leakage current in a single SRAM cell, the damping conductance of each current component is calculated using the model derived in Section III. Knowing the total numbers of idle and active SRAM cells, we are able to calculate the conductance of $g_{\rm on}$, $g_{\rm sub}$, $g_{\rm gate}$, and $g_{\rm total}$ of the entire SRAM array. The supply noise value is then calculated and compared with HSPICE simulation results. The estimation error was only 6% using the proposed approach which saves the time-consuming simulation of full-chip supply noise for large scale circuits. The results also show that the overall resonant noise is reduced by 38% with the consideration of the current induced damping effect.

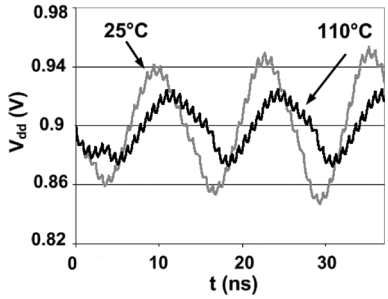


Fig. 10. Simulated noise waveforms at 25 °C and 110 °C for an ISCAS benchmark circuit (C3540, 8-bit ALU).

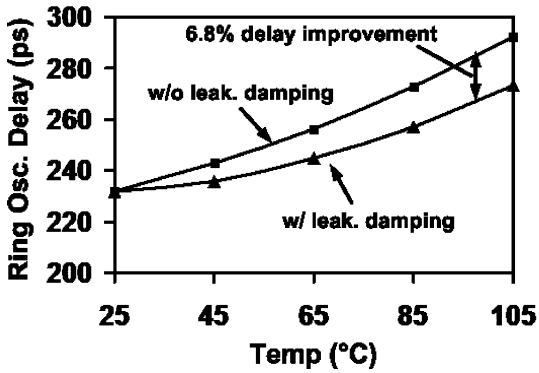


Fig. 11. Ring oscillator delay at different temperatures including and not including the leakage damping effect. The performance loss at high temperatures is partially compensated due to the reduced supply noise with increased subthreshold leakage.

VI. BENEFITS OF LEAKAGE INDUCED DAMPING EFFECT

A. Performance Compensation At High Temperatures

An interesting phenomenon we observed in Section IV is that at higher temperatures, the supply noise is reduced due to the increase of leakage induced damping. Fig. 10 shows the transient noise waveforms simulated on benchmark circuits at different temperatures. We used an ISCAS'85 benchmark circuit [C3540, 8-bit arithmetic logic unit (ALU)] clocked at 640 MHz for generating the supply noise. Six additional circuit blocks of the same kind are placed in idle mode to provide the subthreshold and gate leakage. To excite the resonant noise at (80 MHz $=$ 640 MHz$/8$), a large capacitive load is driven by a divided clock that is 8 times slower than the system clock. Fig. 10 confirms the increased damping effect at a higher temperature due to the increase in subthreshold leakage as explained in Fig. 6(c).

The previous observation indicates that the performance loss at higher temperature can be partially compensated by the extra damping provided by the increased subthreshold leakage current. Fig. 11 shows delay of a ring oscillator at different temperatures with and without considering the leakage induced damping. The delay is measured under the worst supply droop in each temperature. For a comparison of the temperature dependency, the starting point of the supply noise at room temperature is set to be the same in both cases. The figure shows that although delay increases at higher temperatures in both cases, the performance loss is compensated by the reduced supply noise with the leakage induced damping effect. The

TABLE III
DELAY AND SUPPLY NOISE AT DIFFERENT TEMPERATURES WITH AND WITHOUT LEAKAGE DAMPING

Temp. (C°)	Total Noise w/o Damp (mV)	Total Noise w/ Damp (mV)	DC Noise* (mV)	Delay w/o Damp (ps)	Delay w/ Damp (ps)	Delay Diff. (%)
25	69	69	2	232	232	0
45	70	54	3	243	236	2.9%
65	72	44	5	256	244	4.7%
85	74	38	7	273	257	5.9%
105	77	35	11	293	273	6.8%

* The DC noise is included in the total noise value in previous columns.

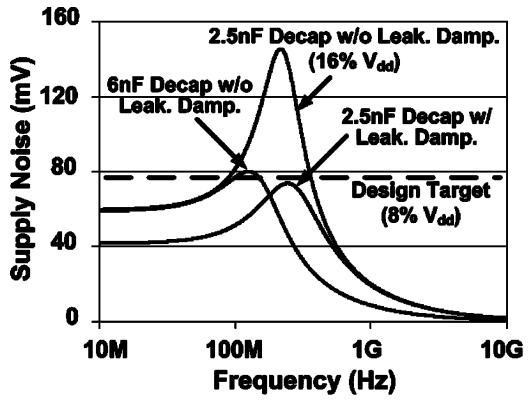


Fig. 12. Frequency spectrum of supply noise with and without considering the leakage damping effects for decap assignment.

results in Fig. 11 are summarized in Table III. Note that at a higher temperature, the dc supply noise increases because of the dramatic increase of leakage current (5× at 105 °C in this case). As a result, the reduction of ac supply noise from leakage damping is compensated a little from the increase of dc supply noise. However, because the ac noise component is much larger than the dc noise, the ac supply noise still has the dominant impact on the delay of the circuit. Overall, we observe the leakage induced damping helps the circuit's performance at higher temperatures.

B. Decap Area and Leakage Saving

In order to meet the supply noise constraints, the most common solution is to add more on-chip decaps [8]. Adding decaps is inefficient because one has to pay a large amount of decap area overhead to bring down the Q factor of the *RLC* network which is given as $Q = 1/R \cdot \sqrt{L/C}$. This is especially the case when the supply network resistance R is small. The gate tunneling leakage through the MOS decaps can be significant in scaled technologies due to the ultra-thin oxide thickness [9]. Simulation results in Fig. 12 show that the decap requirement can be alleviated when the leakage induced damping effect is taken into account. The parameters for the test circuit are given in Table IV. Decap of the original circuit is approximately 2.5 nF causing the resonant supply noise to

TABLE IV
SIMULATION PARAMETERS FOR DECAPS ASSIGNMENTS

I_{on}	95mA	I_{sub}	20mA
I_{gate} (w/ decap leakage)	50mA	f_{res}	225MHz
R_s	0.2Ω	L	0.2nH
Required decap w/o leak. damping	6.5nF	Required decap w/ leak. damping	2.5nF

reach 16% of the nominal supply voltage. In order to meet a supply noise target of 8%, an additional 4 nF of decap has to be added if the leakage induced damping effect is not considered. Our simulation results show that when the leakage induced damping effect is considered, no additional decap needs to be added because substantial damping is already been provided by the leakage current of the decap itself. This leads to a total decap reduction of 61% achieving significant saving in area and decap gate leakage power. Note that reducing the amount of decap increases the supply noise at frequencies higher than the resonant frequency, and hence a tradeoff has to be made between the resonant noise and high frequency noise for optimal supply network designs.

VII. CONCLUSION

Leakage power in modern VLSI circuits is becoming comparable to active power. A fact that has generally gone unnoticed is that on-chip leakage current can provide damping for power supply noise. This is especially beneficial for suppressing the resonant supply noise which can severely degrade the circuit performance once excited. This paper investigates the leakage induced damping effect in scaled technologies. Models for the damping effect induced by the active current, subthreshold leakage, and gate leakage are developed and verified with HSPICE simulations in a 32-nm CMOS technology. The voltage dependent conductance of leakage current shows 22% additional reduction of supply noise compared with a voltage independent damping model. The impact of PVT variations on damping effect is also investigated. Simulation shows that gate leakage provides the strongest damping per current while subthreshold leakage varies the most with PVT variations. Design example of a 64-kB SRAM circuit is shown to illustrate the application of the derived model on large scale integrated circuits. Compared with HSPICE simulation results, an estimation error of 6% is achieved by using the proposed model which significantly saves the simulation time for power supply networks. Benefits of leakage induced damping are shown including performance compensation at high temperatures and decap area saving. Simulation shows 7% compensation in circuit speed at 105 °C due to the enhanced damping from the increased subthreshold leakage. A 61% reduction in decap area and decap leakage can also be achieved when the leakage induced damping effect is considered.

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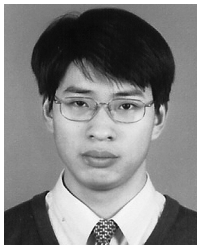

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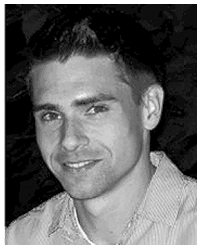

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