Silicon Odometers: On-Chip Test Structures for Monitoring Reliability Mechanisms and Sources of Variation

John Keane Tae-Hyoung Kim Chris H. Kim
University of Minnesota, Minneapolis, MN

The aggressive down-sizing of device dimensions and voltage margins has left little room for transistor degradation, so in addition to dealing with PVT variations, a detailed understanding of numerous aging processes generally studied by device scientists is needed at the circuit and system levels. In this paper, we describe a number of circuit methods to efficiently monitor accelerated device degradation due to bias temperature instability (BTI), as well as time dependent gate dielectric breakdown (TDDB). The measurement schemes presented here can also be applied to monitor spatial or temporal variations affecting chip performance. Results from such sensors can be used to gather process information, verify existing degradation models, or trigger real-time on-chip adjustments during product usage.

First, we present an on-chip negative bias temperature instability (NBTI) sensor using a delay-locked loop (DLL), in which the increase in PMOS threshold voltage due to NBTI stress is translated into a control voltage shift in the DLL for high sensing gain [1]. The proposed sensor is capable of supporting both DC and AC stress modes. Measurements from a 130nm test chip show a maximum gain of 16X in the operating range of interest, with measurement times in tens of microseconds possible for minimal unwanted threshold voltage recovery. NBTI degradation readings across a range of operating conditions are presented to demonstrate the flexibility of this system.

Second, we describe a fully-digital on-chip monitor for high resolution differential frequency measurements in digital circuits [2]. The proposed technique measures the beat frequency of two ring oscillators (ROSC), with one acting as a reference point, to achieve 50X higher delay sensing resolution than prior techniques. The differential measurement also eliminates the effects of common-mode environmental variation, such as temperature drifts, between the sampling points. A 265x132μm^2 test chip has been fabricated in a 1.2V, 130nm CMOS technology. The measured resolution of the proposed monitoring circuit was 0.02%. The ring oscillator in this design has a period of 4ns, which then translates to a temporal resolution of 0.8ps. This precision would lend itself well to measuring, for instance, even slight voltage variations in an appropriate sensor configuration. Also, the 2μs measurement time was short enough to suppress the unwanted BTI recovery effect from concealing the actual circuit degradation when one ROSC was placed under accelerated stress.

Finally, we present a circuit design that performs automated measurements in a test array to efficiently gather the TDDB characteristics that define this statistical process [3]. The proposed circuit can monitor a progressive decrease in gate resistance, or simply an abrupt failure often referred to as a hard breakdown. This structure greatly reduces the required process characterization testing time, which may involve continuously monitoring the current through a single device under test (DUT) per experiment with a finely tuned parametric test system. Given the need for up to thousands of test samples to correctly define the Weibull slope of the time to breakdown distribution, that serial testing process quickly becomes cumbersome. In addition, the array format is also a convenient method to study any spatial variations in gate dielectric strength, without requiring sophisticated testers or elaborate test setups.

This summary paper will allow us to present the benefits and drawbacks of each of the designs listed above. Each circuit here is well-suited to provide information about critical reliability and/or variability mechanisms in advanced process. Such measurement concepts are in high demand now due not only to scaling, but also the rapid introduction of new process features such as strained silicon and high-k gate dielectrics. Dealing with the range of challenges in advanced technologies requires rigorous work from the device level and up through the system level, with on-chip monitors playing a critical role in that spectrum.

[1] J. Keane, T.-H. Kim, and C. H. Kim, "An On-Chip NBTI Sensor for Measuring PMOS Threshold Voltage Degradation," Int. Symp. on Low Power Electronics and Design, pp. 189-194, August 2007.

[2] T.-H. Kim, R. Persaud, C. H. Kim, "Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits," IEEE Symposium on VLSI Circuits, pp. 122-123, June 2007.

[3] J. Keane, S. Venkatraman, P. Butzen, C. H. Kim, "An Array-Based Test Circuit for Fully Automated Gate Dielectric Breakdown Characterization," Custom Integrated Circuits Conference, September 2008.