Enhancing *Beneficial Jitter* Using Phase-Shifted Clock Distribution

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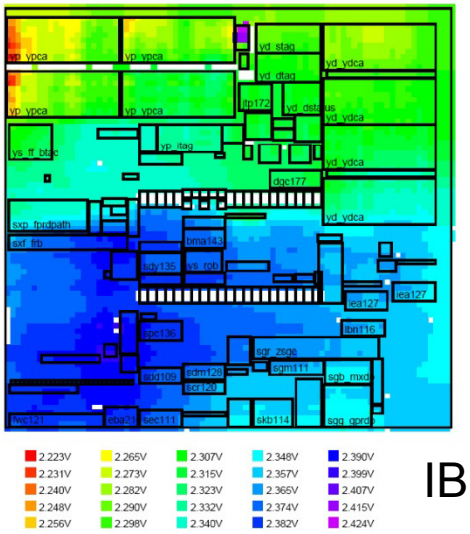
Presentation Agenda

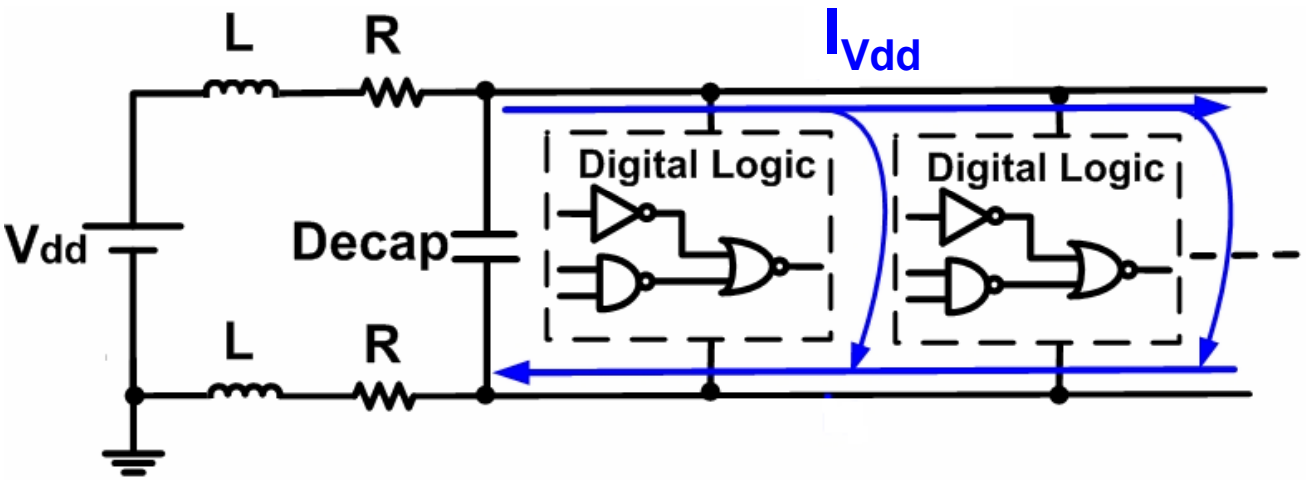
- Resonant Noise and Timing
- Overview of *Beneficial Jitter* Effect
- Timing Models and 65nm Simulations
- Phase-Shifted Clock Distribution
- Conclusions

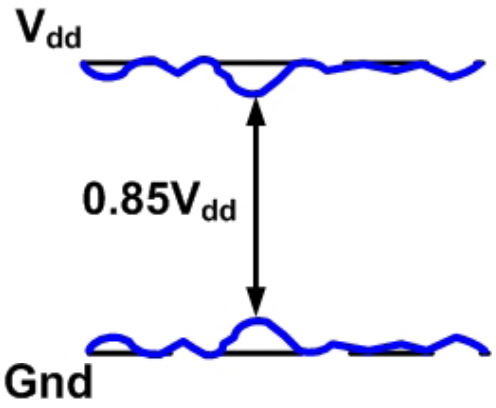
Power Supply Noise

- ***IR* and *Ldi/dt* noise:**
  - **Typically around 10~15% nominal V_{dd}**
- **Lower V_{dd}, larger I_{Vdd}, higher f_{clk}:**
  - **Worsening supply noise with scaling**
- **Problems due to supply noise:**
  - **Timing, noise margin, reliability, *etc***

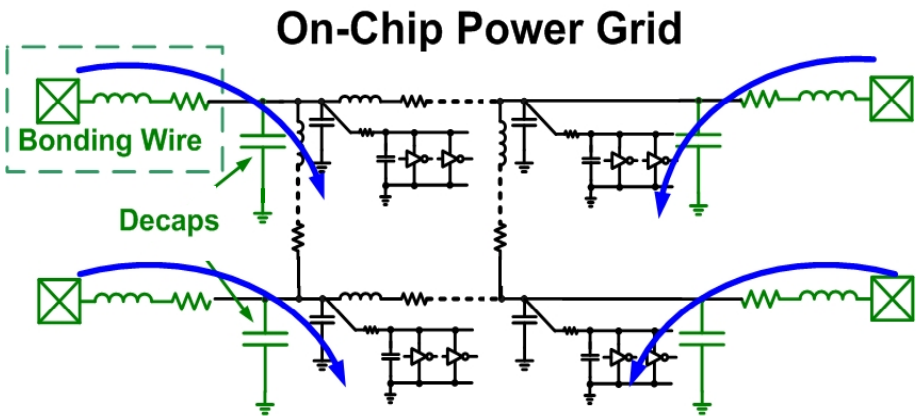


IBM

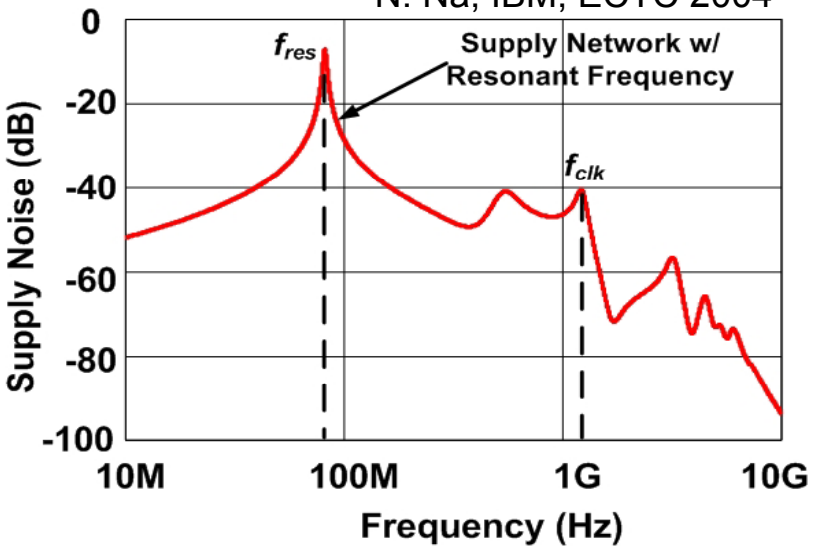




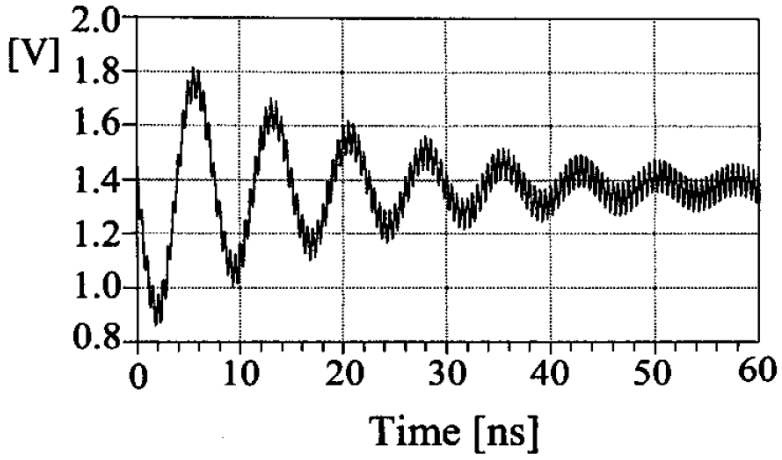
Resonant Supply Noise



N. Na, IBM, ECTC 2004

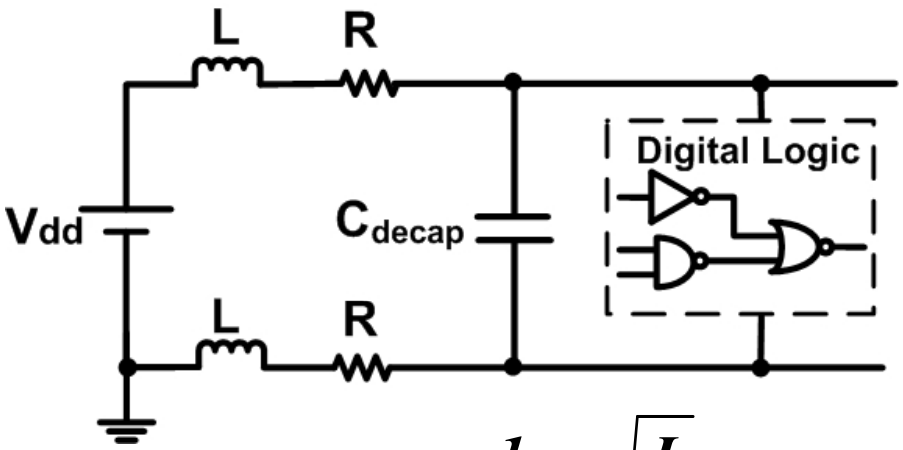


- **Typical resonant frequency is 50-300MHz**
- **Excited by processor loop operation or current spike**
- **Large magnitude and long duration affects the whole chip**



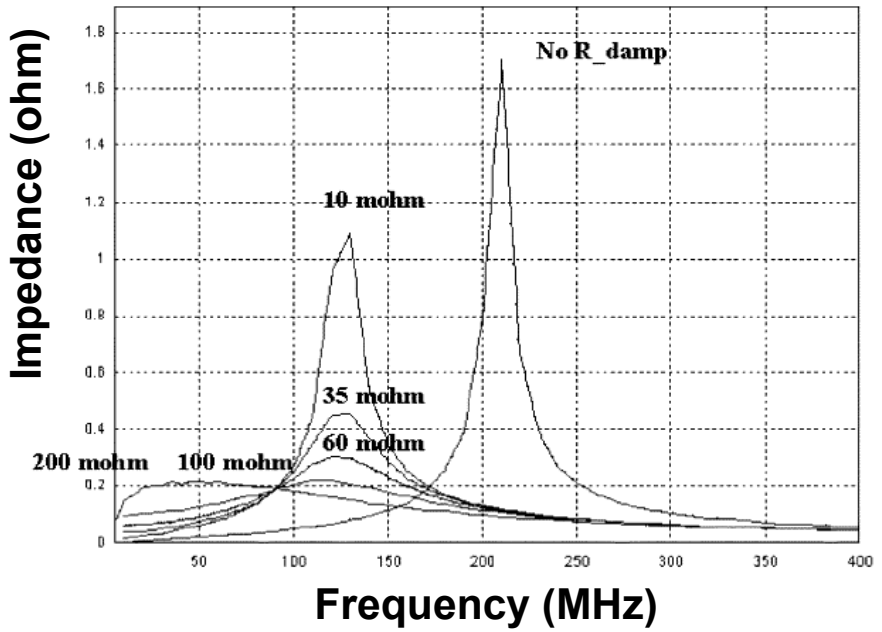
Passive Resonance Suppression

Increase on-chip decap



$$Q = \frac{1}{R_{wire}} \cdot \sqrt{\frac{L}{C}}$$

Increase on-chip resistance



G. Ji, et al., T. Adv. Packaging, 2005

- ***Q*** **factor signifies impedance peak**
- **Penalty for bringing down *Q* factor:**
  - **↑*R*: Extra *IR* drop and power**
  - **↑*C*: Area and leakage overhead**
- ***Can resonant noise be utilized to improve circuit timing?***

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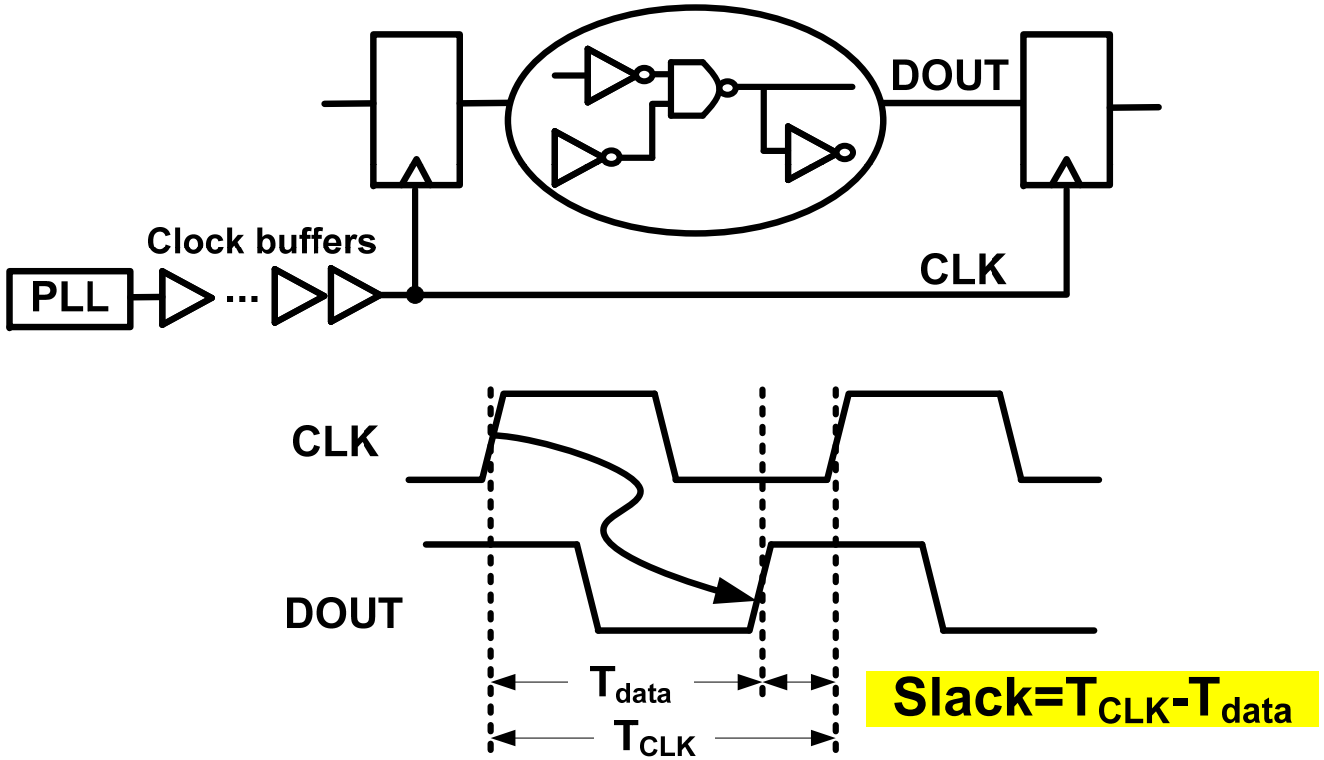
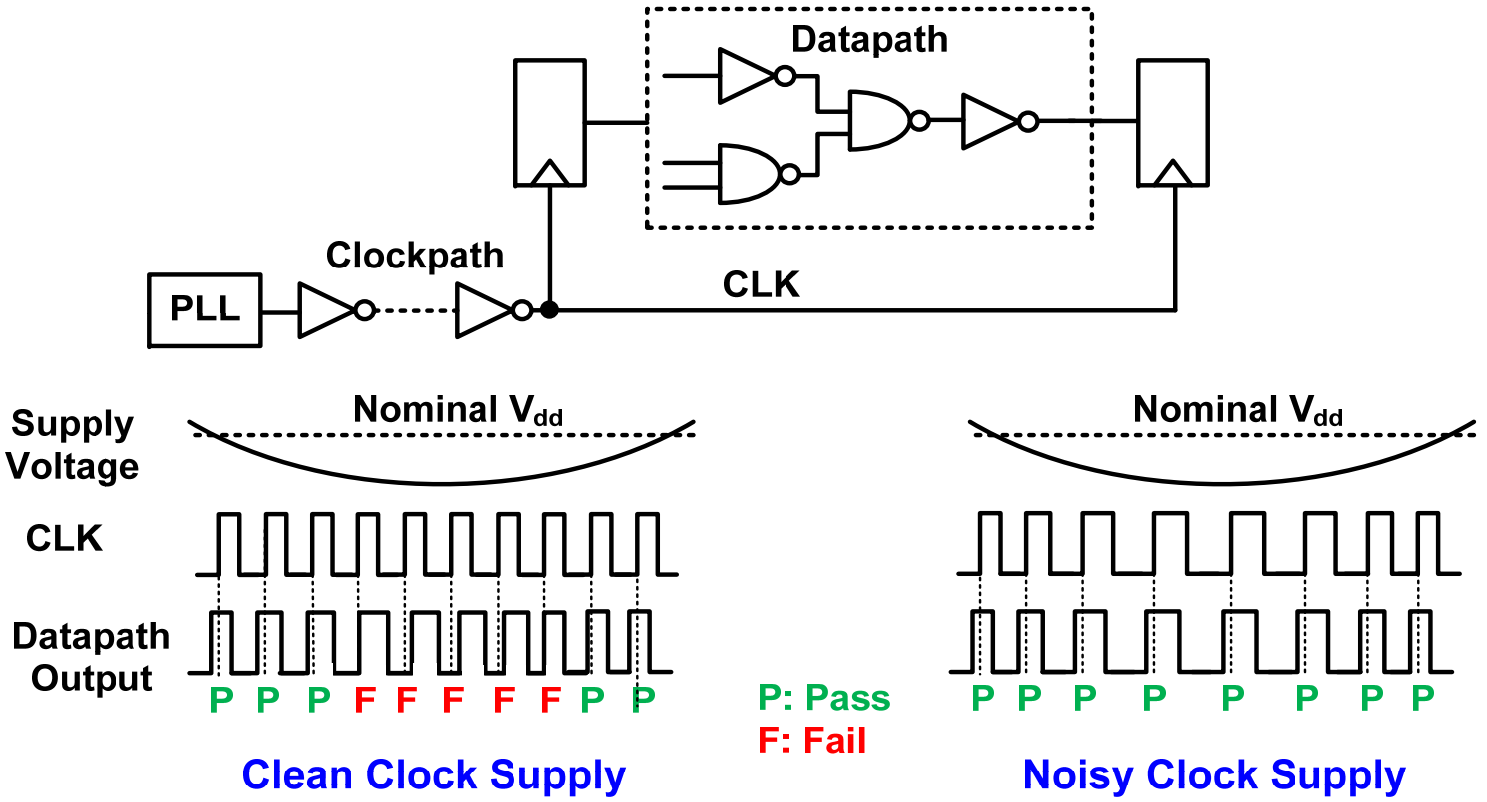
Timing Slack in Datapath

- Timing margin between clock period and datapath delay



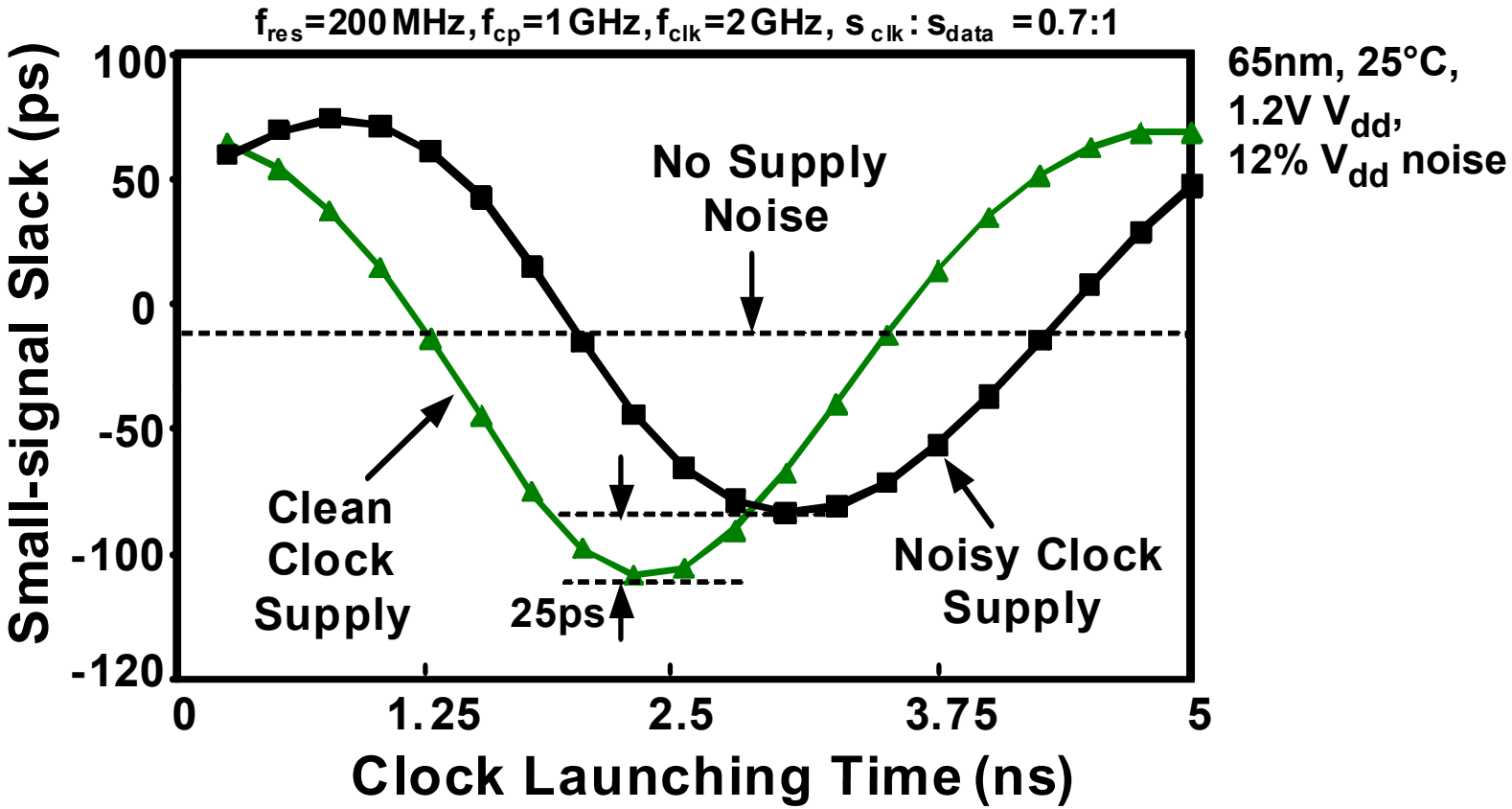
- Positive slack means correct operation

Beneficial Jitter Effect: Natural Timing Compensation Between Clock and Data



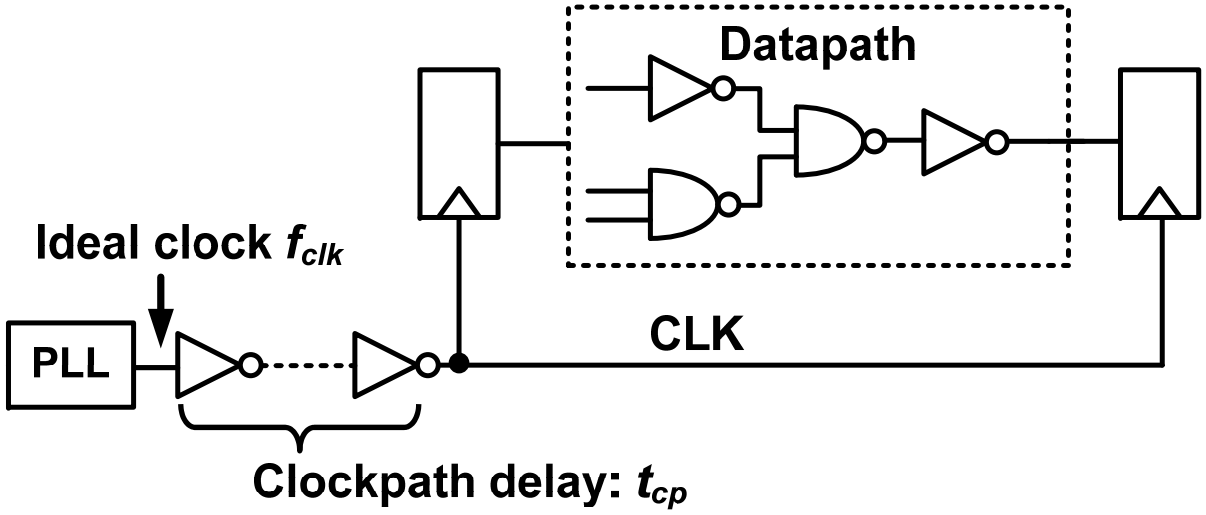
- Traditional analysis considers datapath delay only
- In reality, both datapath delay and clock period varies with supply noise

Beneficial Jitter Effect Simulation



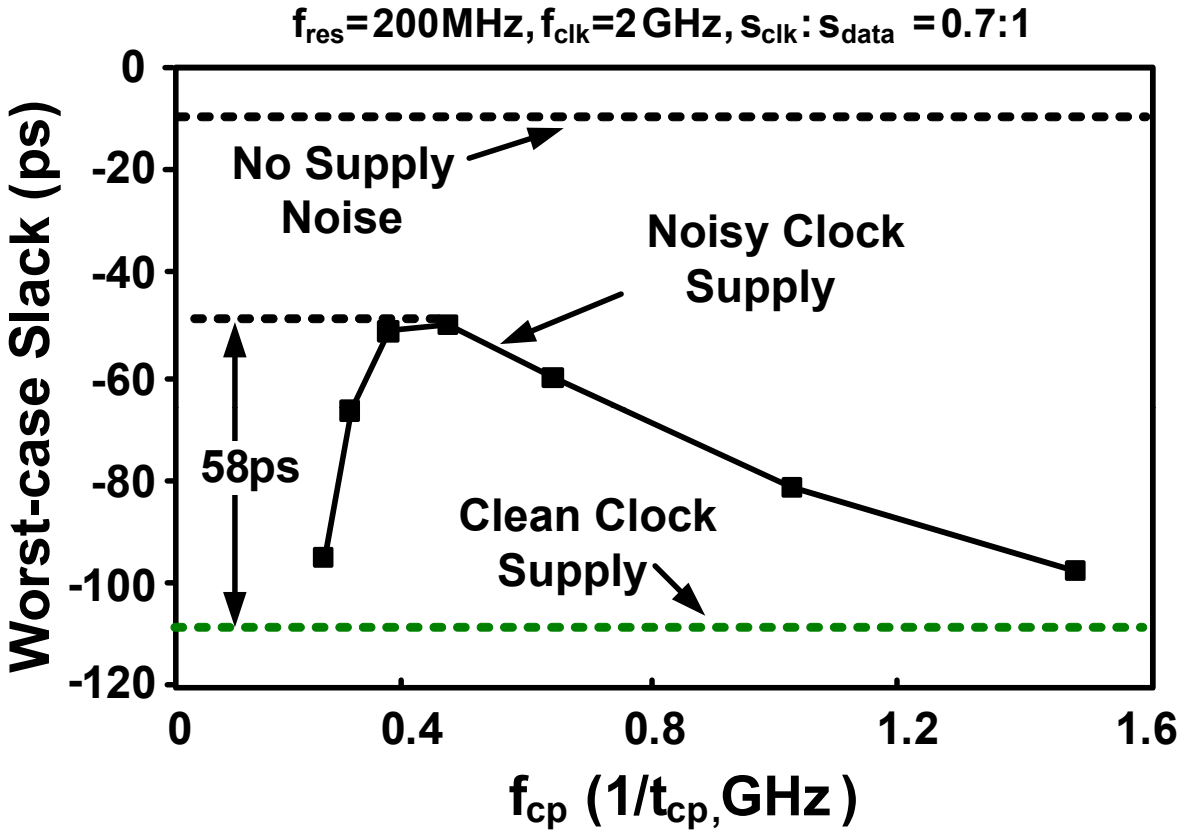
- Inherent timing compensation between clock and data
- 25ps (or 5% T_{clk}) slack improvement when considering *beneficial jitter* effect

Factors Affecting *Beneficial Jitter* Effect



- θ_{res}: Supply noise phase at clock launch
- t_{cp} or $1/f_{cp}$: Clock path delay
- s_{clk}, s_{data}: Delay sensitivity to supply
  - Change in speed with respect to supply variation
  - E.g. If 10% Vdd change causes 15% speed change, *s* is 1.5
- f_{res}: Resonant frequency

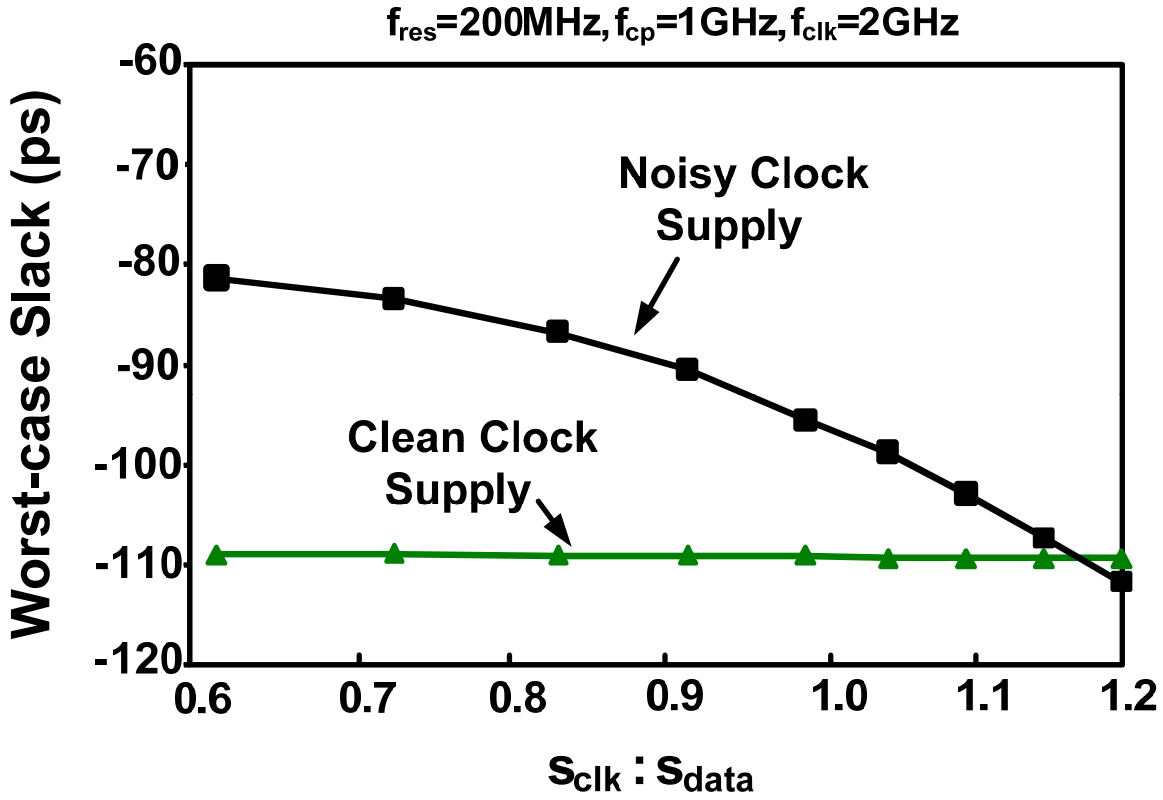
Impact of Clock Path Delay



65nm, 25°C,
1.2V V_{dd}
12% V_{dd} noise

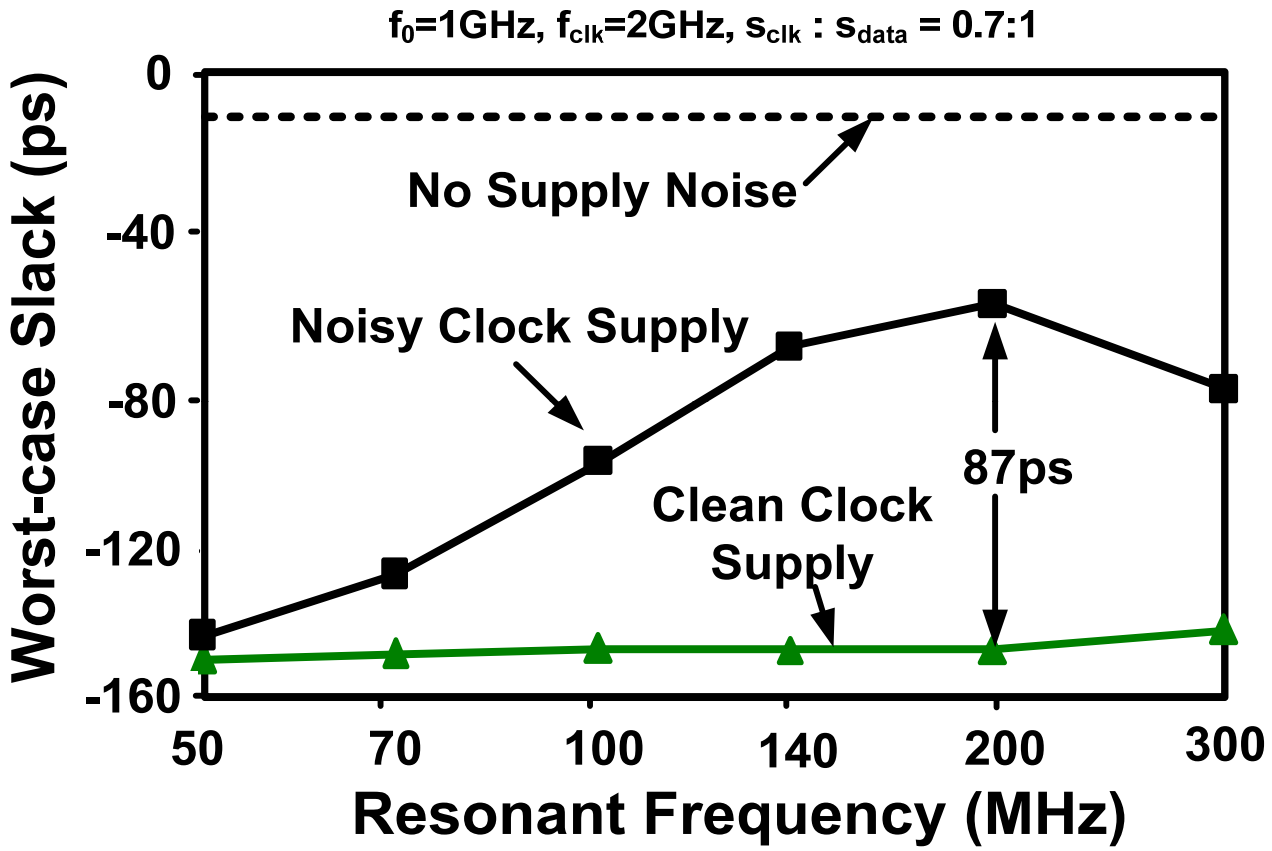
- **Optimal clock path delay exists**
  - **Small f_{cp} : Approaches clean clock case**
  - **Large f_{cp} : Average supply voltages seen by clock edges closer**
- **Up to 58ps (11.6% T_{clk}) slack improvement with proper f_{cp}**

Impact of Delay Sensitivity



- Typical clock path delay sensitivity is around 0.6 due to interconnect RC delay
- Much larger (or much smaller) sensitivity worsens timing slack

Impact of Resonant Frequency



- Beneficial jitter effect prominent in typical resonant frequency range
- Up to 87ps (11.6% T_{clk}) slack improvement

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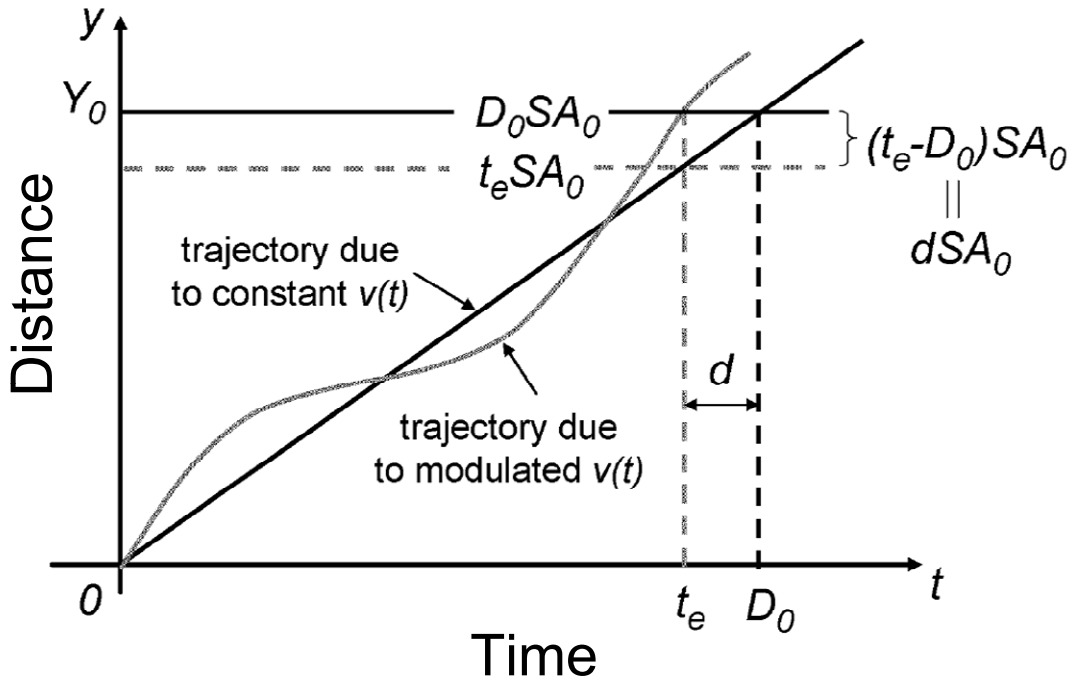
Beneficial Jitter Effect Modeling



D_0, t_e : **Nominal/actual delay**

Y_0 : **Nominal distance**

A_0, a : **DC/AC supply voltage**

S, s : **Delay sensitivity**

[WRM06] K. L. Wong, et al., JSSC 2006

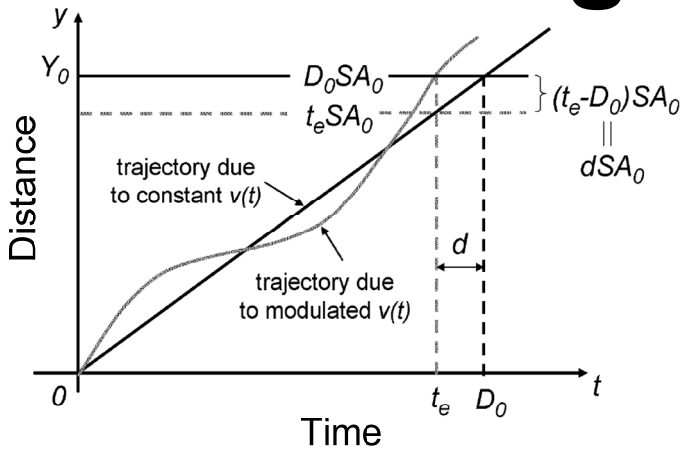
- **Adopted methodology from [WRM06]**
- **Propagating signal represented as traveling wave with speed ∝ supply voltage**
- **Propagation delay equivalent to traveling distance**

Beneficial Jitter Effect Modeling

- **Mathematical derivations:**

$$Y_0 = \int_0^{t_0} SA_0 dt = SA_0 t_0$$

$$Y_0 = \int_0^{t_e} [SA_0 + sa\cos(\omega_m t - \theta)]dt \quad \text{(i)}$$



- **Previous model [WRM06]**

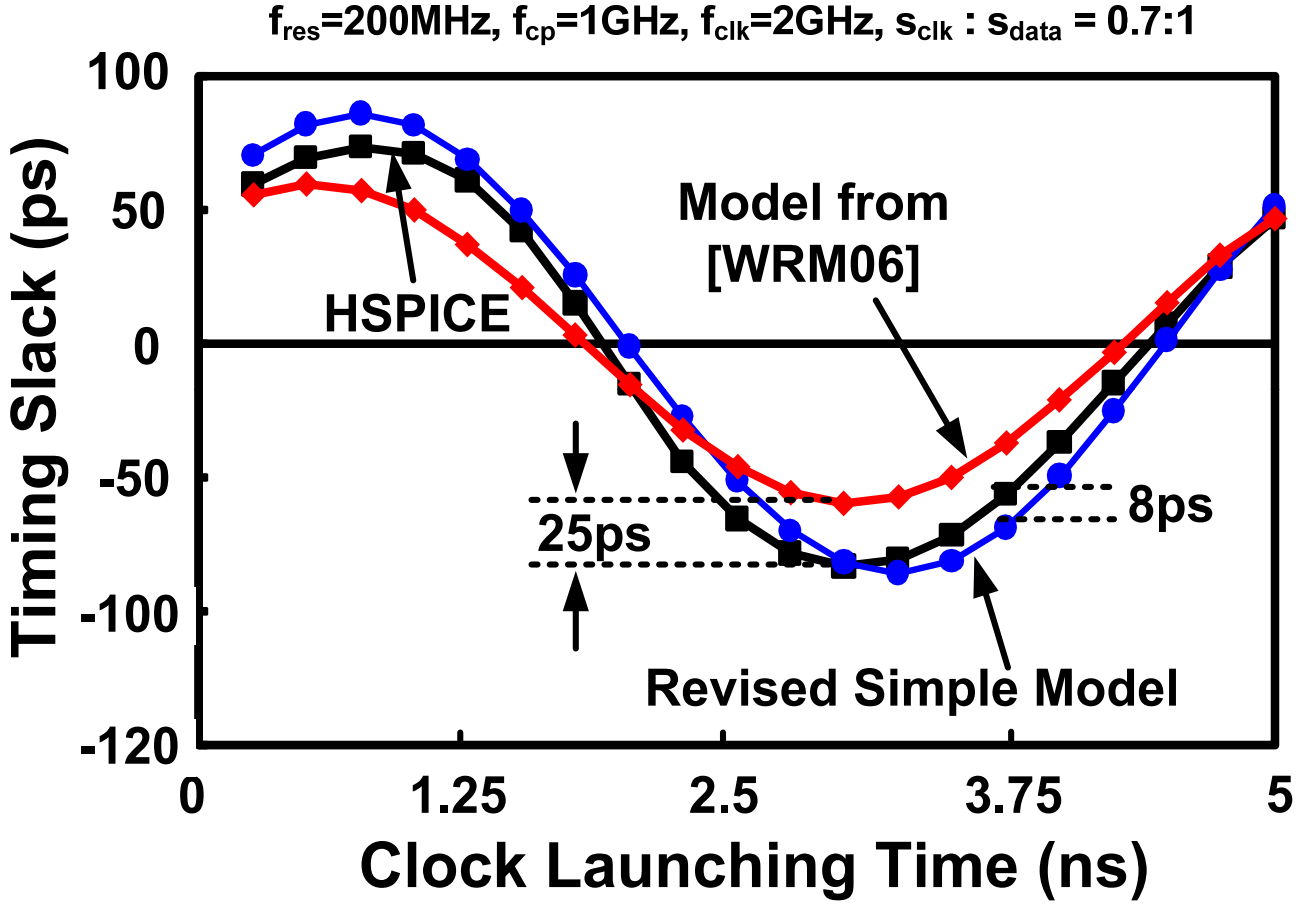
$$slack(\theta) = \frac{s_{clk}}{S_{clk}} \frac{2a}{A_0} \frac{f_{clk}}{\pi f_m} \sin\left(\frac{\pi f_m}{f_{clk}}\right) \sin\left(\frac{\pi f_m}{f_0}\right) \times \sin\left(\theta - \frac{\pi f_m}{f_0} - \frac{\pi f_m}{f_{clk}}\right) + \frac{s_{data}}{S_{data}} \frac{a}{A_0} \cos\theta$$

- **Revised simple model**

$$slack(\theta) = \frac{s_{clk}}{S_{clk}} \frac{2a}{A_0} \frac{f_{clk}}{\pi f_m} \sin\left(\frac{\pi f_m}{f_{clk}}\right) \sin\left(\frac{\pi f_m}{f_0}\right) \times \sin\left(\theta - \frac{\pi f_m}{f_0} - \frac{\pi f_m}{f_{clk}}\right) + \frac{s_{data}}{S_{data}} \frac{a}{A_0} \cos\left(\theta - \frac{\pi f_m}{f_{clk}}\right)$$

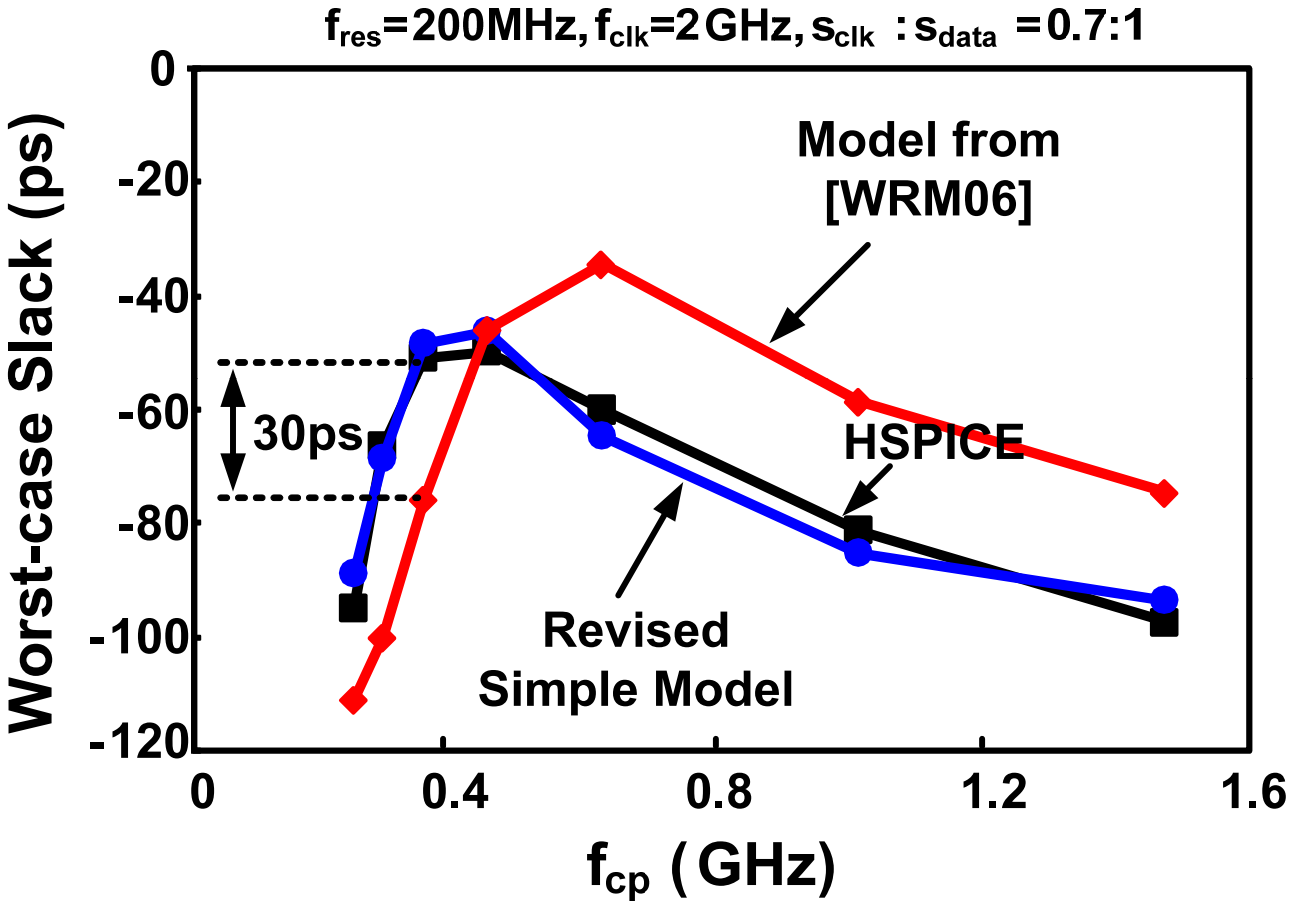
- **Revised accurate model**
  - **No closed-form expression exists**
  - **Solve non-linear equation (i) without making approximations**
  - **Follow derivation steps of simple model**

Timing Model versus HSPICE



- Confirms intrinsic compensation effect
- Reduces modeling error from 25ps to 8ps (5% to 1.6% T_{clk})

Timing Model versus HSPICE



65nm, 25°C,
1.2V V_{dd}
12% V_{dd} noise

- Revised simple model good for first order approximation
- Reduces modeling error from 30ps to 4ps (6% to 0.8% T_{clk})

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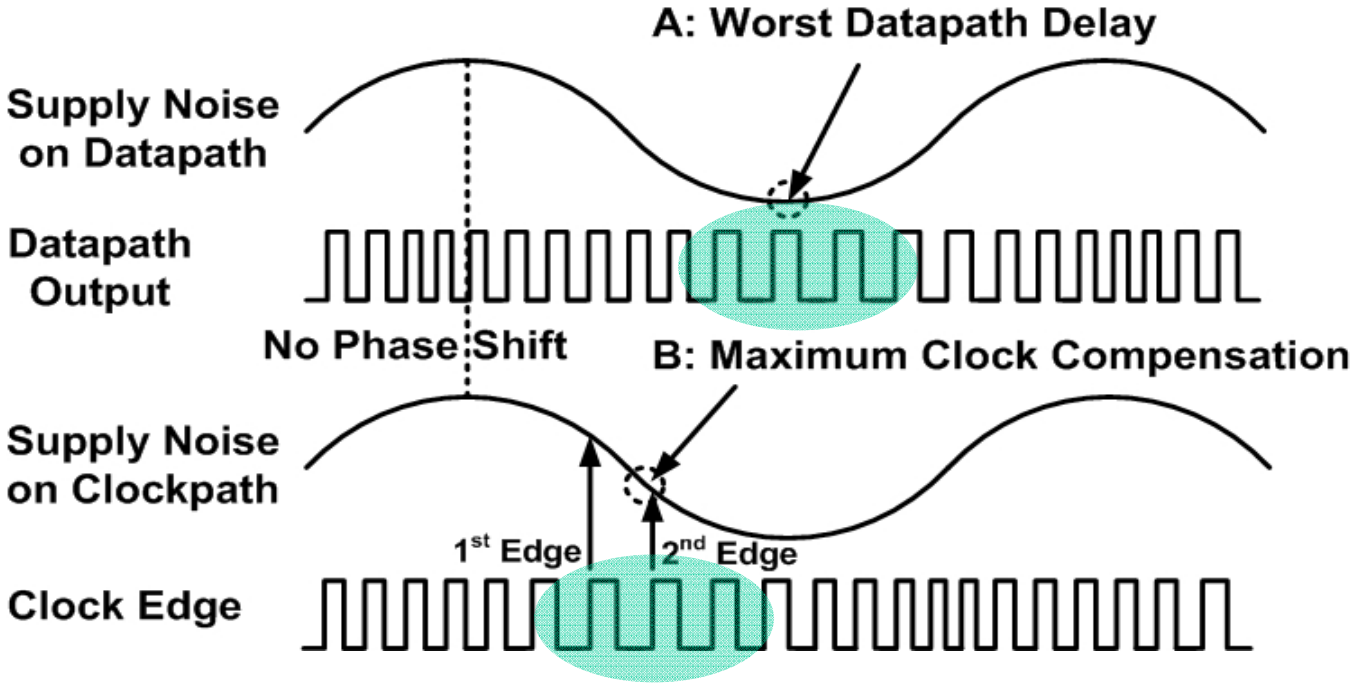
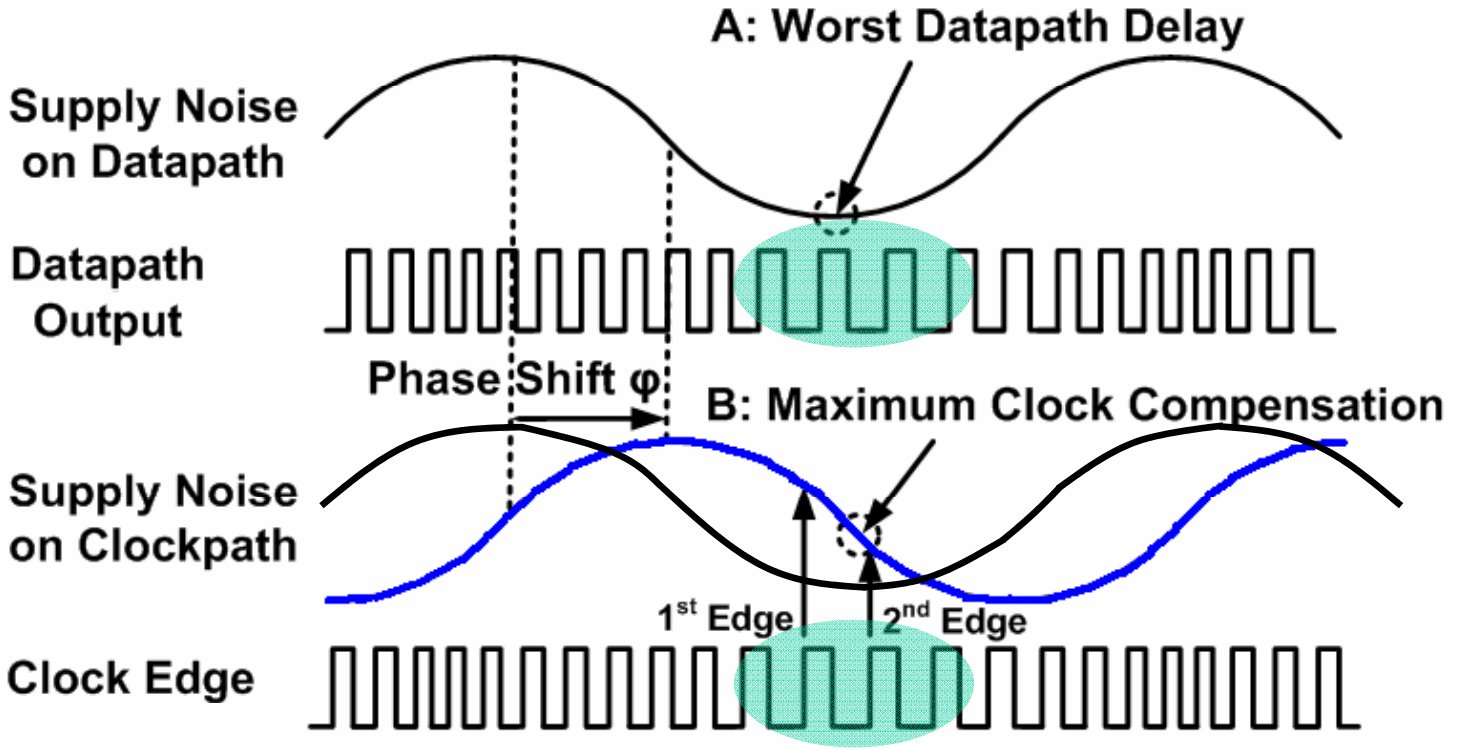
Intrinsic *Beneficial Jitter* Effect



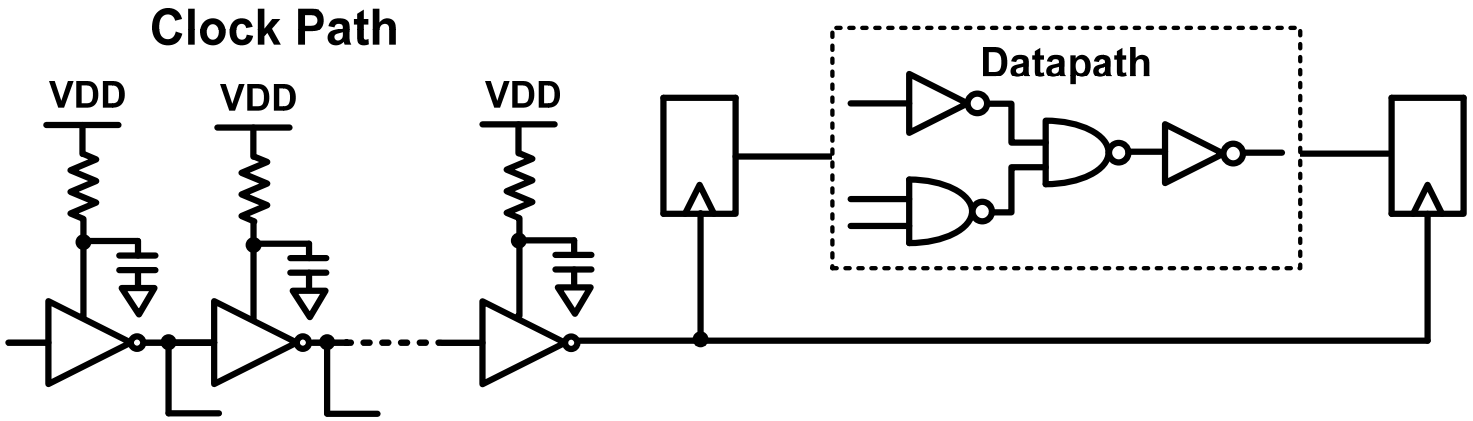
- ***Beneficial jitter*** **effect can be harnessed further**
  - **Datapath delay depends on instantaneous V_{dd} value.**
  - **Clock period depends on V_{dd} value *difference* seen by two consecutive clock edges.**
  - **Worst delay point does not coincide with max clock period point**

Enhancing *Beneficial Jitter* Effect Using Phase-Shifted Clock Distribution

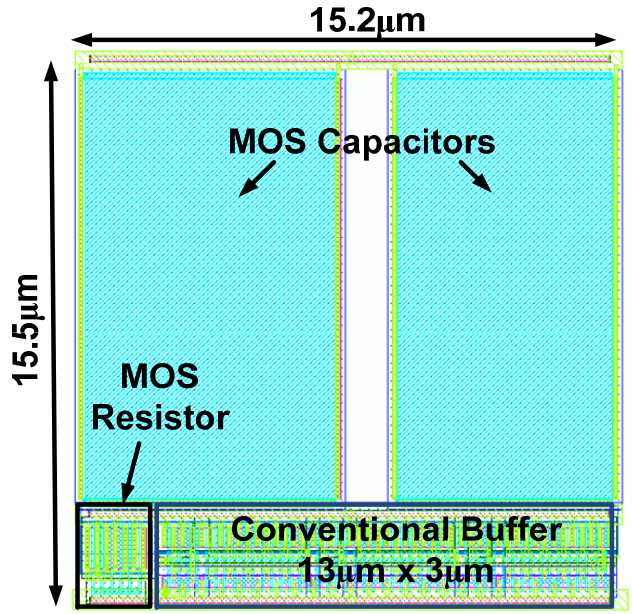


- Phase-shift the clockpath supply noise
- Clock period can be stretched out the most when the worst case datapath delay occurs

Phase-Shifted Clock Buffer Design

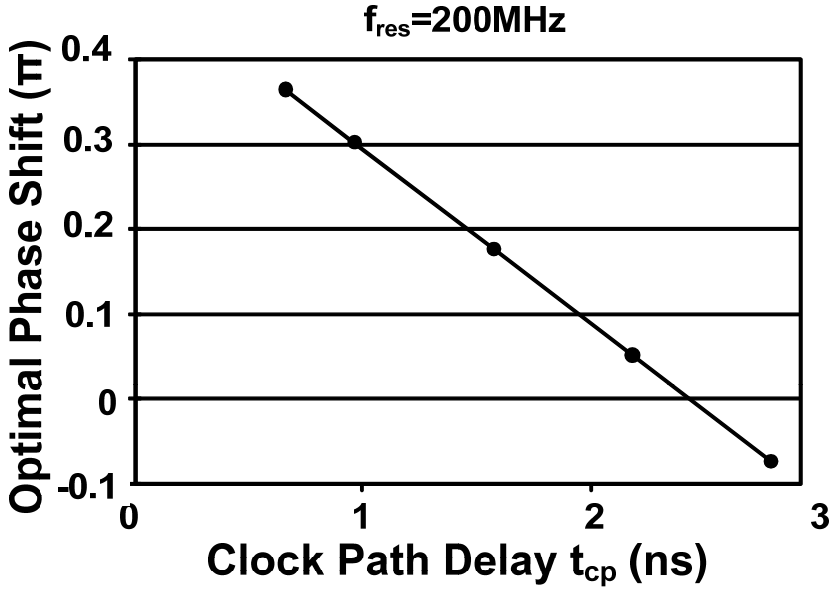


- New clock buffer with built-in *RC* filter
- Optimal *RC* value selected using the revised timing models to enhance *beneficial jitter* effect
- *IR* drop < 50mV



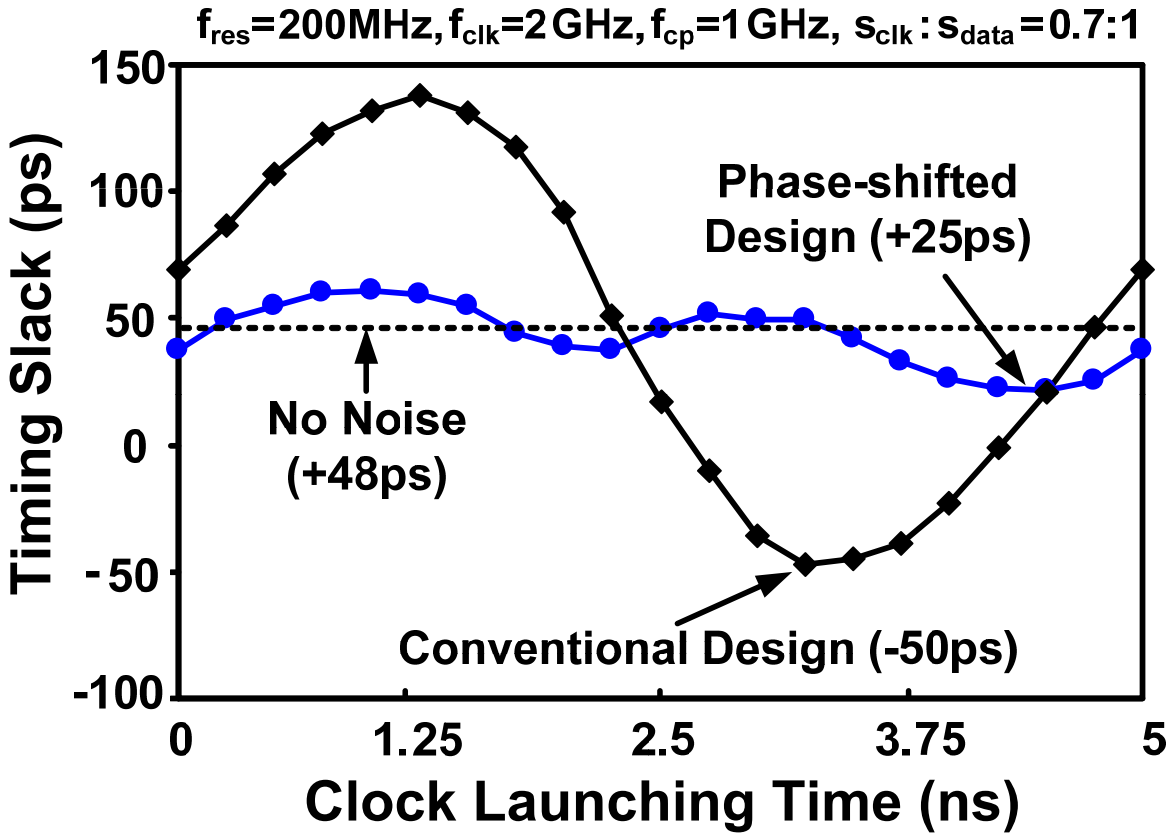
Calculation of Optimal Phase Shift

$$\frac{f_{res}\pi}{f_{cp}} + \phi_{shift} = \frac{\pi}{2}$$



- **Intuitive explanation**
  - $\frac{f_{res}\pi}{f_{cp}}$ **: Phase difference caused by clock path delay**
  - $\frac{\pi}{2}$ **: Phase difference between largest slope point and lowest supply point**
- **Revised simple model used assuming ideal phase shift**

Timing Slack Improvement



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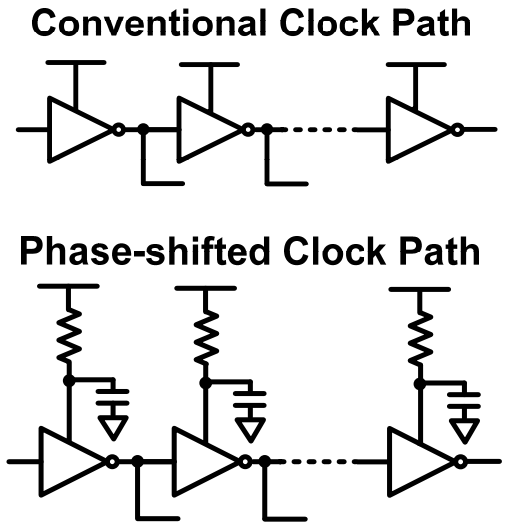
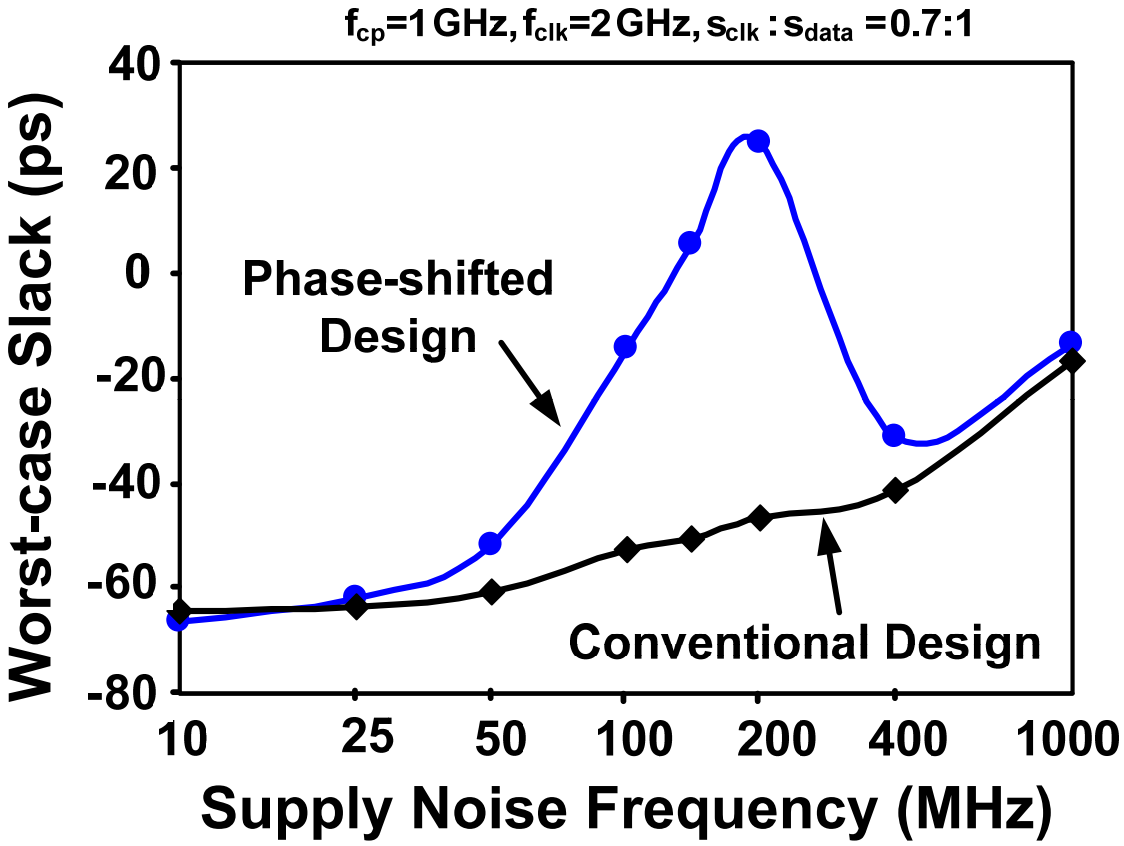


- 75ps (or 15% T_{clk}) slack improvement
- Phase-shifted clock distribution keeps timing slack positive ensuring correct operation

Effectiveness for Wide Band Noise

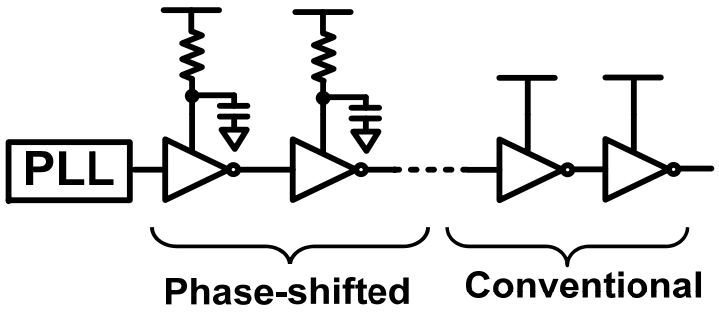


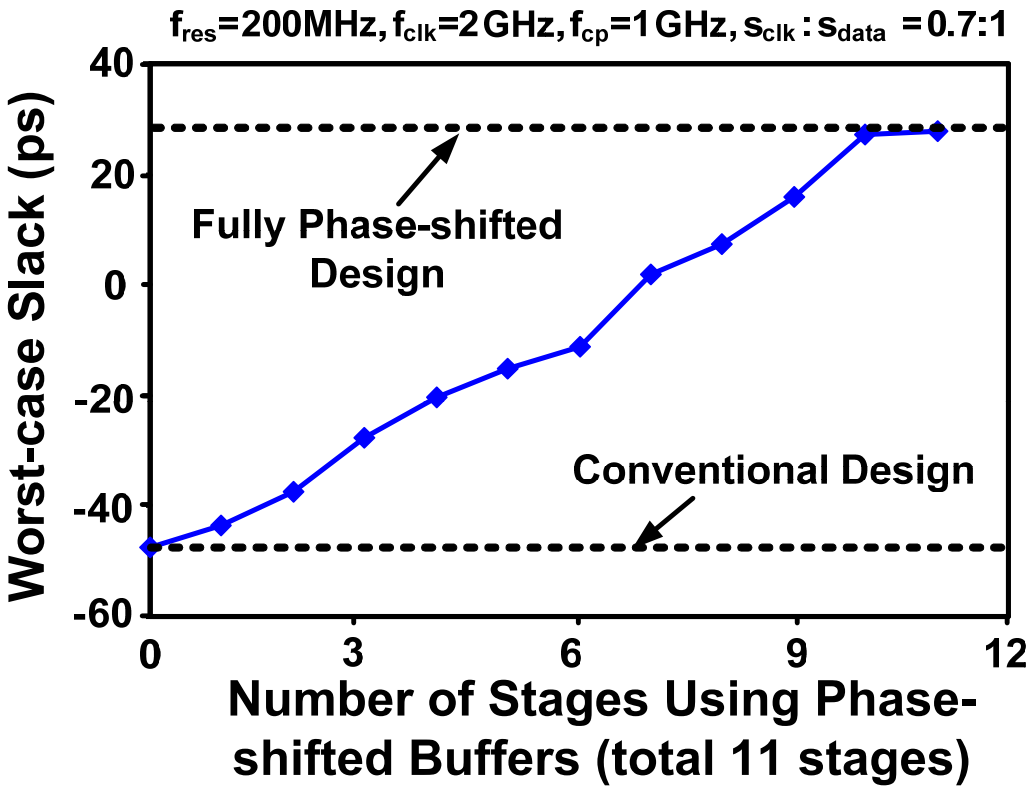
65nm, 25°C,
1.2V V_{dd}
12% V_{dd} noise

- Phase-shifted design most effective for typical resonant frequency range
- Does not affect performance for other noise frequencies

Partial Phase-Shifted Clock Distribution

65nm, 25°C, 1.2V V_{dd}
12% V_{dd} noise

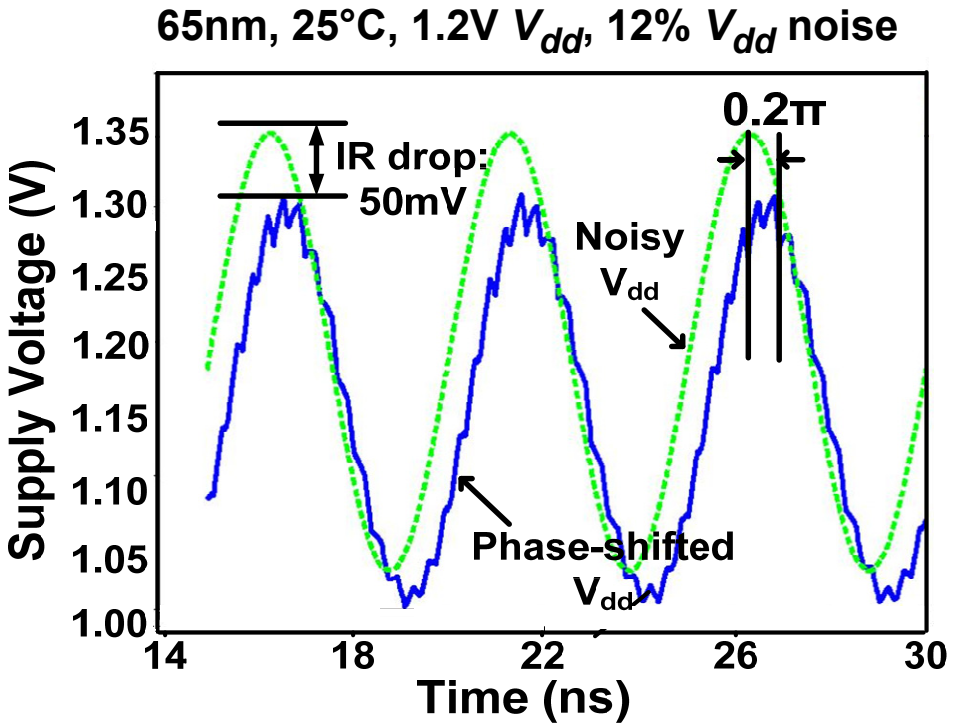




- Using phase-shifted clock buffers only in the global clock network still improves timing slack
- Effectiveness of phase-shifting technique can be traded off for die area

Results Summary

Resonant Noise	200MHz
Clock Frequency	2GHz
Intrinsic Decap C*	6nF
Package Inductance L*	0.1nH
Load Current*	1A
R in RC Filter	300 Ω
C in RC Filter	2pF
Phase Shift	0.2π
Slack Improvement	75ps (15% T_{clk})
Equivalent Decap	24nF
Decap Saving	80%



*The L, C and load current values are scaled down proportionally to account for the smaller clock tree used in our test setup.

Conclusions

- Resonant noise is an important concern for power supply network designs
- Inherent timing compensation between clock and data improves timing slack
- Timing models proposed to accurately describe this *beneficial jitter* effect
- Phase-shifted clock distribution proposed
  - Enhances *beneficial jitter* effect
  - Slack improvement by 15% T_{clk}
  - Performance equivalent to 5X larger decap