Enhancing *Beneficial Jitter* Using Phase-Shifted Clock Distribution

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ABSTRACT

Clock jitter is generally considered undesirable but recent publications have shown that it can actually improve the timing margin. This paper investigates the "beneficial jitter" effect and presents an accurate analytical model which is verified with HSPICE. Based on our model, a phase-shifted clock distribution technique is proposed to enhance the beneficial jitter effect. By having an optimal phase shift between the supply noise and the clock period, the timing margin can be improved by 2.5X to 15% of the clock period. The benefit of the proposed technique is equivalent to that of having a 5X larger decoupling capacitor.

Categories and Subject Descriptors

B.7.1 [Integrated Circuits]: Types and Design Styles - *Microprocessors and microcomputers; VLSI (very large scale integration*)

General Terms

Management, Performance, Design

Keywords

Resonant supply noise, Clock jitter

1. INTRODUCTION

Power supply noise is considered to be one of the major causes of performance degradation and device reliability concerns [1]. Supply noise caused by on-chip current introduces delay variation in datapaths, as well as jitter in clock paths. As a result, the launched data from one stage in a pipeline can no longer be guaranteed to be captured by the next clock edge within a given timing window (i.e., the clock cycle) leading to a timing failure [2]. Significant efforts have been made to alleviate the impact of supply noise on timing errors. A popular method to reduce the supply noise is to add passive or active decoupling components. For example, Pant proposed to optimize the placement of decoupling capacitors (decaps) by using activity profiles based on architecture simulators [3]. Xu proposed an active damping circuit to reduce the resonant noise in the supply grids [4]. Gu proposed an active decap circuit to reduce the decap area and power [5]. All of these techniques to regulate supply noise have power and area overhead. Meanwhile, several circuit techniques and design methodologies have been developed to reduce the clock jitter. For instance, Mansuri proposed an adaptive delay compensation circuit for clock buffers to reduce their sensitivity to supply noise [6]. Chen developed closed-form formulas for jitter prediction and proposed a clock buffer chain to minimize the jitter [7]. More recently, adaptive or error correction circuits were developed to perform jitter compensation on-the-fly. Examples include the noise-adaptive delay line used in Intel's Foxton processor and the error correction flip-flop which can be re-triggered upon the detection of error proposed by Yasuda [8-9].

On-chip power supply noise consists of IR and Ldi/dt noise components. Recent publications show that the resonant supply noise typically in the 50-300MHz range can become dominant once excited [10-11]. Fig. 1(a) shows the supply impedance of an IBM PowerPC microprocessor [12]. A large impedance peak is observed at 250MHz, which is referred to as the resonant frequency. This noise component is caused by the resonance between the package inductance and die capacitance. Because of the large impedance, a small current at the resonant frequency will excite a large supply fluctuation. Resonant noise can be excited during microprocessor loop operations near the resonant frequency or a sudden current spike caused by the clock signal or a processor wakeup. The latter case introduces the so called "first-droop noise" which is shown in Fig. 1(b) [13-14]. Due to the large magnitude and long duration (typically 10s of clock cycles), the resonant noise has been considered as the worst-case supply noise and has motivated a surge of circuit techniques to deal with this issue in recent years [4, 12, 15]. For example, a slow clock ramping circuit was developed in [12] to avoid a dramatic current transient which may trigger the first-droop noise.

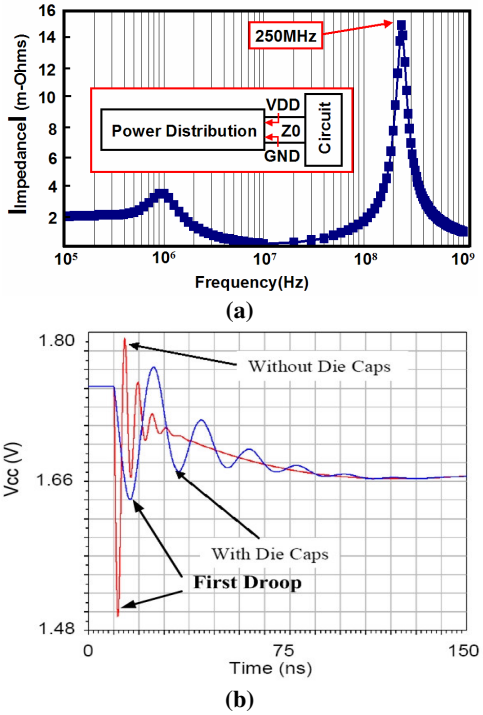

Fig. 1 (a) A typical on-chip power supply network impedance shows a resonance at 250MHz [12]. (b) First droop noise [13].

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Wong et al. recently published an intriguing paper showing the potential delay compensation between clock path and datapath under the influence of mid-frequency resonant noise [13-14]. It was shown that the jitter induced by supply noise helps to improve the delay margin on the datapath. We refer to this effect as "beneficial jitter" in this paper. Fig. 2 illustrates the concept of beneficial jitter through clock/data compensation. The conventional design criterion tells us that in order to prevent timing violations in a typical pipelined datapath, the clock period has to be greater than the critical path delay under the worst-case supply noise. In other words, the timing slack, defined as the clock period minus the actual circuit delay, has to be kept positive. That is:

$$slack = T_{clk} - T_{data} > 0 \quad (1)$$

where T_{clk} is the clock period and T_{data} is the datapath delay. Conventional design methodologies only address the increased delay on datapaths caused by the worst-case supply droop in order to guarantee a positive slack. However, as shown in Fig. 2, with a noisy supply on the clock path, the clock period is also stretched due to the increased clock buffer delay leading to extra timing margin to compensate the slowdown in the datapath. Thus the chance of timing failure under supply droop is reduced. This observation indicates that ignoring the clock/data compensation effect will lead to pessimistic performance estimations or overdesigned decaps. Although an analytical model was derived previously for this effect [14], no circuit simulation results were used to backup the theory. Our evaluation in this paper shows that the previous model is not accurate in predicting the compensation from the clock path due to a number of simplifications. A clock supply filtering scheme was also proposed in [14] to reduce the clock jitter. However, the principle of using a filtered clock was not explained and the selection of clock supply filter was not discussed. Another major shortcoming of the prior technique is that the entire clock tree has to share the filtered supply increasing the area penalty due to the additional supply routing as well as making the timing compensation effect highly unpredictable between the distributed buffers.

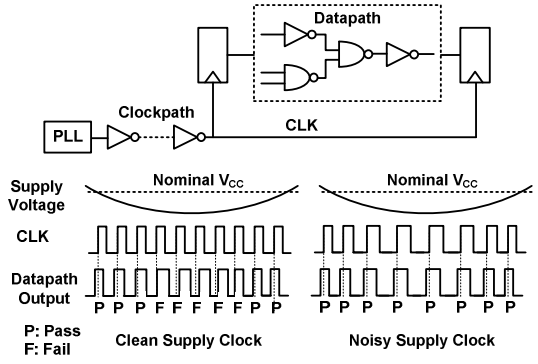


Fig. 2 Illustration of beneficial jitter effect. The clock edge stretches in response to the noisy supply voltage compensating for the increased datapath delay. On the contrary, a clock path with a clean supply has a fixed clock period which can lead to a timing failure.

Based on the preliminary observations in [13-14], this work explores design methodologies to enhance the beneficial jitter effect to prevent timing failure under supply noise. The contributions of this paper with respect to previous work are as follows:

- The beneficial jitter effect has been verified and closed form expressions for slack improvement and optimum clock tree propagation delay are derived. The accuracy of the derived model has been significantly improved compared with those in previous publications.
- A phase-shifted clock distribution scheme is proposed to enhance the beneficial jitter effect. Unlike prior art, each clock buffer contains its own RC filter which makes the clock tree design simple and modular. The optimal phase shift based on our analytical model was used to achieve the maximum timing compensation.

The remainder of this paper is organized as follows. In section 2 we derive a closed form formula for the worst-case timing slack considering the clock/data compensation effect, which is more accurate compared with the previous work. In section 3 we derive an analytical model for the proposed phase-shifted clock distribution technique. Equations for slack improvement and optimal phase shift are formulated and verified by simulation results. Note that all HSPICE simulation results in this paper are based on an industry level 65nm CMOS technology with a 1.2V supply voltage. Finally, we summarize our work in section 4.

2. MODELING BENEFICIAL JITTER EFFECT

An analytical model for the clock/data compensation effect was derived in [14]. In this section, we will show that the previous model does not match well with HSPICE simulation results due to several simplifications. An improved model is derived in this work which is further verified with simulation results.

A signal in a digital circuit (e.g., clock path or datapath signals) can be modeled as a signal wave propagating through a fixed length medium at a velocity which is proportional to the instantaneous supply noise. Fig. 3 illustrates the signal propagation model for the delay on a clock path or a datapath [14].

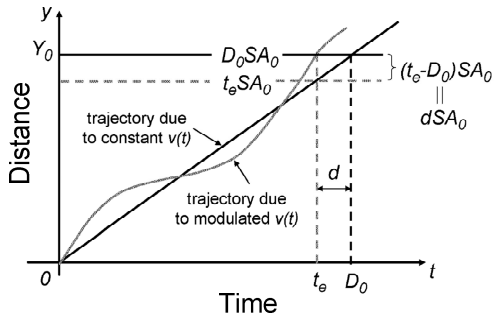


Fig. 3 Delay model for clock path or datapath [14].

The velocity of the traveling wave can be expressed as:

$$v(t) = SA_0 + sa\cos(\omega_m t - \theta) \quad (2)$$

where S is the large-signal sensitivity of $v(t)$ with respect to supply, s is the small-signal sensitivity to supply, A_0 is the DC value of supply, a is the AC amplitude of supply, ω_m is the supply noise frequency, and θ is the phase of the supply noise when the signal is issued. Integrating the velocity over the total traveling time t_e gives us the total distance Y_0:

$$Y_0 = D_0SA_0 = \int_0^{t_e} [SA_0 + sa\cos(\omega_m t - \theta)]dt \quad (3)$$

$$t_eSA_0 + \frac{sa}{\omega_m}(\sin(\omega_m t_e - \theta) - \sin(-\theta)) = D_0SA_0 \quad (4)$$

Here, D_0 is the nominal traveling time of the signal. By defining the small-signal delay as $d=t_e-D_0$, we get:

$$d = -\frac{2sa}{SA_0\omega_m}\sin(\frac{\omega_m t_e}{2})\cos(\frac{\omega_m t_e}{2} - \theta) \quad (5)$$

Using this expression, we can calculate the change in clock period under supply noise by taking the difference between the traveling times of two successive clock edges. The clock period modulation can be calculated as:

$$\Delta p = d[n] - d[n-1] = \frac{4 s_{clk} a}{S_{clk} A_0 \omega_m} sin(\frac{\theta_{n-1} - \theta_n}{2}) sin\frac{\omega_m t_e}{2} sin(\frac{\omega_m t_e - \theta_n - \theta_{n-1}}{2}) \quad (6)$$

where $d[n]$ and $d[n-1]$ are the traveling time of the n^{th} and $(n-1)^{th}$ *clock edges* derived from equation (5). θ_n and θ_{n-1} are the phases at which the corresponding clock edges enter the clock path.

Approximating $\theta_n - \theta_{n-1} = \omega_m / f_{clk}$ and $t_e = D_0 = 1/f_0$ where $f_{clk}(=1/T_{clk})$ is the clock frequency and f_0 is the inverse of the nominal clock path delay, we find the clock period variation as follows:

$$\Delta p \approx \frac{2 s_{clk} a f_{clk}}{S_{clk} A_0 \pi f_m} sin(\frac{\pi f_m}{f_{clk}}) sin\frac{\pi f_m}{f_0} sin(\theta_n - \frac{\pi f_m}{f_0} - \frac{\pi f_m}{f_{clk}}) \quad (7)$$

where Δp has been normalized to the clock frequency f_{clk}.

The datapath delay can be derived similarly using equation (5):

$$d = -\frac{2 s_{data} a}{T_{clk} S_{data} A_0 \omega_m} \sin(\frac{\omega_m t_e}{2}) \cos(\frac{\omega_m t_e}{2} - \theta) \quad (8)$$
$$\approx -\frac{2 s_{data} a}{T_{clk} S_{data} A_0 \omega_m} \frac{\omega_m T_{clk}}{2} \cos(\frac{\omega_m t_e}{2} - \theta) \approx -\frac{s_{data} a}{S_{data} A} \cos\theta.$$

Here $\omega_m t_e/2$ in the *cos()* function is ignored because it is relatively small. Finally, the small-signal slack due to clock/data compensation can be calculated by finding the difference in the delay variations on the clock path and datapath as follows:

$$slack(\theta) = \Delta p - d = \frac{s_{clk}}{S_{clk}} \frac{2a}{A_0} \frac{f_{clk}}{\pi f_m} \sin(\frac{\pi f_m}{f_{clk}}) \sin(\frac{\pi f_m}{f_0}) \times \sin(\theta - \frac{\pi f_m}{f_0} - \frac{\pi f_m}{f_{clk}}) + \frac{s_{data}}{S_{data}} \frac{a}{A_0} \cos\theta \quad (9)$$

Equation (9) was used in [14] as a closed-form solution to evaluate the clock/data compensation effect. Note that the second term is the slack caused by delay on the datapath only and has the most negative value of $\frac{s_{data}}{S_{data}} \frac{a}{A_0}$. A negative slack means that the timing margin has been reduced compared with the nominal condition. Thus the design goal is to minimize the most negative, (or worst-case) slack in (9).

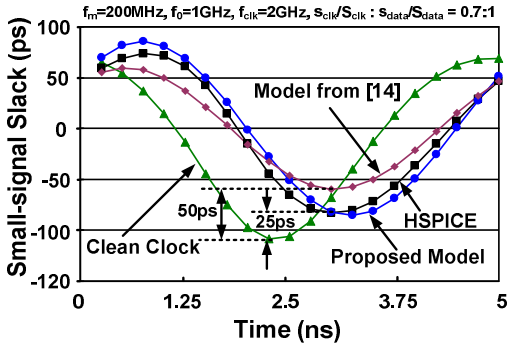


Fig. 4 Slack variation in time domain for different models.

A simplified clock tree was designed to verify the results from equation (9). A clock path with 26 stages of inverters was used to produce a clock delay of 1ns or f_0 of 1GHz. Another 16 stages of inverters were chained to represent a datapath with a frequency of 2GHz which is also the clock frequency f_{clk}. A supply noise at f_m=200MHz is applied to the supply representing the dominant resonant, or first-droop noise. Because the clock buffers drive interconnects in the datapath, the clock path has lower delay sensitivity with respect to supply noise. s_{clk}/S_{clk} : s_{data}/S_{data}=0.7:1 was found in this work which is consistent with what was reported in [14]. Fig. 4 shows that the previous model in (9) exhibits a relatively large discrepancy when compared with HSPICE simulations. The improved worst-case slack due to the beneficial jitter from HSPICE simulation is about 25ps (5% of clock period) which is smaller than the 50ps (10% of clock period) predicted by equation (9). Such a discrepancy comes from several simplifications used during the derivation. Our further evaluation indicates that the approximation of ignoring $\omega_m t_e/2$ in equation (8) introduces a significant error.

To improve the accuracy of the closed-form model, we consider the term $\omega_m t_e/2$ in (8). As a result, equation (9) becomes:

$$slack(\theta) = \frac{s_{clk}}{S_{clk}} \frac{2a}{A_0} \frac{f_{clk}}{\pi f_m} sin(\frac{\pi f_m}{f_{clk}}) sin(\frac{\pi f_m}{f_0}) \times sin(\theta - \frac{\pi f_m}{f_0} - \frac{\pi f_m}{f_{clk}}) + \frac{s_{data}}{S_{data}} \frac{a}{A_0} cos(\theta - \frac{\pi f_m}{f_{clk}}) \quad (10)$$

Fig. 4 verifies that the slack value predicted from equation (10) has significantly improved the accuracy of the analytical model.

Since θ is a time-varying variable, (10) does not directly indicate the worst-case slack which is most important to a circuit designer. To find the maximum slack values, we convert (10) to:

$$\begin{aligned} slack(\theta) &= \frac{s_{clk}}{S_{clk}} \frac{2a}{A_0} \frac{f_{clk}}{\pi f_m} \sin(\frac{\pi f_m}{f_{clk}}) \sin(\frac{\pi f_m}{f_0}) \\ &\times (\sin(\theta)\cos(\frac{\pi f_m}{f_0} + \frac{\pi f_m}{f_{clk}}) - \cos(\theta)\sin(\frac{\pi f_m}{f_0} + \frac{\pi f_m}{f_{clk}})) \\ &+ \frac{s_{data}}{S_{data}} \frac{a}{A_0} (\cos(\theta)\cos(\frac{\pi f_m}{f_{clk}}) + \sin(\theta)\sin(\frac{\pi f_m}{f_{clk}})) \\ &= A\sin\theta - B\cos\theta = \sqrt{A^2 + B^2}\, \sin(\theta + \phi) \end{aligned} \quad (11)$$

where

$$A = \frac{s_{clk}}{S_{clk}} \frac{2a}{A_0} \frac{f_{clk}}{\pi f_m} sin(\frac{\pi f_m}{f_{clk}}) sin(\frac{\pi f_m}{f_0}) cos(\frac{\pi f_m}{f_0} + \frac{\pi f_m}{f_{clk}}) + \frac{s_{data}}{S_{data}} \frac{a}{A_0} sin(\frac{\pi f_m}{f_{clk}})$$

$$B = \frac{s_{clk}}{S_{clk}} \frac{2a}{A_0} \frac{f_{clk}}{\pi f_m} sin(\frac{\pi f_m}{f_{clk}}) sin(\frac{\pi f_m}{f_0}) sin(\frac{\pi f_m}{f_0} + \frac{\pi f_m}{f_{clk}}) - \frac{s_{data}}{S_{data}} \frac{a}{A_0} cos(\frac{\pi f_m}{f_{clk}})$$

$$\phi = a\tan(\frac{-B}{A})$$

Now, the worst-case slack in equation (11) can be found from the magnitude of that equation:

$$|slack_{wc}| = \sqrt{A^2 + B^2} = \sqrt{\begin{aligned} &4(\frac{s_{clk}}{S_{clk}})^2 (\frac{a}{A_0})^2 (\frac{f_{clk}}{\pi f_m})^2 sin^2(\frac{\pi f_m}{f_{clk}}) sin^2(\frac{\pi f_m}{f_0}) + (\frac{s_{data}}{S_{data}} \frac{a}{A_0})^2 \\ &- 4\frac{s_{clk}}{S_{clk}} \frac{s_{data}}{S_{data}} (\frac{a}{A_0})^2 \frac{f_{clk}}{\pi f_m} sin(\frac{\pi f_m}{f_{clk}}) sin^2(\frac{\pi f_m}{f_0}) \end{aligned}} \quad (12)$$

It is important to realize that the interplay between the clock and data can either improve or degrade the timing slack depending on the phase between the signals and the supply noise. If we compare the clean clock and the noisy clock results in Fig. 4, the slack is improved for the earlier noise cycle while for the rest of the time, the slack is actually worsened. However, the compensation between the clock and data is beneficial for the worst-case slack $|slack_{wc}|$ which is more critical. The smaller the $|slack_{wc}|$ is, the less performance degradation the supply noise will inflict. Because f_{clk} (>2GHz) is much higher than f_m (<300MHz), $sin(\pi f_m / f_{clk})$ can be approximated as $\pi f_m / f_{clk}$. So (12) can be further simplified to:

$$|slack_{wc}| = \sqrt{4(\frac{s_{clk}}{S_{clk}})(\frac{a}{A_0})^2 sin^2(\frac{\pi f_m}{f_0})(\frac{s_{clk}}{S_{clk}} - \frac{s_{data}}{S_{data}}) + (\frac{s_{data}}{S_{data}} \frac{a}{A_0})^2} \quad (13)$$

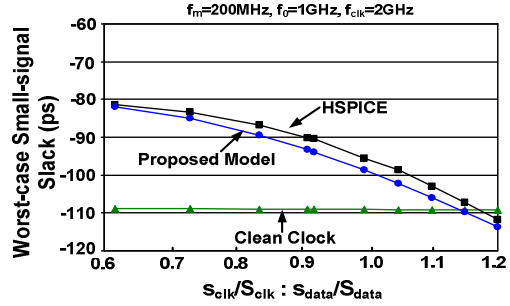
The second term inside the square root of (13) models the slack degradation with a clean clock while the first term models the

compensation effect from the clock path. Equation (13) can be used by circuit designers to optimize the effect of the clock/data compensation. Because f_m is determined by the package and f_{clk} has always been pushed toward limits, the parameters that can be adjusted to minimize the $|slack_{wc}|$ are clock propagation delay f_0, clock path sensitivity s_{clk}/S_{clk} and datapath sensitivity s_{data}/S_{data}. Equation (13) indicates that compared with a clean clock case, the slack is improved only when $s_{clk}/S_{clk} < s_{data}/S_{data}$, which is usually true because of the interconnect RC in the clock path. Fig. 5(a) shows the worst-case slack variation versus relative ratio between delay sensitivities of the clock path and the datapath. The result follows the trend predicted by (13). Smaller clock path sensitivity produces better compensation. The minor discrepancy between simulation and model comes from the simplification used when deriving (13).

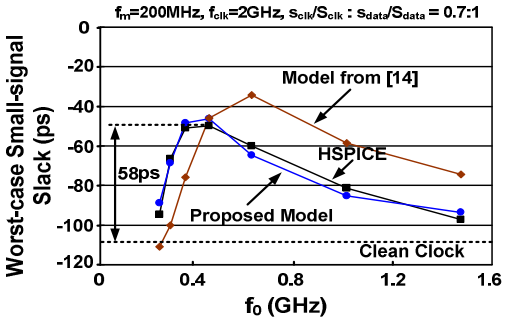
Furthermore, equation (13) also predicts that the maximum compensation happens when:

$$\sin\left(\frac{\pi f_m}{f_0}\right) = 1 \quad \text{or} \quad f_0 = 2 f_m \tag{14}$$

This result is consistent with what was shown in [14] and is verified by simulations in Fig. 5(b). The best clock path delay happens at 400MHz ($=2f_m$) and improves the worst-case slack by 58ps (12% of clock period) compared with the clean clock case.



(a)

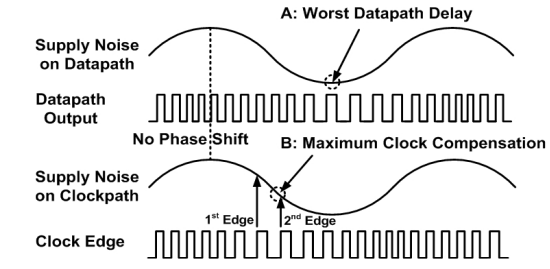


(b)

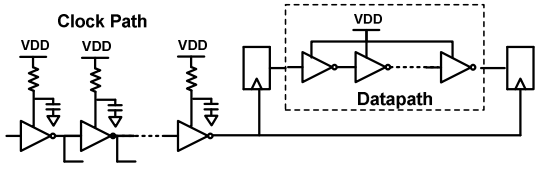
Fig. 5 (a) Worst-case slack variation vs. delay sensitivities. (b) Worst-case slack variation vs. clock path delay frequency f_0.

3. PHASE-SHIFTED CLOCK DISTRIBUTION NETWORK DESIGN

We have shown in the previous section that the delay change on the clock path can partially compensate for the delay increase in the datapath. However, in a normal clock tree, the compensation effect is not optimized, so the benefits may be small. Fig. 6(a) illustrates the compensation effect on a normal clock tree. The slope of the supply noise determines the amount of timing compensation because the clock period is stretched only when the second clock edge sees a lesser supply than the first one. Therefore, the best compensation happens at point B where noise slope is sharpest and the clock period is stretched to the largest extent. However, point B does not represent the worst-case delay point on the datapath which actually happens at point A. To maximize the compensation from the clock path, we propose to use a phase-shifted clock tree where the supply noise on the clock buffers is shifted by an optimal amount. Fig. 6(b) shows the schematic of the proposed phase-shifted clock tree. RC filters are used on the clock buffer supply to defer the supply noise in the clock tree by an amount determined by the filter components. As shown in Fig. 6(c), with a phase shift of φ, the longest clock period due to supply noise is shifted in the time axis to coincide with the largest data delay so that the worst-case slack is improved. Although this phase-shifted clock scheme is similar to what has been proposed in [13-14], the phase-shift effect was not dealt with in previous work. In fact, the impact of phase shift is more significant than the attenuation of supply noise amplitude by the RC filter which was considered as the primary reason for the timing compensation in [13-14]. Moreover, [13-14] used a single RC filter for the entire clock distribution which can lead to uncertain phase shift effects in each clock buffer as they are usually distributed across the entire chip. In this work, we propose a simple structure where each clock buffer contains its own RC filter, which makes the clock distribution design modular and reliable. Though the area of each clock buffer is 6X larger than the conventional one, its impact on total chip area is minimal due to the small chip area used for clock buffers.



(a)



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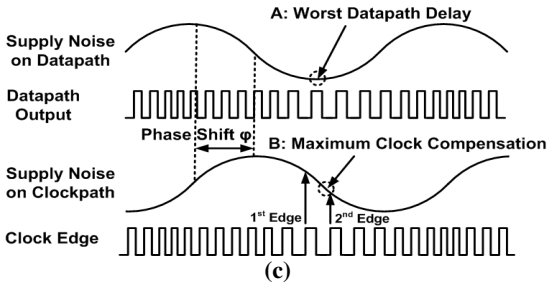


(c)

Fig. 6 (a) Clock/data compensation in a normal clock tree. (b) Schematics of proposed phase-shifted clock distribution. (c) Clock/data compensation in a phase-shifted clock distribution. A denotes the point with worst datapath delay; B denotes the point with maximum clock compensation.

The impact of phase-shifted clock tree can be modeled using the equations derived in Section 2. With an RC filter on the supply of clock path, equation (10) can be modified as:

$$slack(\theta) = \frac{s_{clk}}{S_{clk}} \frac{2a}{A_0} \frac{f_{clk}}{\pi f_m} \sin\left(\frac{\pi f_m}{f_{clk}}\right) \sin\left(\frac{\pi f_m}{f_0}\right) \times A_F \sin\left(\theta - \varphi - \frac{\pi f_m}{f_0} - \frac{\pi f_m}{f_{clk}}\right) + \frac{s_{data}}{S_{data}} \frac{a}{A_0} \cos\left(\theta - \frac{\pi f_m}{f_{clk}}\right) \quad (15)$$

where φ denotes the phase shift on clock path and A_F is the noise magnitude attenuation due to the RC filter. Fig. 7 shows the worst-case slack as a function of phase for our proposed model. It shows that equation (15) matches closely with HSPICE simulation results which indicates a maximum slack improvement of 75ps (15% of the clock period) using a phase shift of 0.2π. The slack improvement has increased by 2.5X compared with the improvement of 30ps (6% of clock period) with the zero phase shift case. This result confirms shifting the phase of clock supply voltage can enhance the delay compensation from the clock path.

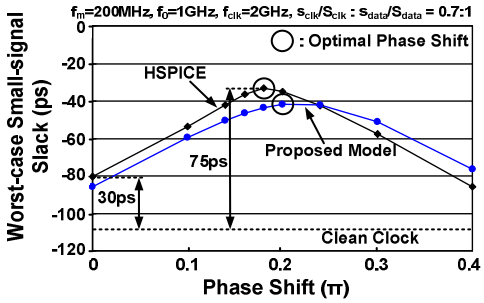


Fig. 7 Worst-case slack variation vs. shifted phase.

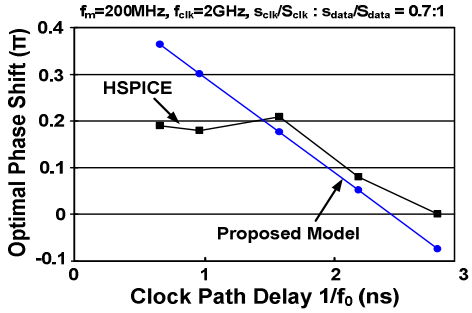


Fig. 8 Optimal phase shift comparison between the proposed model and HSPICE simulation results.

Similar to (12), the worst-case slack can be found as:

$$|slack_{wc}| = \sqrt{4A_F^2 \left(\frac{s_{clk}}{S_{clk}}\right)^2 \left(\frac{a}{A_0}\right)^2 \left(\frac{f_{clk}}{\pi f_m}\right)^2 \sin^2\left(\frac{\pi f_m}{f_{clk}}\right) \sin^2\left(\frac{\pi f_m}{f_0}\right) + \left(\frac{s_{data}}{S_{data}} \frac{a}{A_0}\right)^2 - 4A_F \frac{s_{clk}}{S_{clk}} \frac{s_{data}}{S_{data}} \left(\frac{a}{A_0}\right)^2 \frac{f_{clk}}{\pi f_m} \sin\left(\frac{\pi f_m}{f_{clk}}\right) \sin\left(\frac{\pi f_m}{f_0}\right) \sin\left(\frac{\pi f_m}{f_0} + \varphi\right)} \quad (16)$$

The minimum negative slack is thus achieved when the term $\sin\left(\frac{\pi f_m}{f_0} + \varphi\right)$ is equal to 1. Hence, the best slack improvement can be achieved when:

$$\frac{\pi f_m}{f_0} + \varphi = \frac{\pi}{2} \quad \text{or} \quad \varphi = \frac{\pi}{2} - \frac{\pi f_m}{f_0} \quad (17)$$

Equation (17) indicates that the optimal phase shift decreases with f_m and increases with f_0. Fig. 8 shows the comparison between results from (17) and the simulated optimal phase shift as we vary f_0. Except for some small discrepancies, the simulated optimal phase shift follows the trend predicted by (17). The discrepancies in Fig. 8 are due to the fact that the relationship between the filtered noise magnitude and the phase shift has been ignored. In fact, with a RC filter, A_F is related to φ as follows:

$$A_F = \cos(\varphi) \quad (18)$$

As a result, the more accurate optimal phase shift can be solved by finding the derivative of the non-linear equations from (16). However, the result from (17) still provides a good first-hand approximation for the optimal phase shift.

By deriving the transfer function of the RC filter, φ can be expressed using the RC value in the filter as:

$$\varphi = \tan^{-1}(2\pi f_m RC) \quad (19)$$

Once the optimal φ is determined from (17), R and C values can be selected accordingly to produce the desired phase shift. Since only the product of RC is important, the R can be selected as large as possible to save the area overhead on C which consumes much more area. However, a larger R causes a larger IR droop on the clock power supply and thus is limited by the constraint of clock propagation delay. In our test, we select an R value with a maximum IR droop of 50mV on the clock supply. The value of C is then determined accordingly. The resistor whose value does not have to be precise can be implemented using either a metal resistor or a MOS resistor. The capacitor can be implemented using a MOS capacitor or a Metal-Insulator-Metal (MIM) capacitor. The latter requires more area but consumes less leakage power. Fig. 9 shows the layout of the clock buffers used in our clock tree design. Resistance and capacitance values are chosen to obtain the best timing compensation while keeping the IR drop less than 50mV. Simulated waveforms of the phase-shifted supply are given in Fig. 10 which shows a 0.2π phase shift and 50mV IR drop.

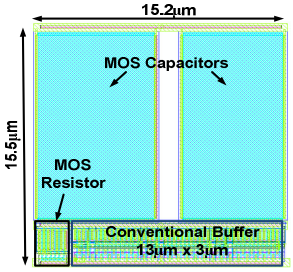


Fig. 9 Layout of phase-shifted clock buffer in 65nm with a built-in RC filter. Although the proposed clock buffer is 6X larger than its conventional counterpart, the impact on total chip area is minimal as clock buffers do not consume large chip area to start with. Moreover, the proposed scheme leads to an 80%+ saving in decap area.

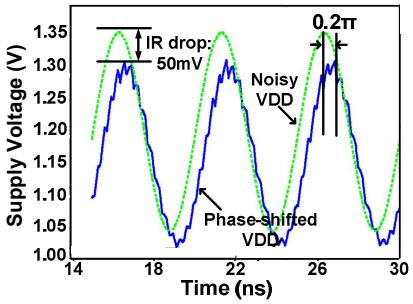
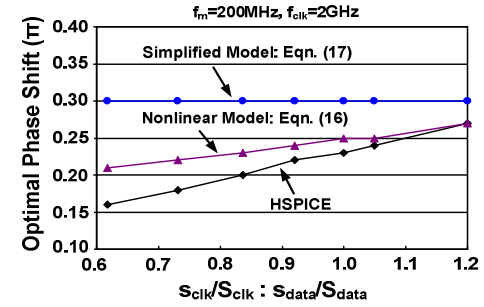


Fig. 10 Simulated waveforms of phase-shifted supply.

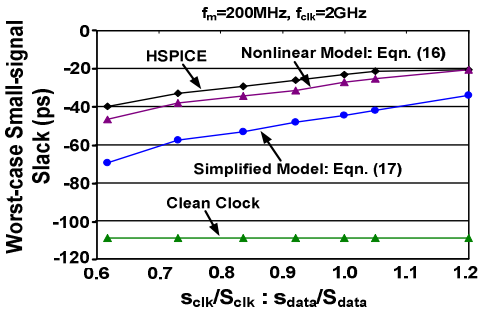
The clock path and datapath delay sensitivities also have an impact on the optimal phase shift and slack improvement. Fig. 11(a) shows the simulated optimal phase shift under different clock path sensitivity to datapath sensitivity ratios. The sensitivities were

varied in our simulation by changing the interconnect load. Both the simplified model in equation (17) and the nonlinear model in equation (16) were used to calculate the optimal phase shift. Compared with simulation result, the nonlinear model from equation (16) provides a more accurate result. As the clock path sensitivity increases, the optimal phase shift value also increases linearly. Fig. 11(b) gives corresponding slack improvement at each optimal phase shift. These results show that a larger clock path sensitivity lead to better slack compensation under the optimal phase shift, which is different from the trend shown in Fig. 5(a) because the compensation with the phase-shifted clock distribution has been maximized.

As mentioned earlier, the design overhead of the proposed phase-shifted clock distribution comes from the use of RC filters in the clock path buffers. Because of the improvement in slack, this technique leads to a significant saving in the amount of decap which makes the area overhead of the proposed scheme negligible. Table 1 summarizes the effectiveness of the proposed technique. For equal performance, an 80% saving of decap area can be achieved using the proposed phase-shifted clock distribution.



(a)



(b)

Fig. 11 (a) Optimal phase shift for different clock path and datapath sensitivities. (b) Corresponding worst-case slack.

Table 1. Summary of the proposed technique

Resonant Noise	200MHz
Clock Frequency	2GHz
Intrinsic Decap C*	6nF
Package Inductance L*	0.1nH
Load Current*	1A
R in RC Filter	300 Ω
C in RC Filter	2pF
Phase Shift	0.2π
Slack Improvement from Phase Shift	75ps (15% T_{clk})
Equivalent Decap	24nF
Decap Saving from Proposed Technique	80%

*The L, C and load current values are scaled down proportionally to account for the smaller clock tree used in our test set up.

4. CONCLUSIONS

Power supply noise introduces delay variation on datapaths and jitter on clock paths. Although clock jitter has been conventionally treated as detrimental, it has been recently shown that jitter can be beneficial for timing as it can provide partial compensation for the increase in datapath delay. This work investigated the "beneficial jitter" effect in a pipeline circuit. An analytical model was derived which improves the prediction accuracy for the clock-delay compensation effect compared with previous publications. A phase-shifted clock distribution technique is proposed to enhance the beneficial jitter effect. The optimal phase shift was found using our model to guide the circuit design of the proposed clock distribution network. The timing compensation effect of our phase-shifted clock distribution was verified with HSPICE simulations using an industry level 1.2V, 65nm process. The impact of noise sensitivities and clock path delay on slack improvement was also evaluated. Results show that the proposed scheme enhances the beneficial jitter effect improving the timing slack from 6% of clock period to 15% of clock period. This improvement translates into an 80% saving of decap area.

5. ACKNOWLEDGEMENT

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