A Multi-story Power Delivery Technique for 3D Integrated Circuits

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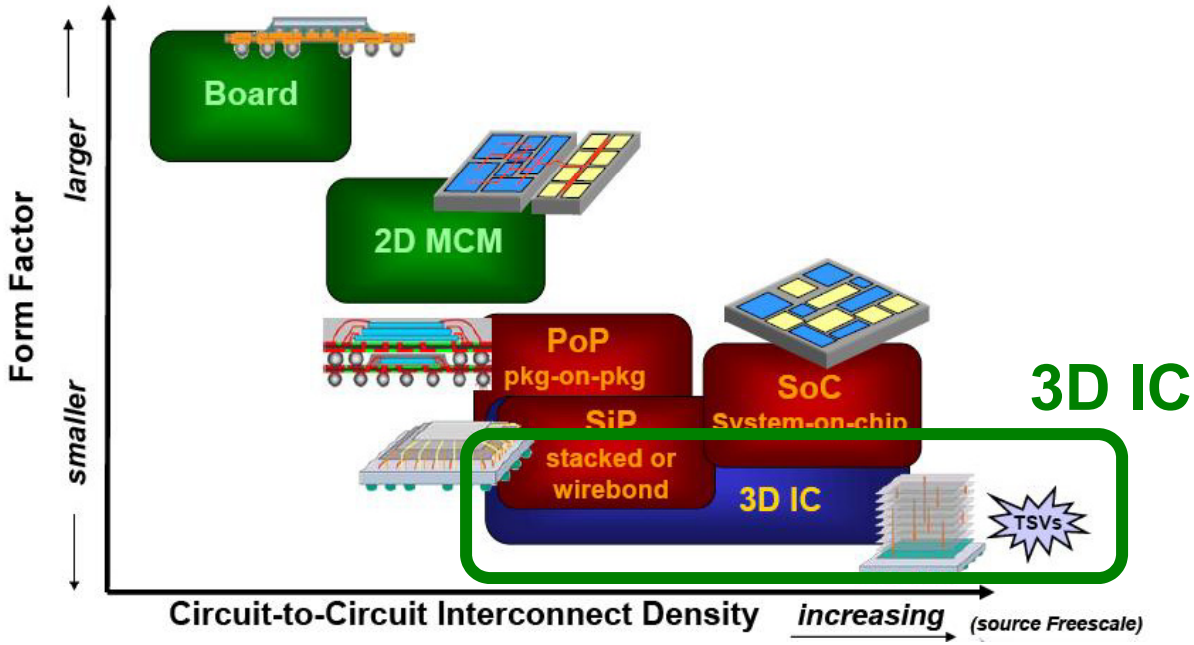
Presentation Agenda

- 3D IC: Motivation and roadblocks
- 3D IC: Power Supply Network (PSN) model
- Power supply integrity: 2D vs. 3D
- Multi-Story Power Delivery (MSPD) for 3D
- 3D SRAM test layout
- Conclusion

3D Integration Technology



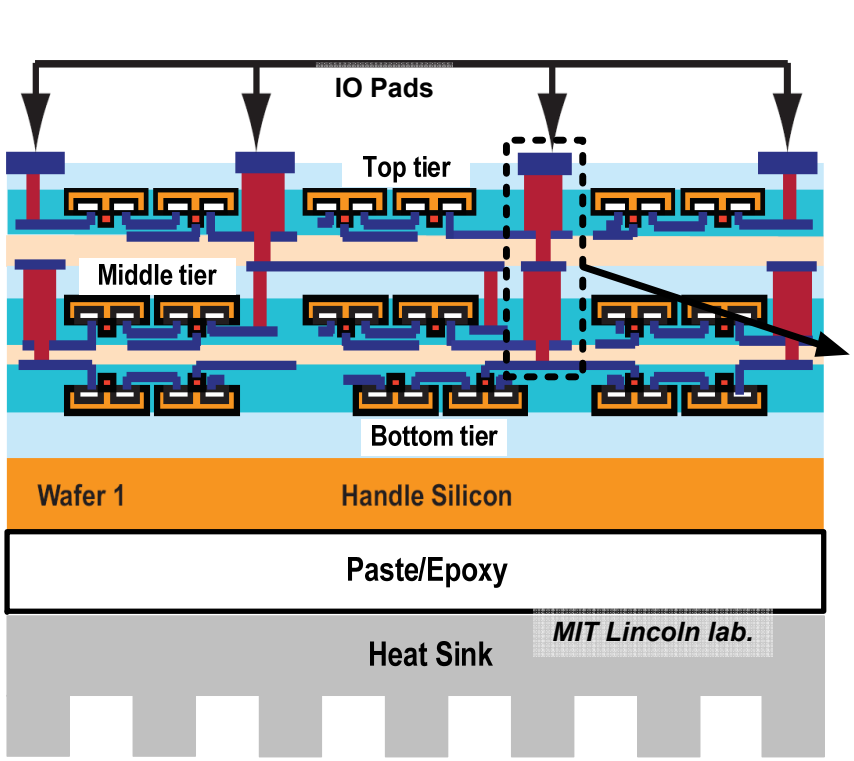
Motivation

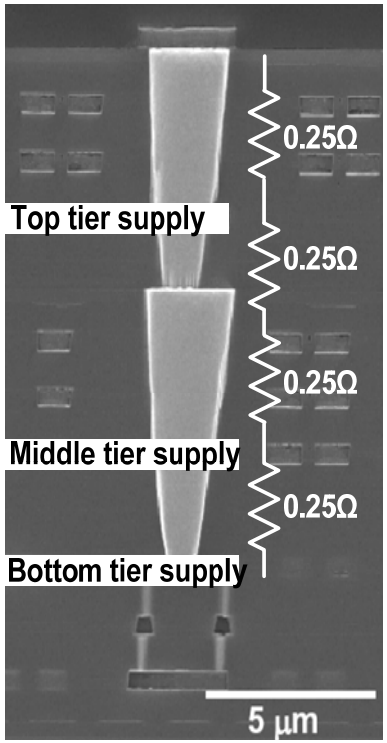
- Reduced interconnect lengths, form factor
- Integrating varied technologies

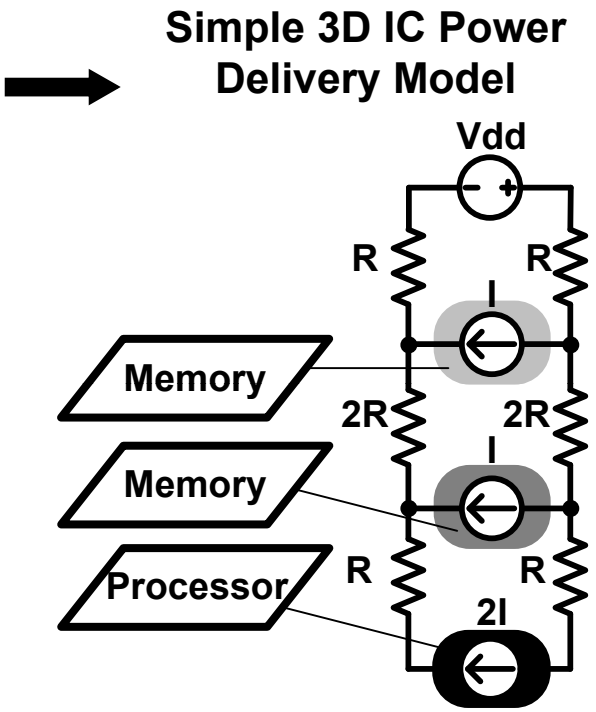
Challenges

- Alignment issues, thermal congestion
- Power delivery issues

Power Delivery Model for 3D IC







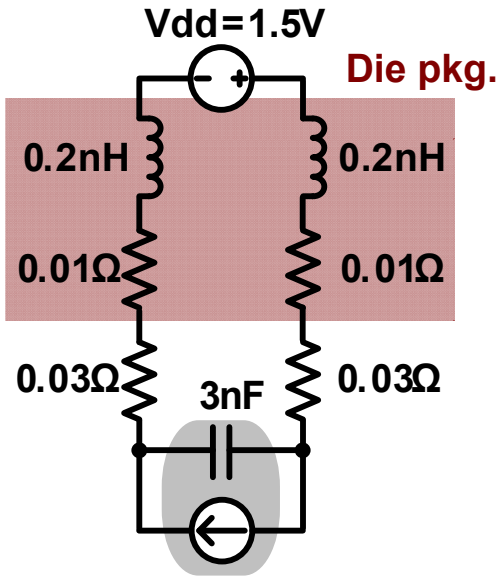
- 0.18µm 3-tier fully-depleted SOI process
- Stacked Through-Si Via (TSV): R~1Ω

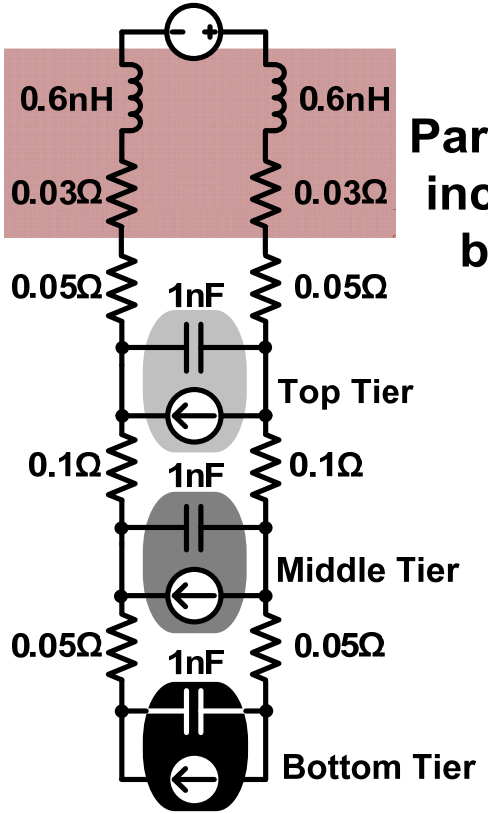
Issue: Power supply noise at the bottom tier

Simplified 2D and 3D PSN Models

2D power delivery

- Lump model with core ckt & package and grid parasitics
- Simplified model with 10 I/O pads





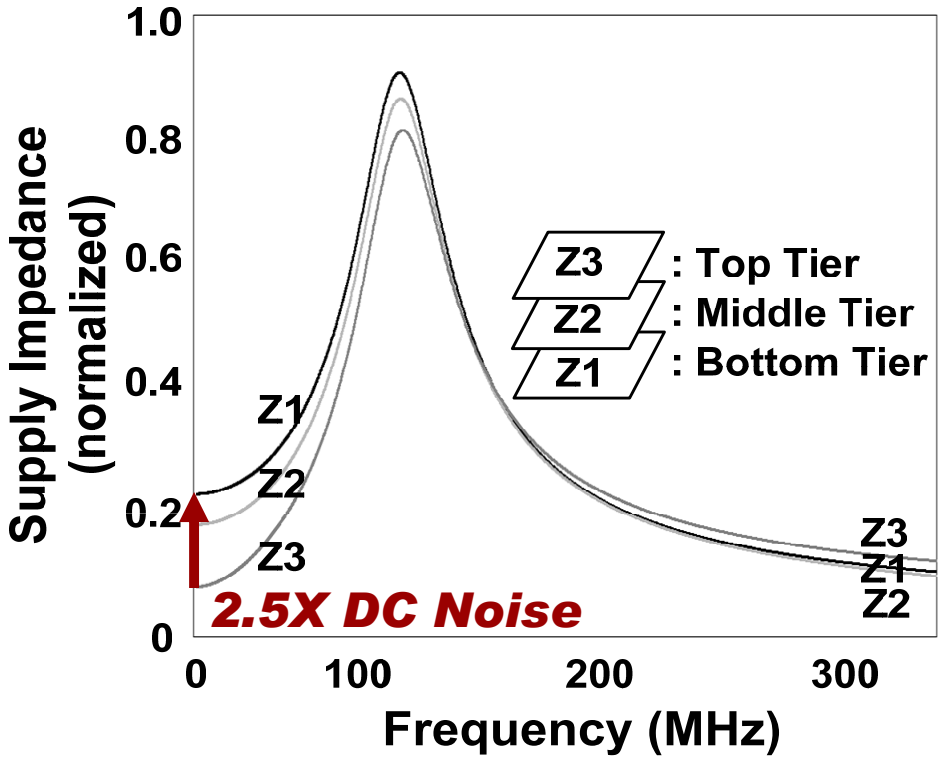
Parasitics increase by 3X

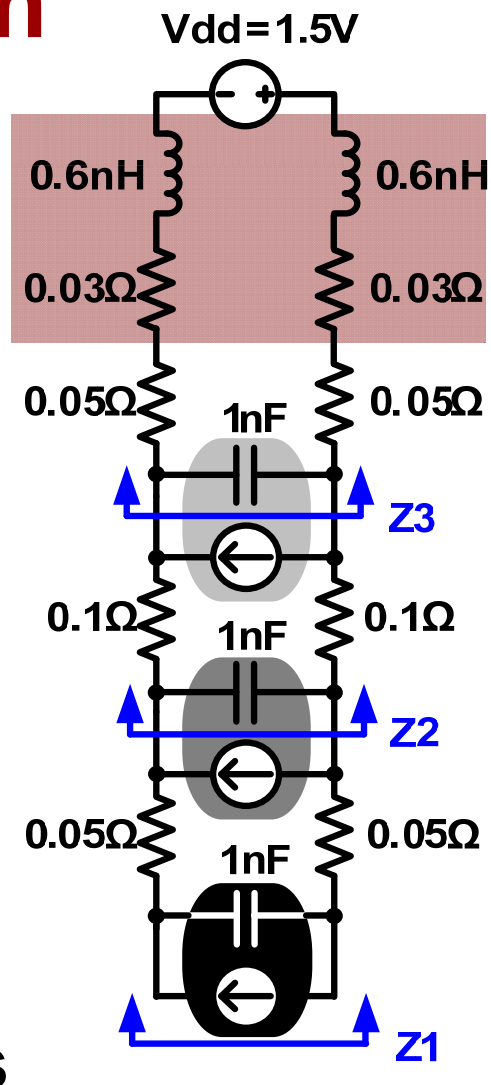
3D power delivery

- Reduced footprint→3X parasitics
- Distributed decap
- Additional TSVs in supply path

Power Supply Noise in 3D IC

Tier-tier comparison

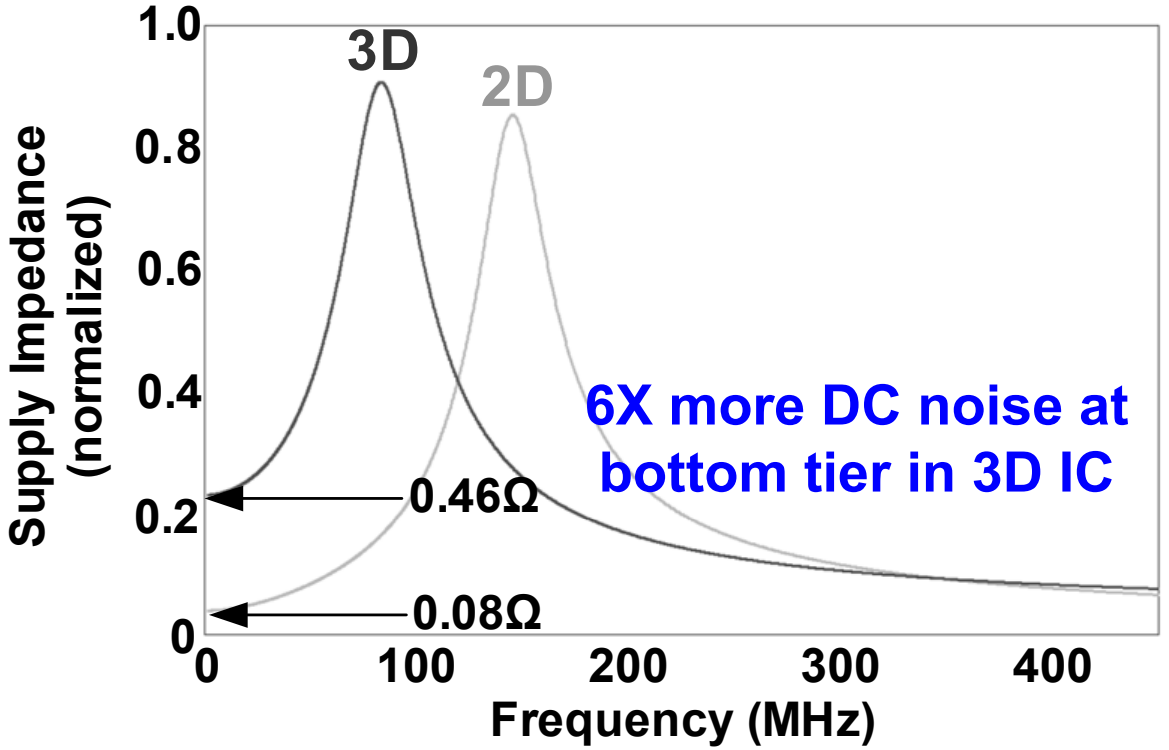




- Low freq. noise: Z1 > Z2 > Z3
- High freq. noise: Z3 > Z1 > Z2
- Similar resonant freq. between tiers

Power Supply Noise in 3D IC

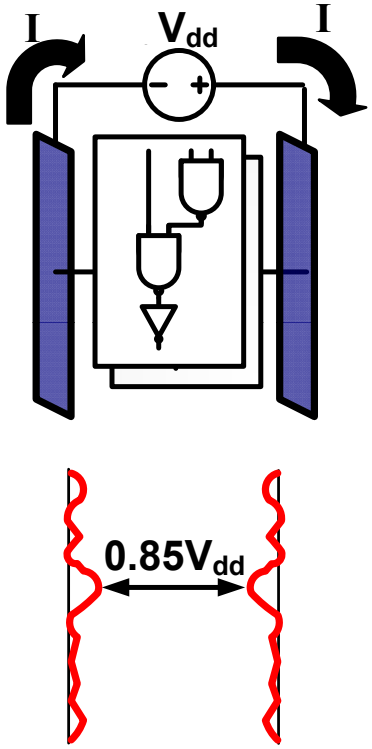
2D vs. 3D



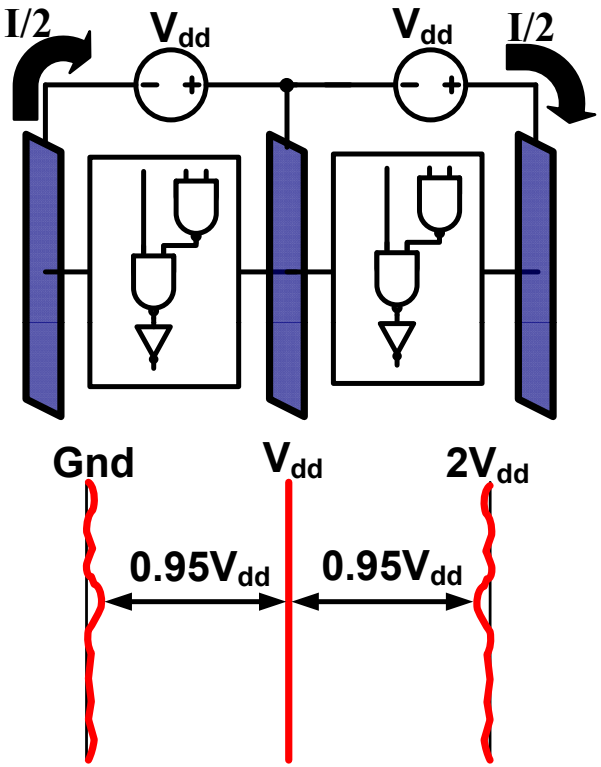
- DC noise greater issue in 3D IC
- Increased L decreases the resonant freq. in 3D.
- Resonant peak almost unchanged

Multi-Story Power Delivery (MSPD)

Single-story



Multi-story



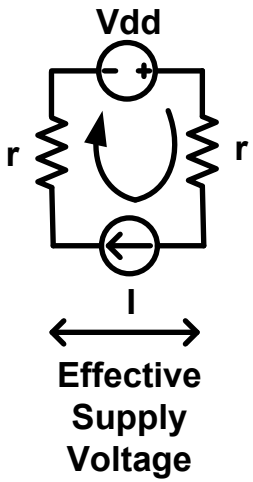
Rajapandian et al.
ISSCC 2005

Gu et al.
ISLPED 2005

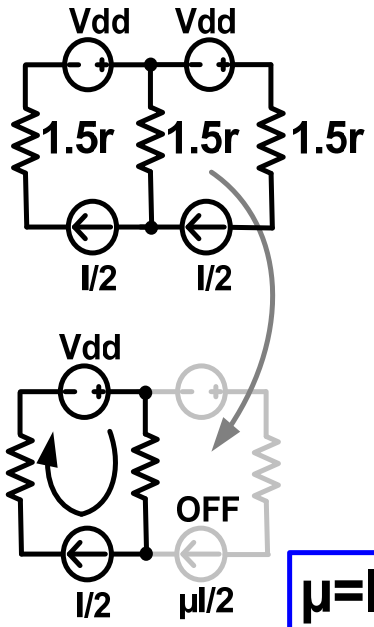
- **Current consumption halved, which cuts DC noise**
- **The middle supply is *quiet* due to current balance**
- **3D ICs offer readily separable PSNs**

DC Supply Noise in MSPD

Single-story

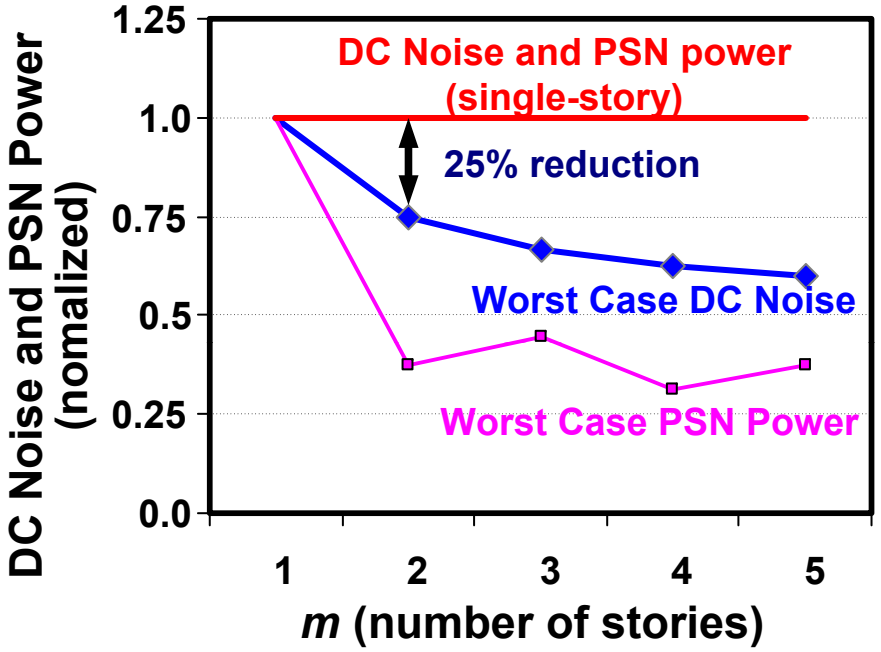


Two-story



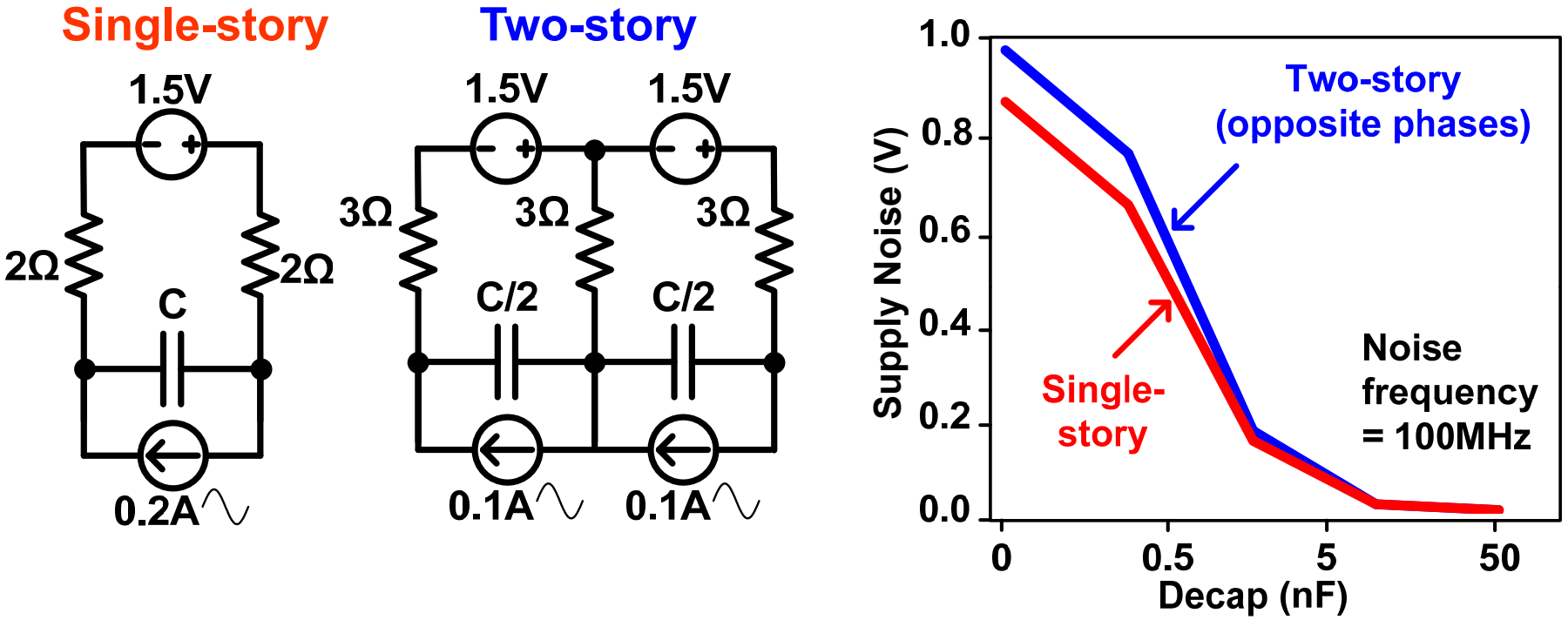
$\mu = I_{leak}/I_{on}$

***m*-story Case (μ=0)**



- **Worst case scenarios compared while keeping the number of supply paths constant.**
- **Beneficial effect of leakage**
- **25% noise reduction for 2-story case with no leakage (μ=0)**
- **Diminishing returns beyond 2 stories**

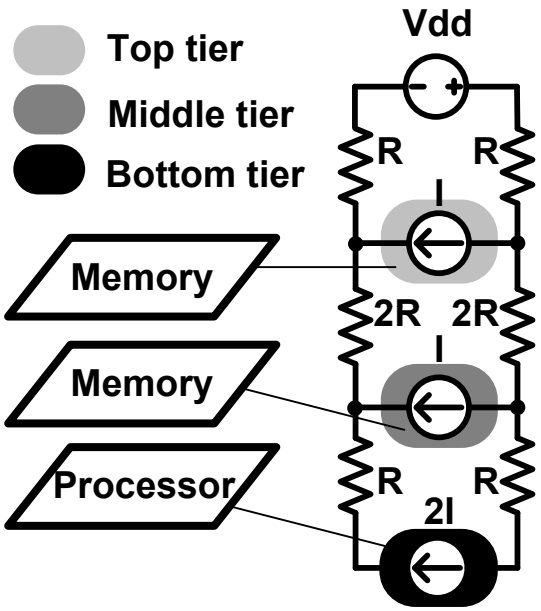
AC Supply Noise in MSPD



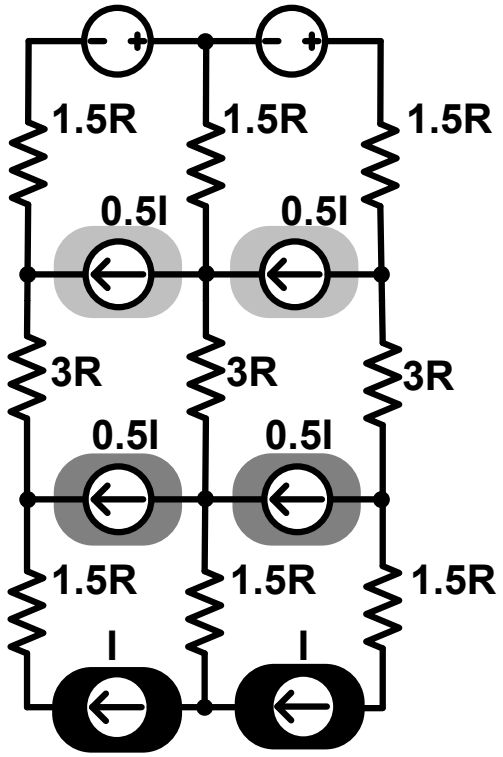
- Total decap and noise source made identical
- Noise in two-story worse for small decaps
- Comparable noise at decap more than 1nF

MSPD in 3D ICs

Single-story 3D IC



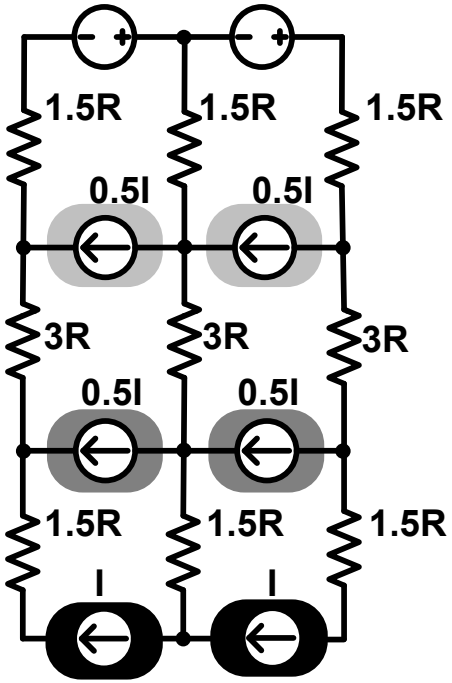
Proposed Balanced Two-story 3D IC



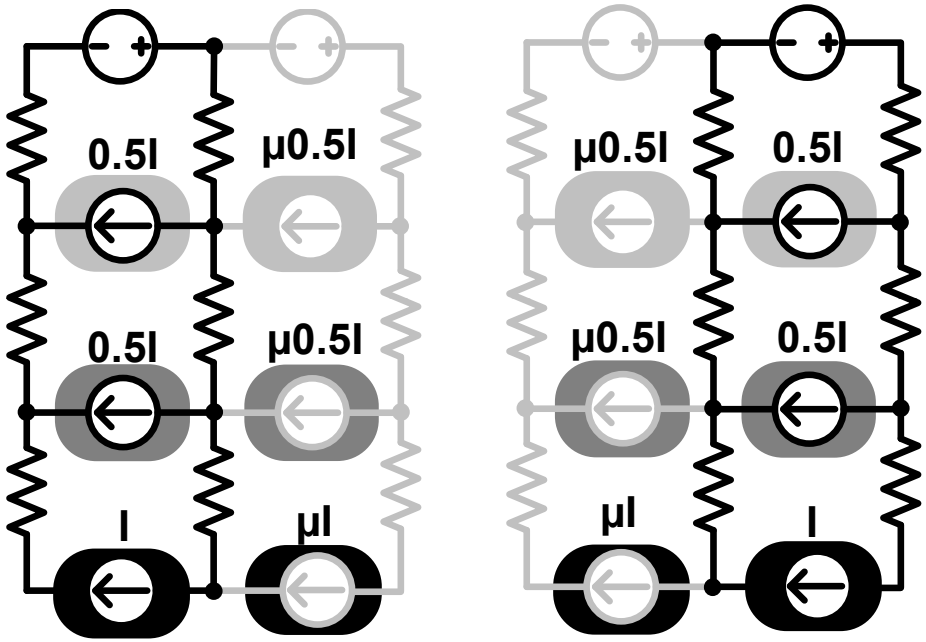
- Simple memory-memory-processor model
- Fine grain MSPD in each tier

MSPD in 3D ICs

Balanced Two-story 3D IC



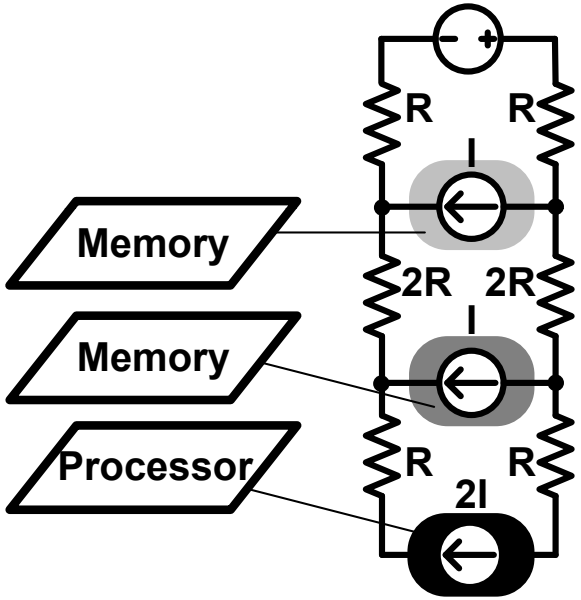
Worst Case Conditions



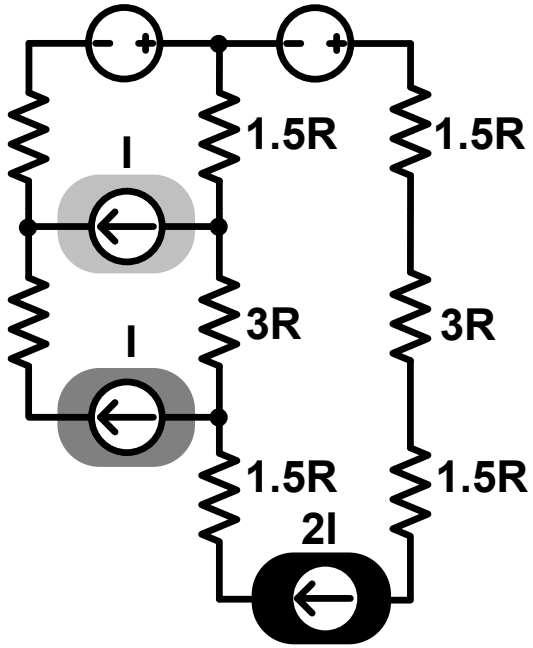
- **44% reduced worst case noise at 50% leakage**
- **PSN power reduction of 60%**
- **Implementation issues: Body effect in bulk process, level conversion**

Coarse MSPD in 3DIC

Single-story 3D IC



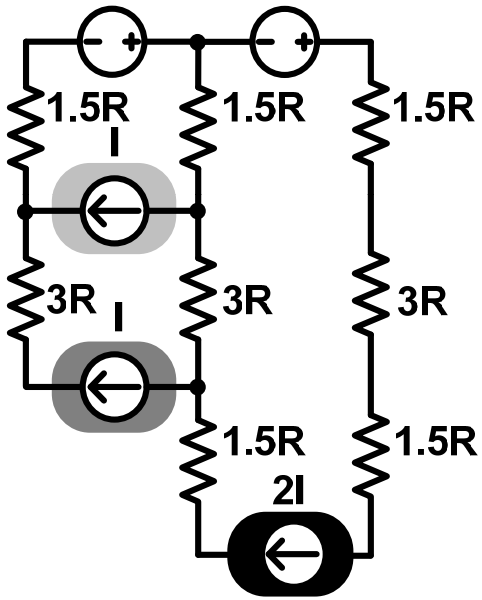
Proposed Coarse Two-story 3D IC



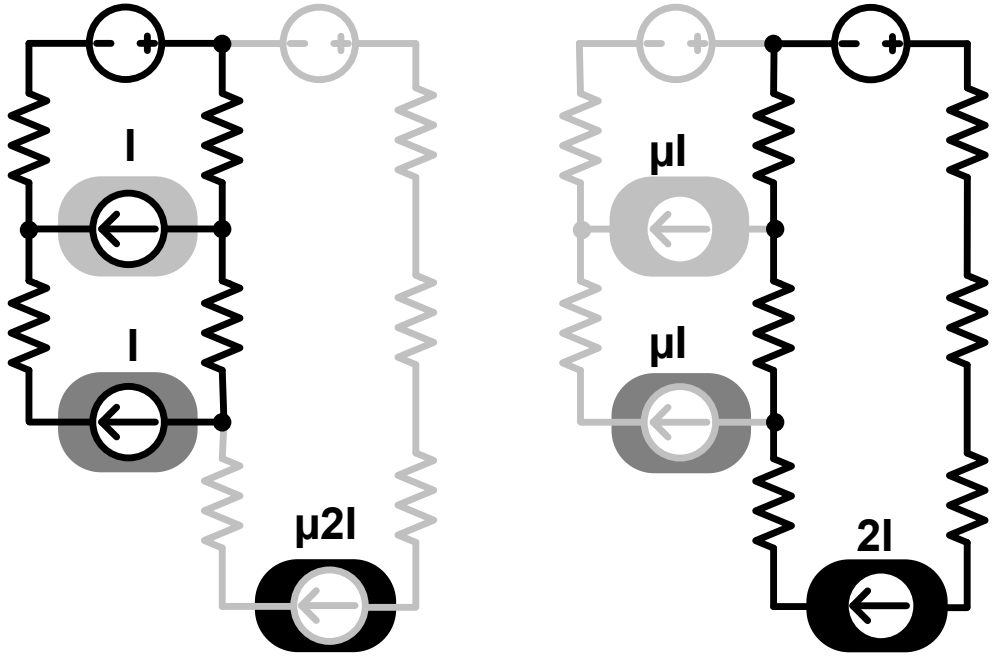
- 3D configuration offers discrete separable stories
- Body effect not an issue

Coarse MSPD in 3DIC

Proposed Coarse Two-story 3D IC



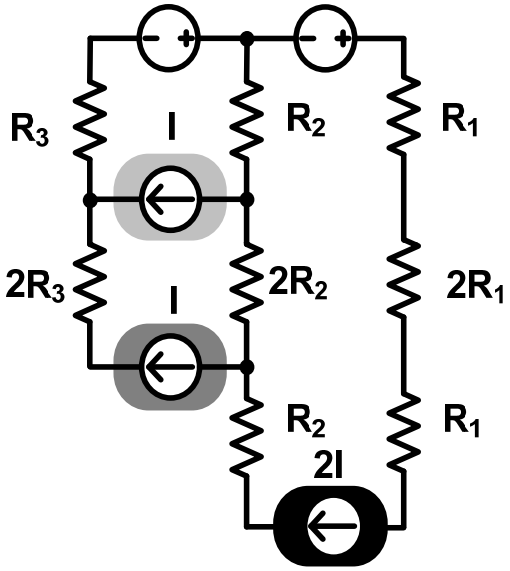
Worst Case Conditions



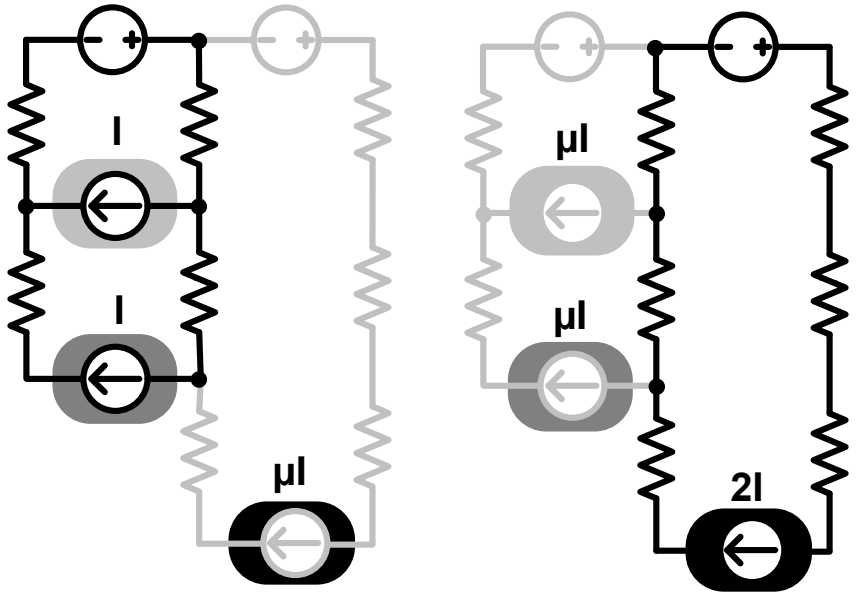
- **TSV redistribution required to leverage MSPD for DC noise reduction**
- **PSN power reduction of 60%**

TSV Optimization in Coarse MSPD

Proposed Coarse Two-story 3D IC



Worst Case Conditions

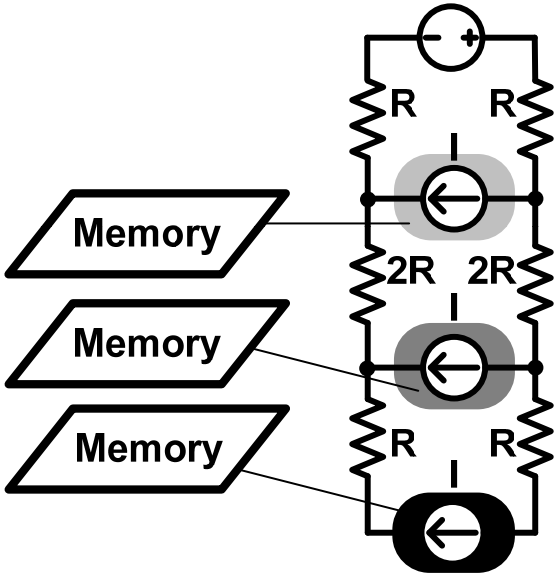


% leakage	*TSV Distribution (N_1, N_2, N_3)*	*DC_{noise} reduction*	*R_1,R_2,R_3 values*
0%	0.86N, 0.86N, 0.28N	22.5%	1.16R, 1.16R, 3.5R
25%	0.95N, 0.79N, 0.27N	28%	R, 1.27R, 3.7R
50%	N, 0.75N, 0.25N	34%	R, 1.33R, 4R

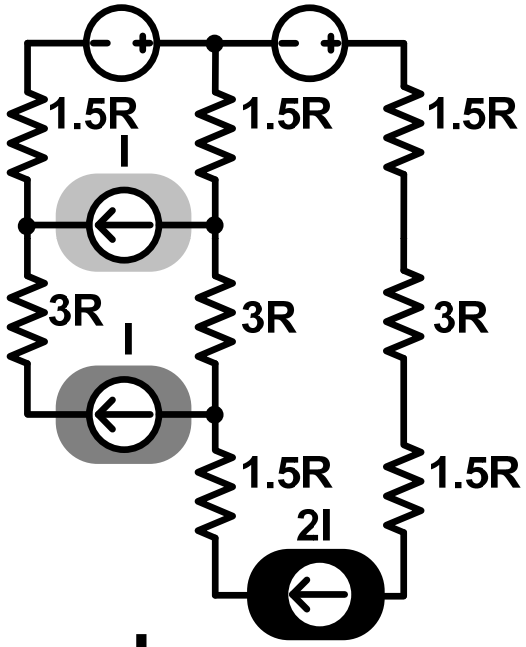
- **DC noise reduction up to 35%**
- **Similar optimization for PSN power reduction**

Coarse MSPD in 3D Memory

Single-story 3D memory

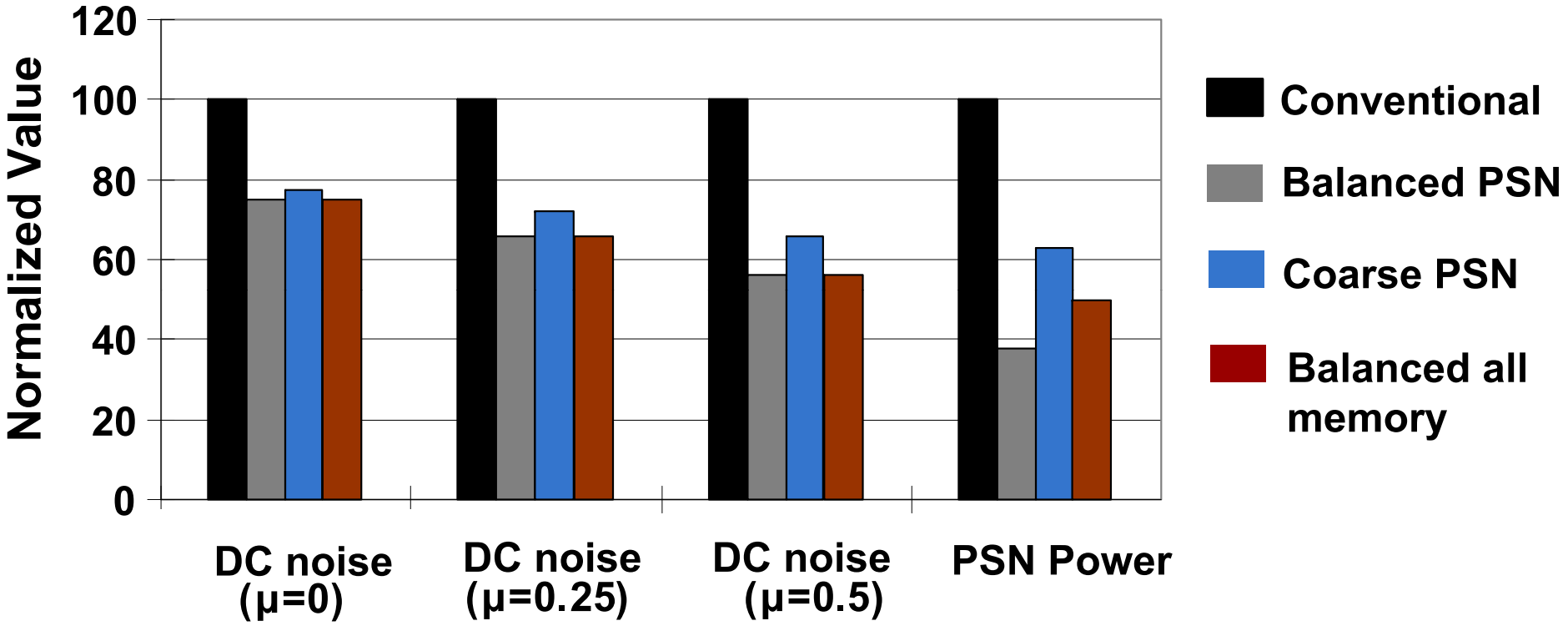


Proposed Coarse Two-story 3D Memory



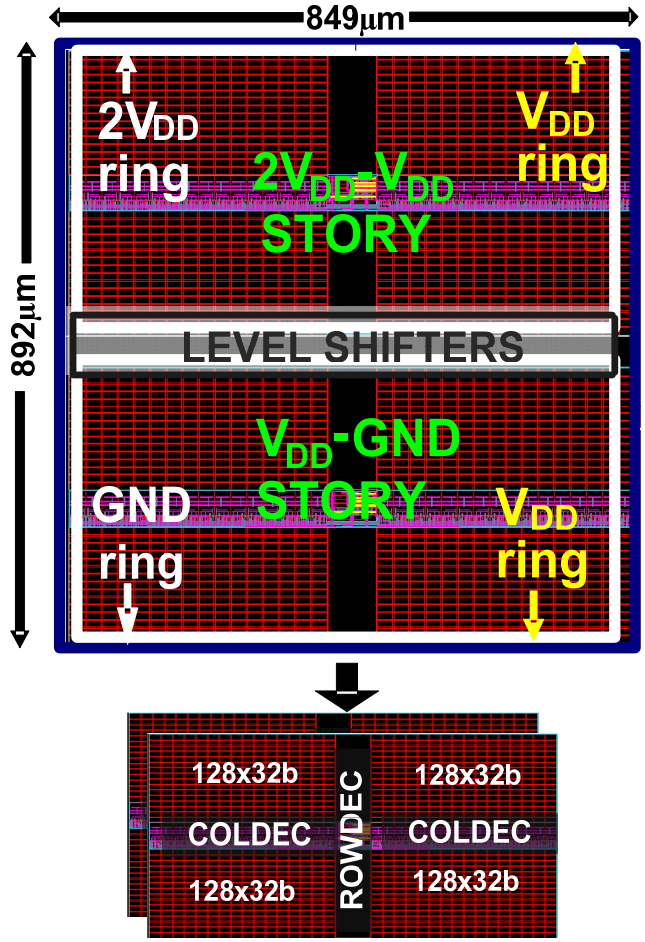
- Worst cases inherently balanced
- DC noise reduction up to 40%
- Simpler implementation
- PSN power reduction of 50%

Noise and Power Comparison



- Power supply noise reduction of 25-45% depending on preferred topology & leakage
- PSN power dissipation cut down by 37-63%

3D SRAM Layout with MSPD



Technology	0.18µm MITLL 3D FD-SOI
Features	128b x 128b x 2 SRAM on each of two upper tiers. Bottom tier left intact for logic integration.
Dimensions	892µm x 849µm
Area overhead	7.4%
Supply voltage	1.5V
Write speed	3.29ns
Read access cycle	1.10ns
Active power	6.8mW
Standby current	8uW

- **Balanced MSPD structure with level shifters**
- **Concentric ring structure for power supply**

Conclusion

- **Power delivery issues for 3D ICs analyzed**
  - DC noise is more of a concern in 3D IC
  - Middle tiers shielded away from high freq. noise
- **Inherent split configuration makes MSPD attractive and promising for 3D ICs**
  - 25-45% DC noise reduction
  - 37-63% PSN power reduction
  - Comparable behavior under high freq. noise
- **Test layout of 3D SRAM using MSPD shows an area overhead of 7.4%**