An Array-Based Test Circuit for Fully Automated Gate Dielectric Breakdown Characterization

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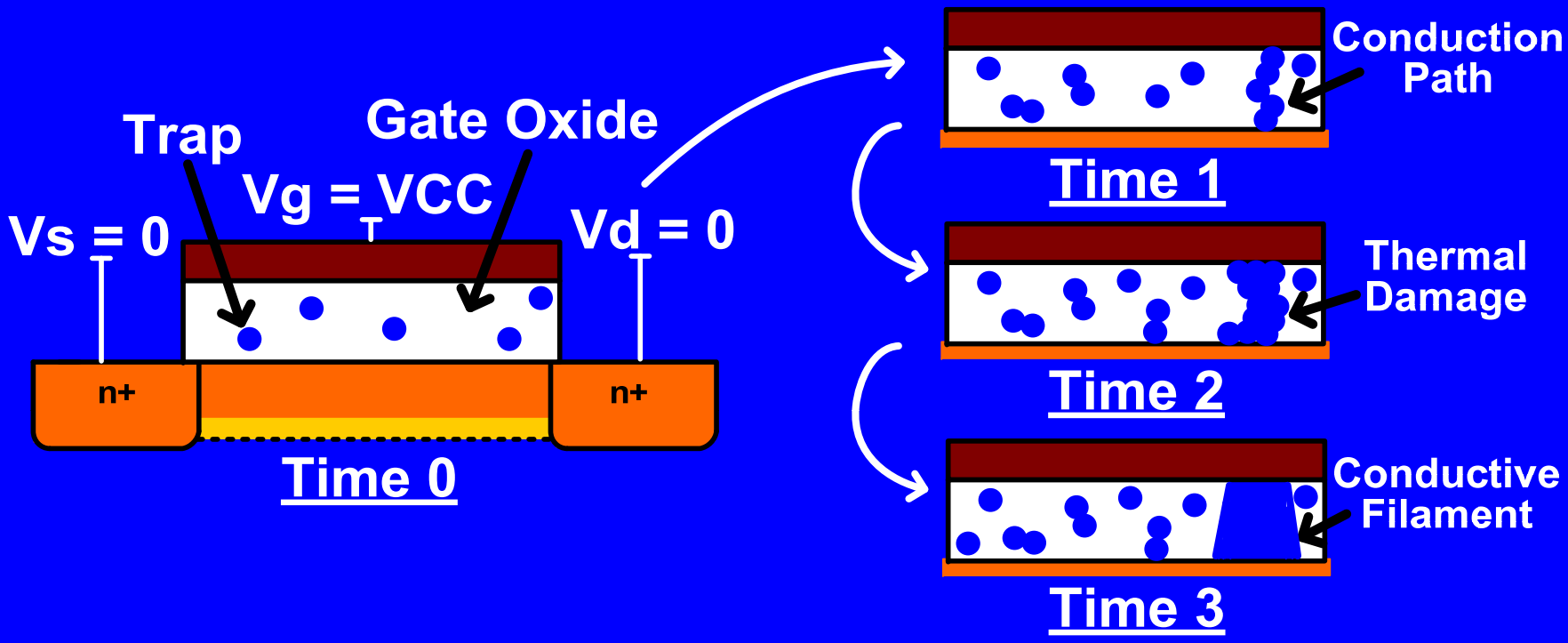
Outline of Presentation

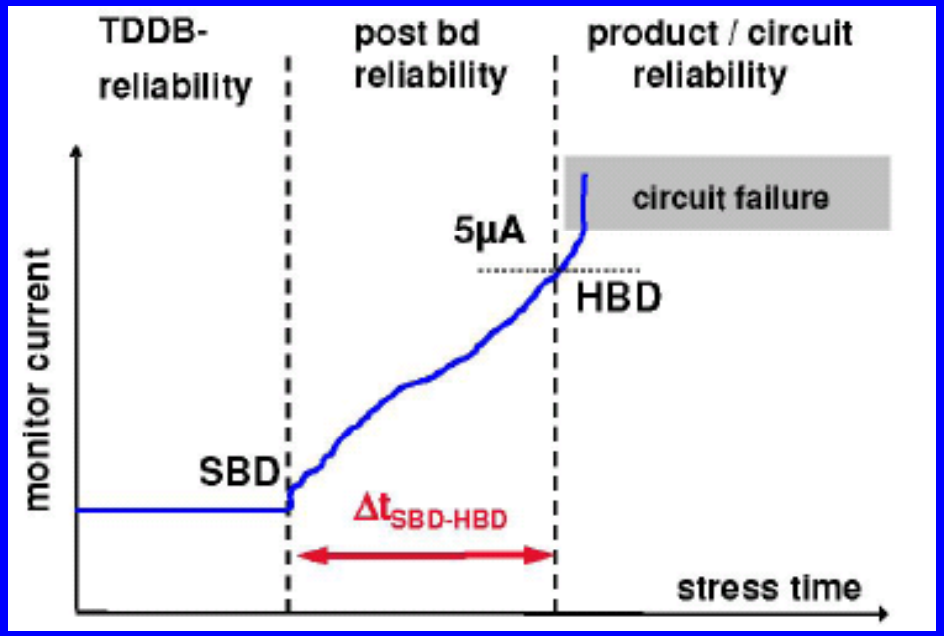
- Introduction to Time Dependent Dielectric Breakdown (TDDB)
- Proposed TDDB Test Array Circuit
- Test Chip Calibration
- Breakdown Measurement Results
- Conclusions

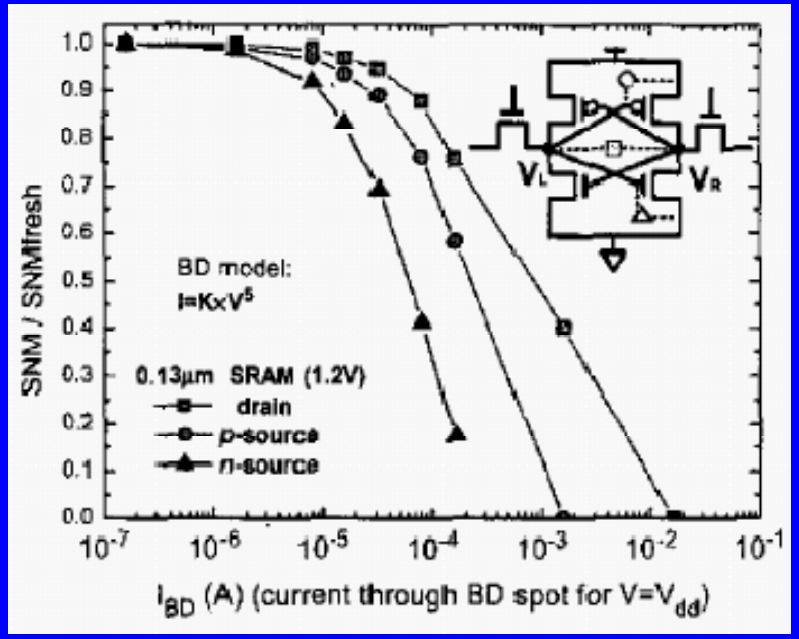
Introduction to TDDB



- Traps generated under the influence of electric field
- Traps overlap
  - Conductive path between gate and substrate
- Gate dielectric no longer a reliable insulator
  - Parametric or functional failure

Progressive Dielectric Breakdown

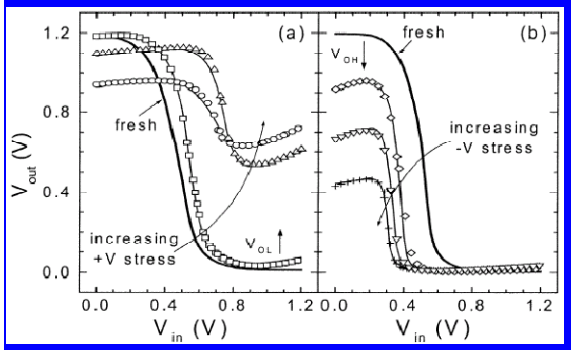


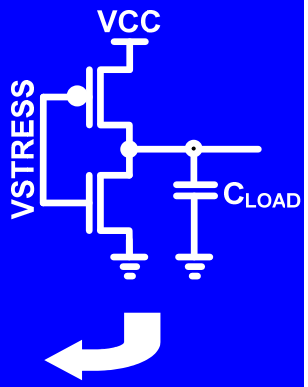


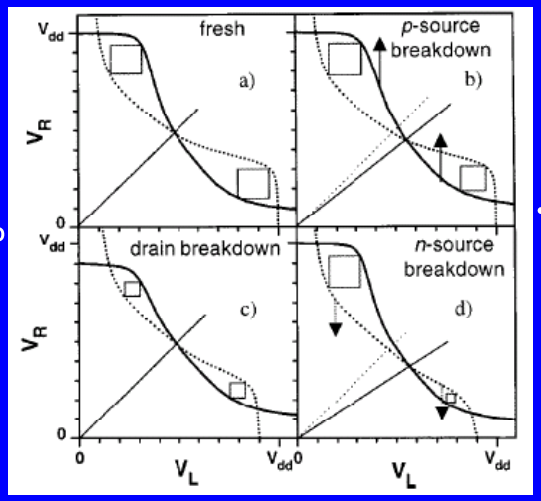
- Ultra-thin dielectrics can experience soft breakdown without failing
- Focus shifts to monitoring current *after* 1st breakdown
- Designers & reliability engineers must settle on reliability metrics for circuits with different sensitivities

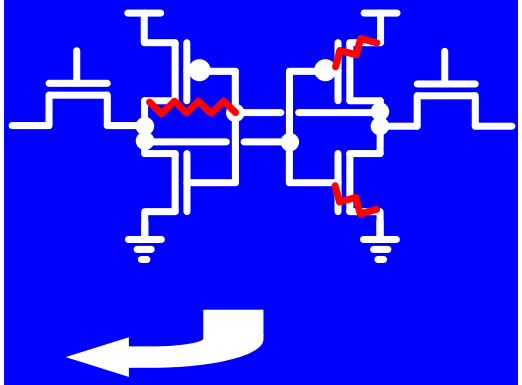
A. Kerber, et al., IRPS, 2007
J. Stathis, CICT, 2005

TDDB Impact on Digital Circuits









- Decreased performance & reliability, increased leakage, or outright failure
- Reduced O/P swing in digital logic can be restored in subsequent stages, but speed suffers
- SRAM SNM is degraded as a function of BD location

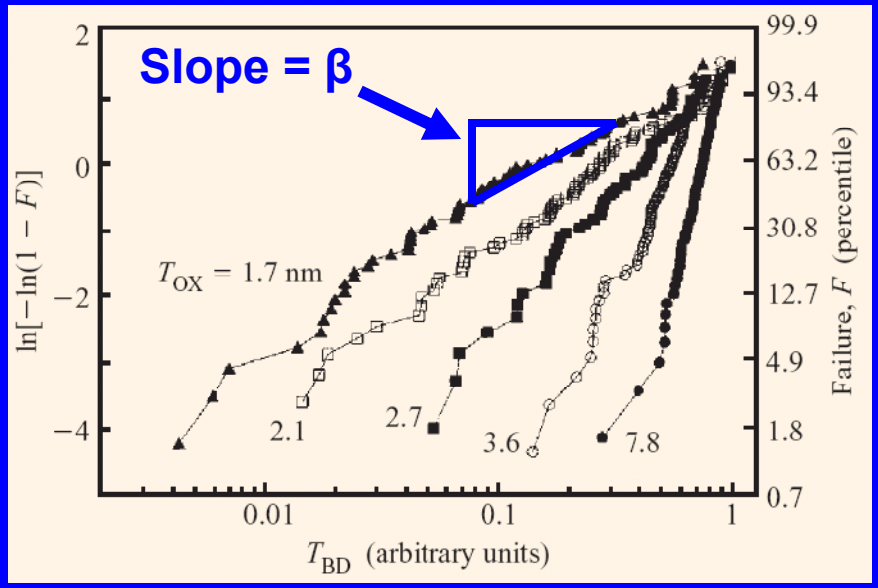
R. Rodriguez, et al., IEDL, 2003
R. Rodriguez, et al., IEDL, 2002

Statistical Characterization of TDB

Weibull Distribution

$$F(T_{BD}) = 1 - \exp\left[-\left(\frac{T_{BD}}{\alpha}\right)^{\beta} \right]$$

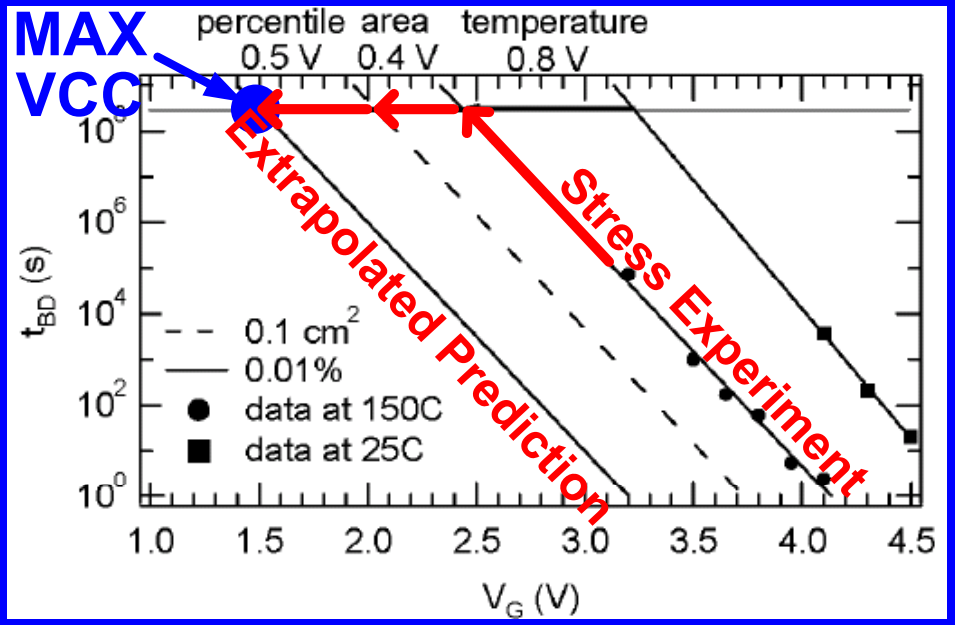
T_{BD} : Time-to-Breakdown
α : characteristic time (T_{BD} at 63%)
β : Weibull slope



- Breakdown related to generation of traps
  - Deterministic : trap generation rate
  - Statistical : critical trap density required for breakdown
- Failure statistics follow Weibull Distribution
- *1000s* of sampled needed to characterize distribution

E. Wu, et al., IBM J. of R & D, 2002

TDDB Lifetime Prediction



- Classical Reliability Approach
  - Extrapolate stress results with respect to:
    - Operating Conditions based on acceleration models
    - Larger Chip Areas based on Poisson area scaling
    - Lower Percentiles based on Weibull distribution
- Today consider unique environmental variables
  - 1st failure may not lead to chip failure, etc...

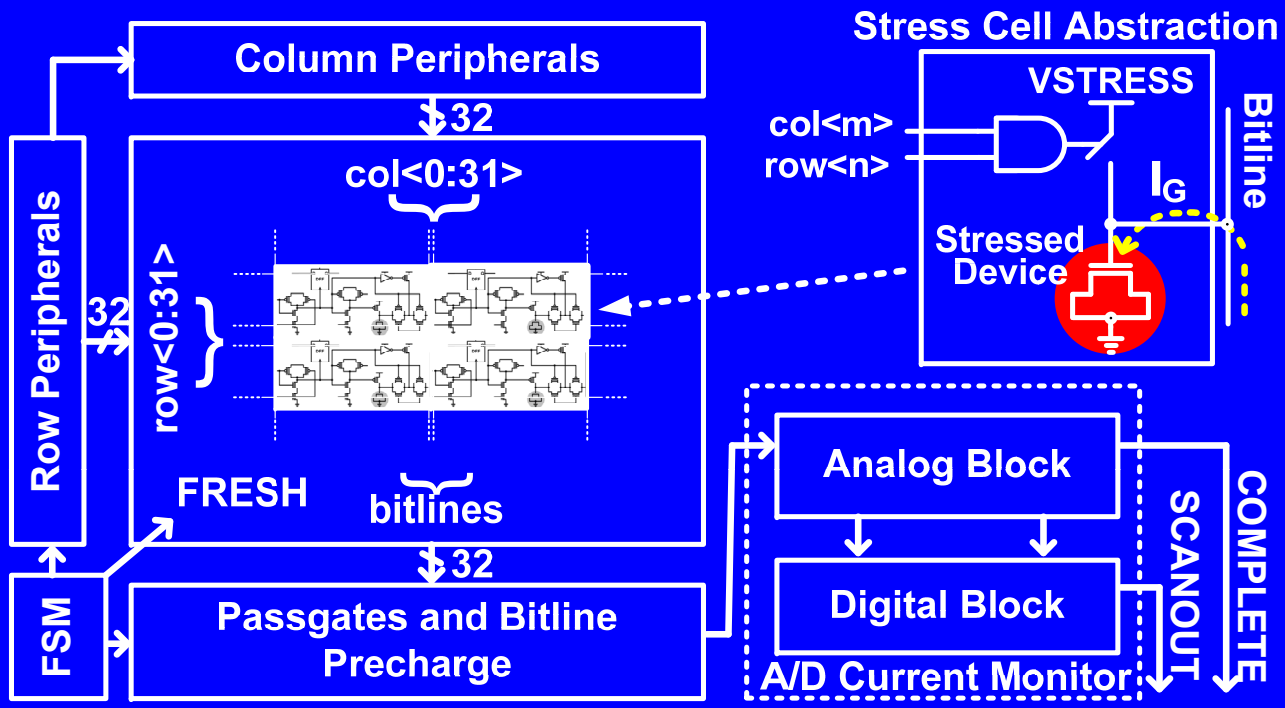
G. Groeseneken, et al., IPFA 2007

Prior TDDB Measurement Methods

- Individual device probing with expensive wafer probes; continuously monitor I_{GATE} or V_{GATE} of a single Device Under Test (DUT) per stress experiment.

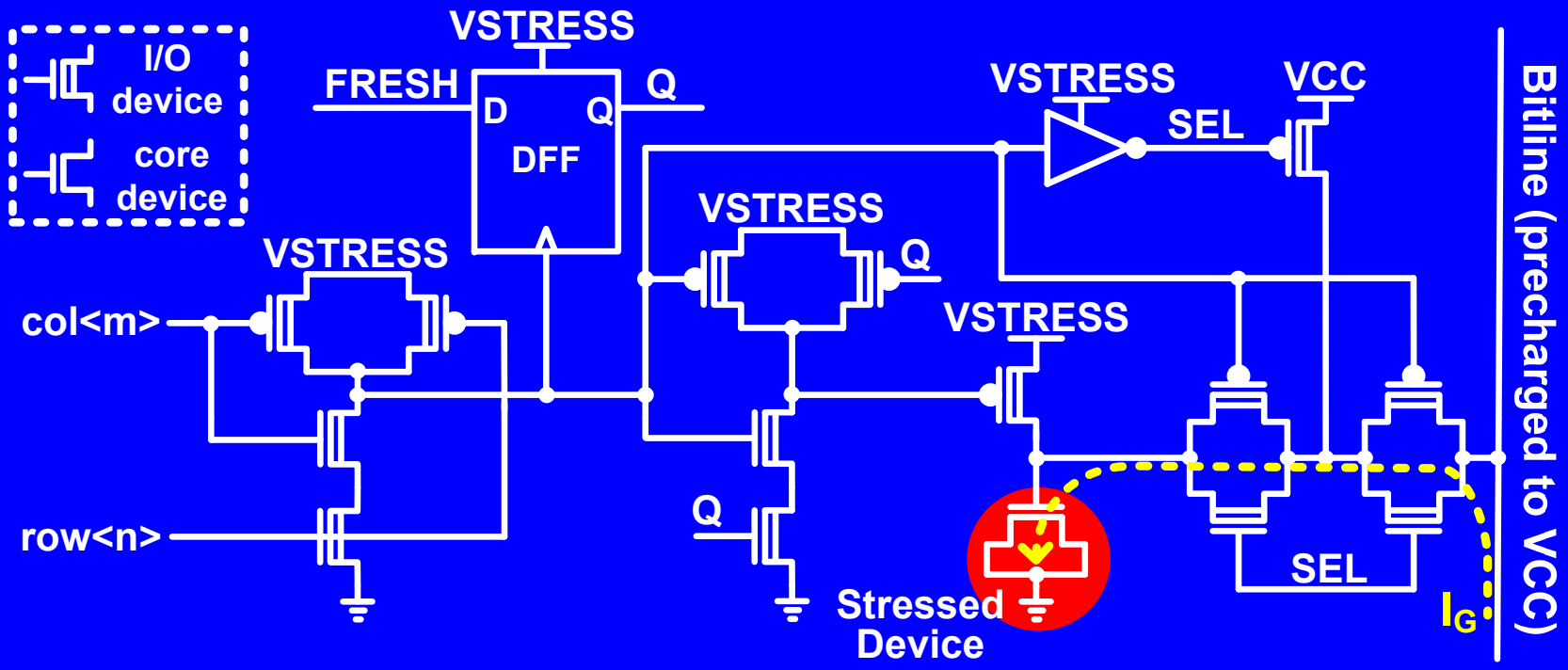
- Karl proposed a method to monitor the increase in gate leakage of a pair of DUTs whose gate voltage controls the frequency of a Schmitt Trigger Oscillator (ISSCC, 2008)

Proposed TDDB Measurement System



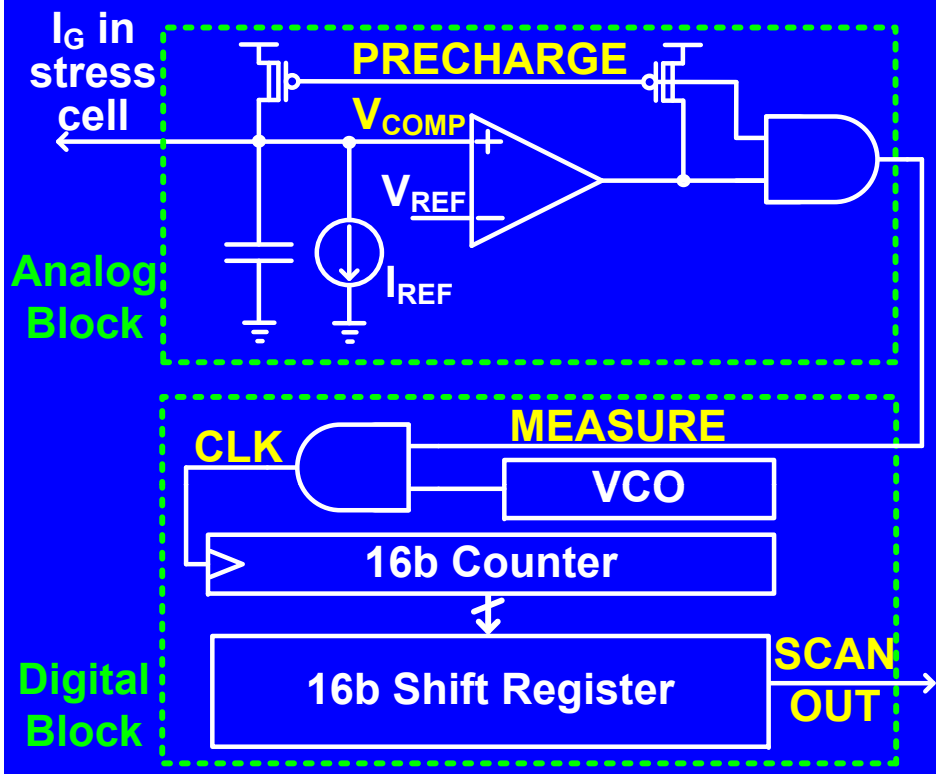
- 32x32 array of stressed NMOS transistors
- Gate currents (I_G) measured with A/D current monitor and on-chip control logic
- 16b results scanned out and stored for post-processing
- Efficient collection of failure statistics by running a simple control program

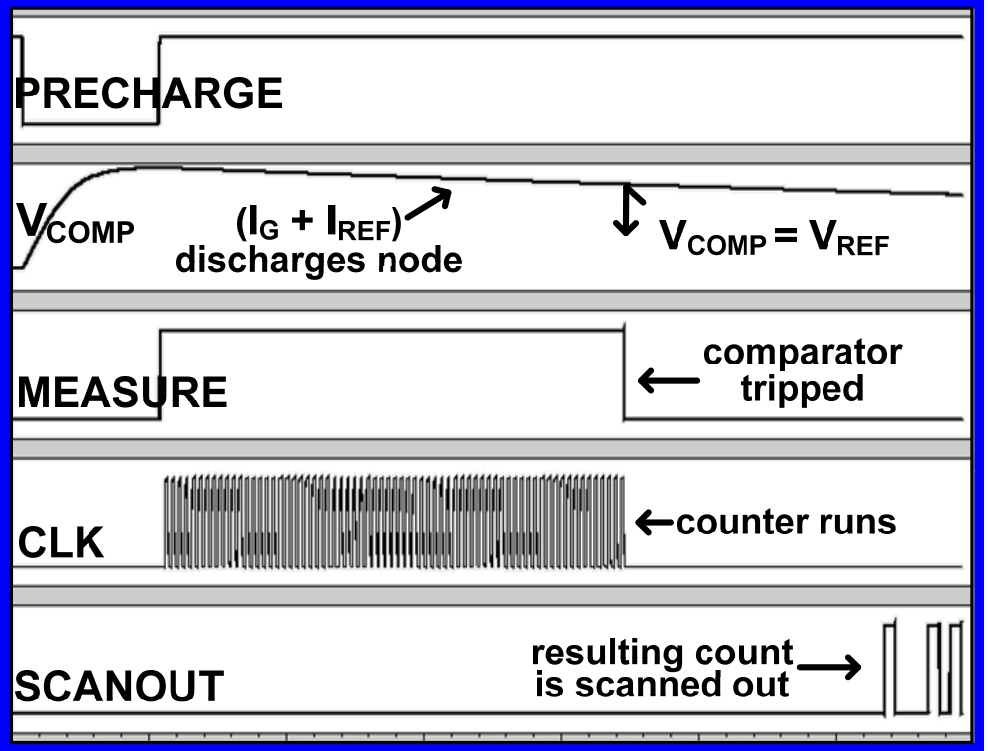
TDDB Stress Cell Design



- Facilitates accelerated stressing of the DUTs by using thick oxide I/O transistors in the supporting circuitry
- row<n> and col<m> signals used to select one cell
- FRESH signal used to gate off stress in any cell(s)
- 2 transmission gates cut off bitline leakage

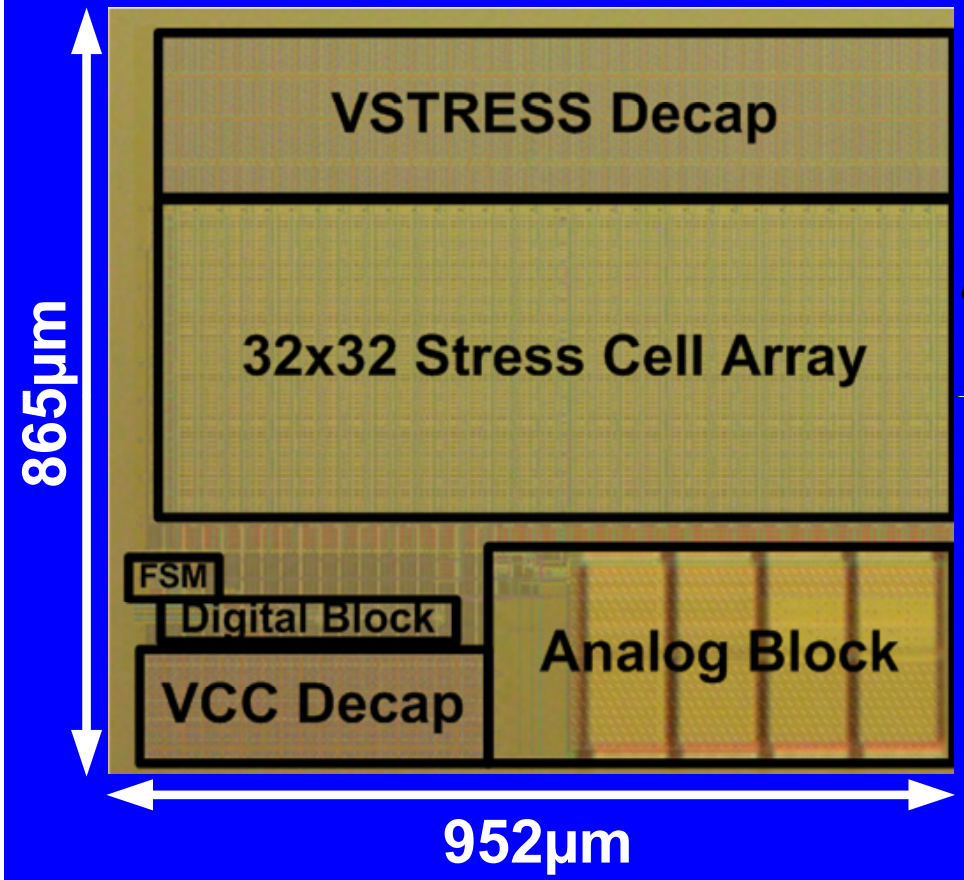
A/D Current Monitor

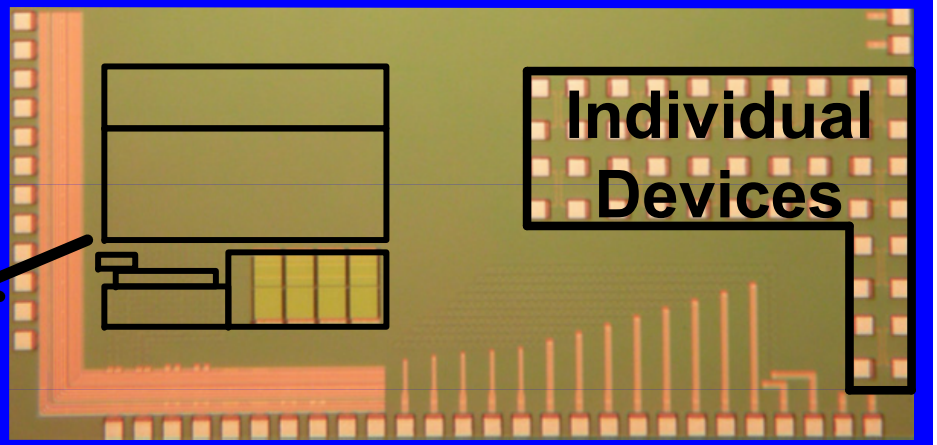




- Comparator output drops when V_{COMP} falls to V_{REF}
- Discharge rate is determined by I_G plus I_{REF}
- 16 bit counter runs at rate set by a VCO
- Less I_G translates to a higher count result

Test Chip Implementation

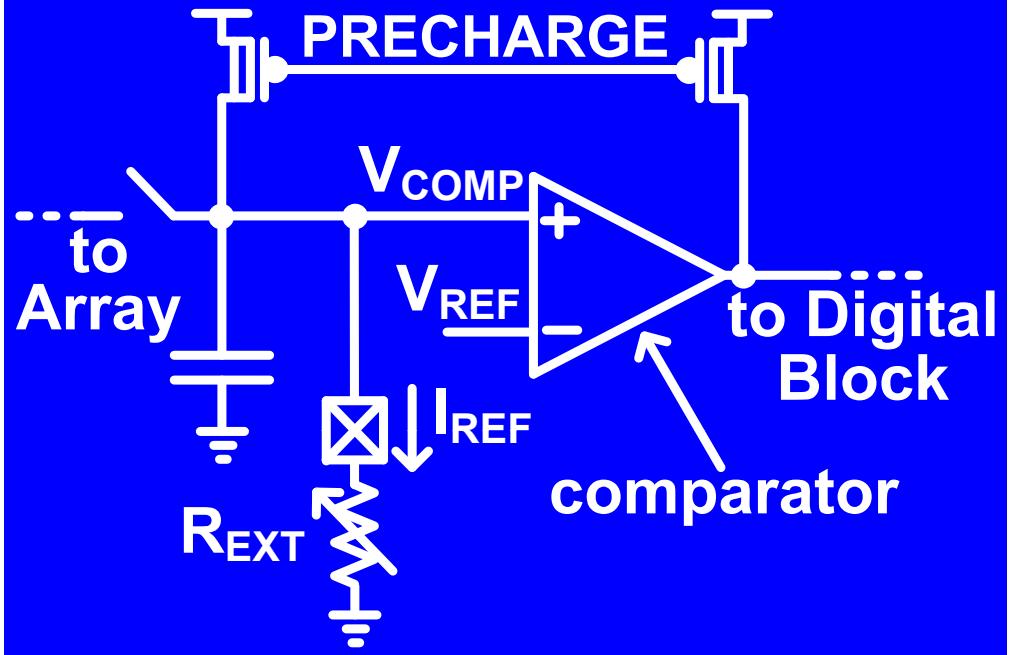


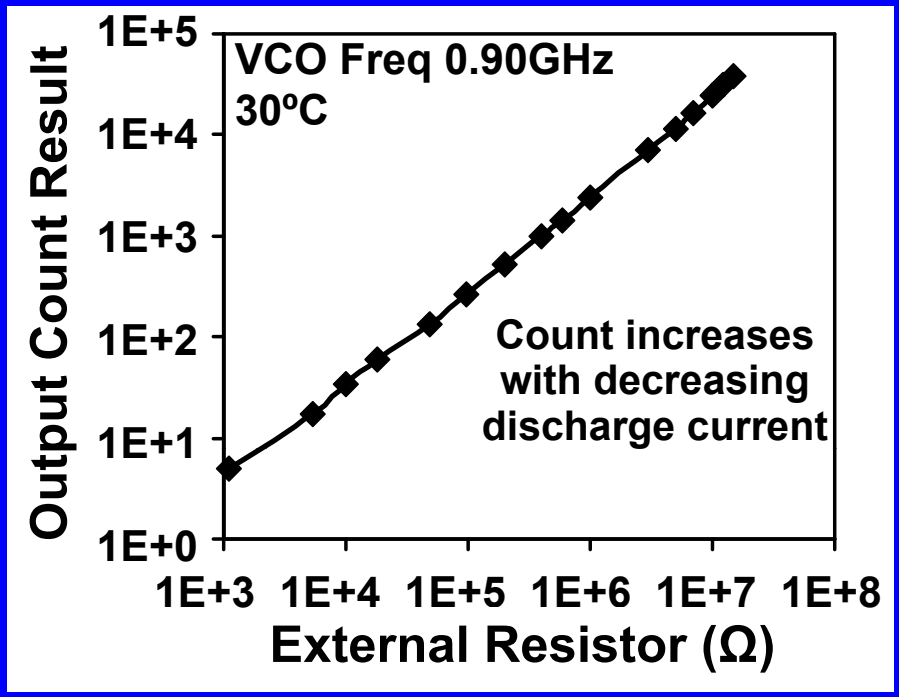


Technology	0.13µm CMOS
Digital Supply	1.2V
Dimensions	952x865µm^2
Gate Resisistance Measurement Range	~1kΩ +

- Measurements automated with LabVIEW and a National Instruments data acquisition board

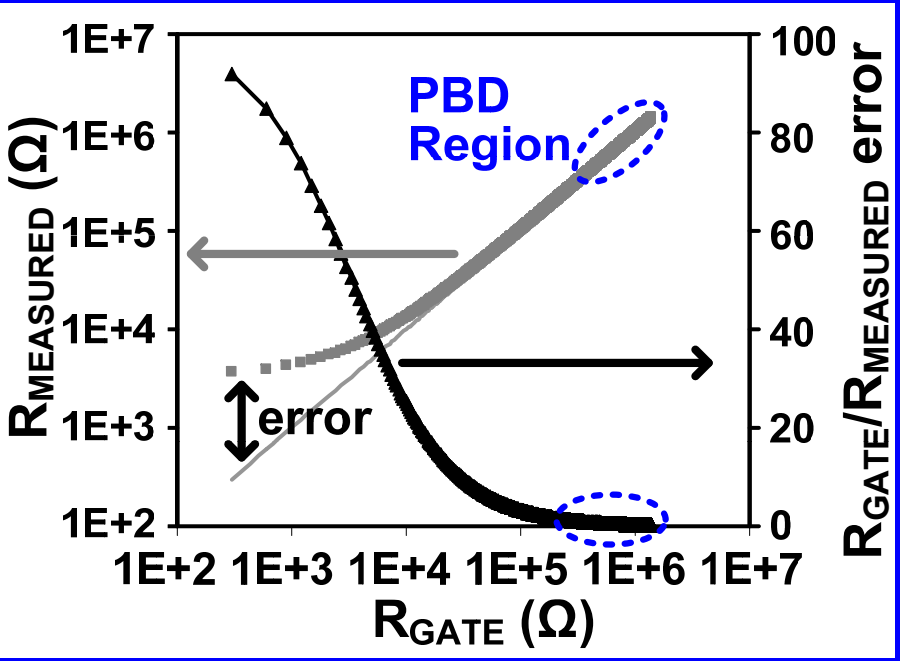
Measurement Array Calibration

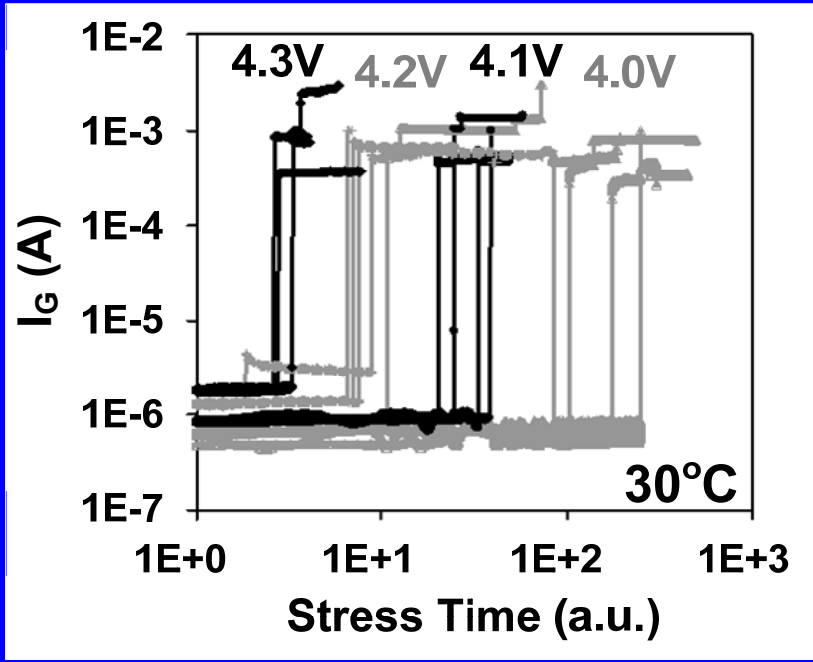




- Obtain final count vs. total discharge path resistance characteristic with adjustable R_{EXT} while A/D monitor is isolated from the array
- Subsequent measurement results translated into gate path resistance (R_{GATE}) by using this calibration curve
  - $R_{TOTAL} = R_{EXT} \parallel R_{GATE}$ (R_{EXT} fixed during measurements)

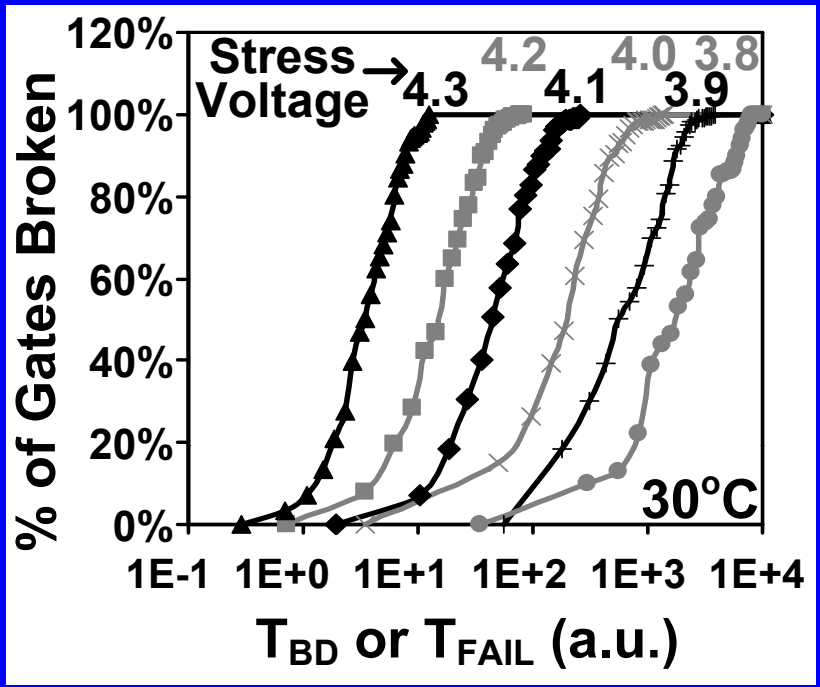
TDDB Array Measurement Issues

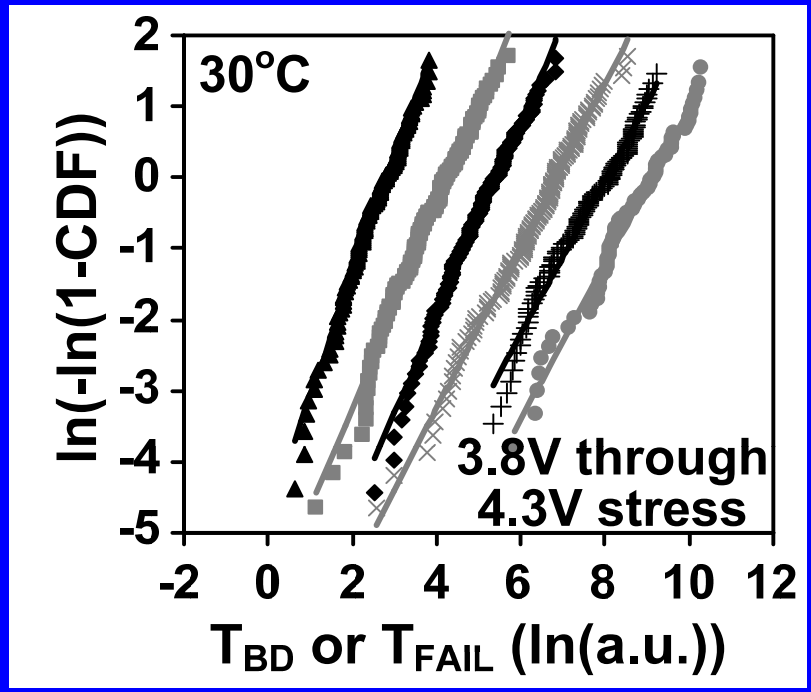




- Resistance of transmission gates on measurement path not accounted for in calibration
- Error < 1.4% for R_{GATE} of 240kΩ+; I_G up to 5μA at 1.2V.
  - Small error in progressive breakdown (PBD) region
- Device probing measurements show hard BD at our stress voltage levels of interest with ~4Hz sampling

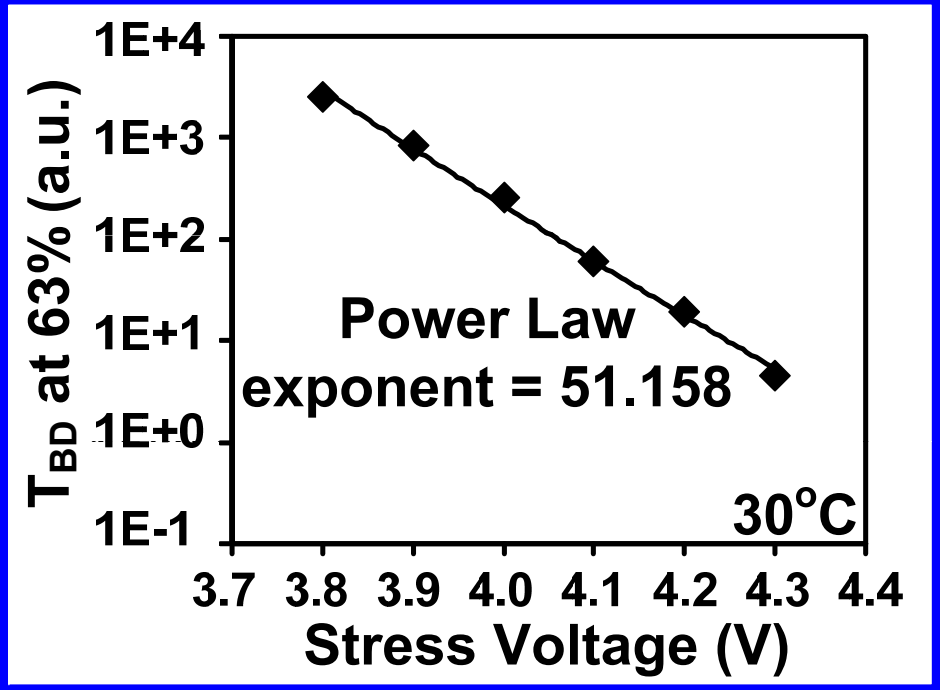
Measured T_{BD} Distributions

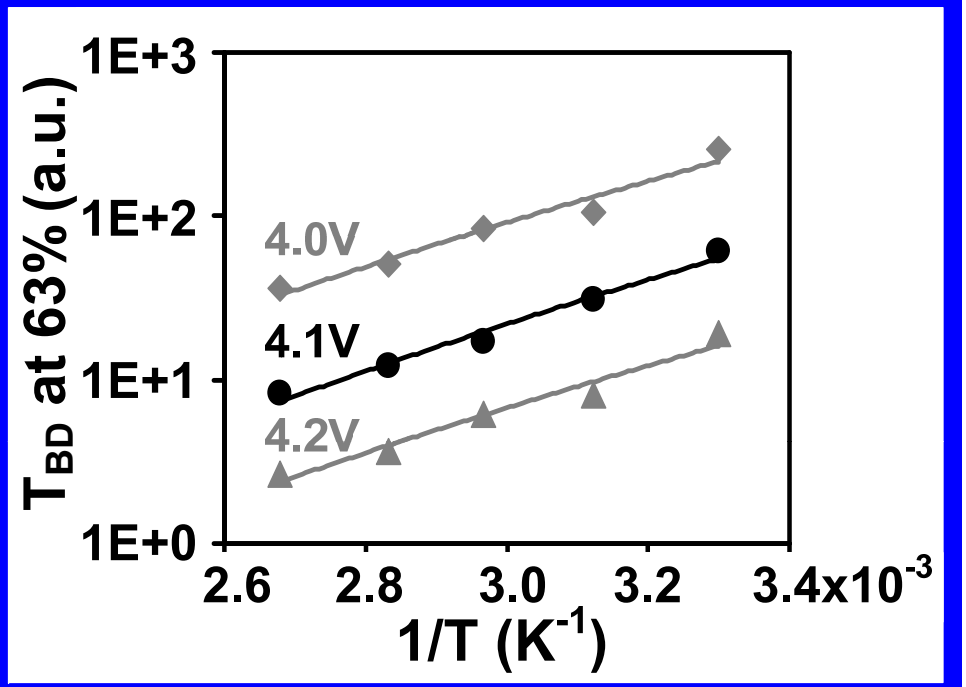




- CDFs of T_{BD} for a range of stress voltages
  - Standard percentage scale (left), and Weibull scale (right)
- The Weibull slope factor (β) for 4.2V stress was 1.443
  - Slightly decreases for lower VSTRESS; increases at 4.3V
- Array-based design allows us to define an accurate CDF with a single test

TDDB Measurement Results





- Exponential relationship of characteristic life with voltage
- In 30°C to 100°C range, TDDB follows Arrhenius behavior
- Careful studies of voltage and temperature acceleration required, particularly in advanced processes, where there has been some debate due to differing results

TDDB Area Scaling

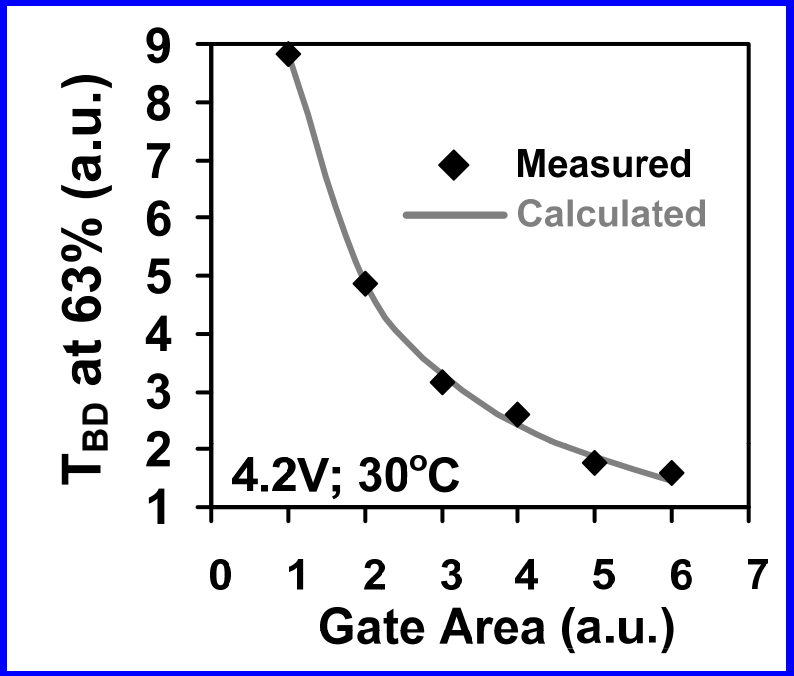
Area Scaling Equation

$$T_{BD}(A_1) = T_{BD}(A_2)\left[\frac{A_2}{A_1}\right]^{1/\beta}$$

T_{BD} : Time-to-Breakdown

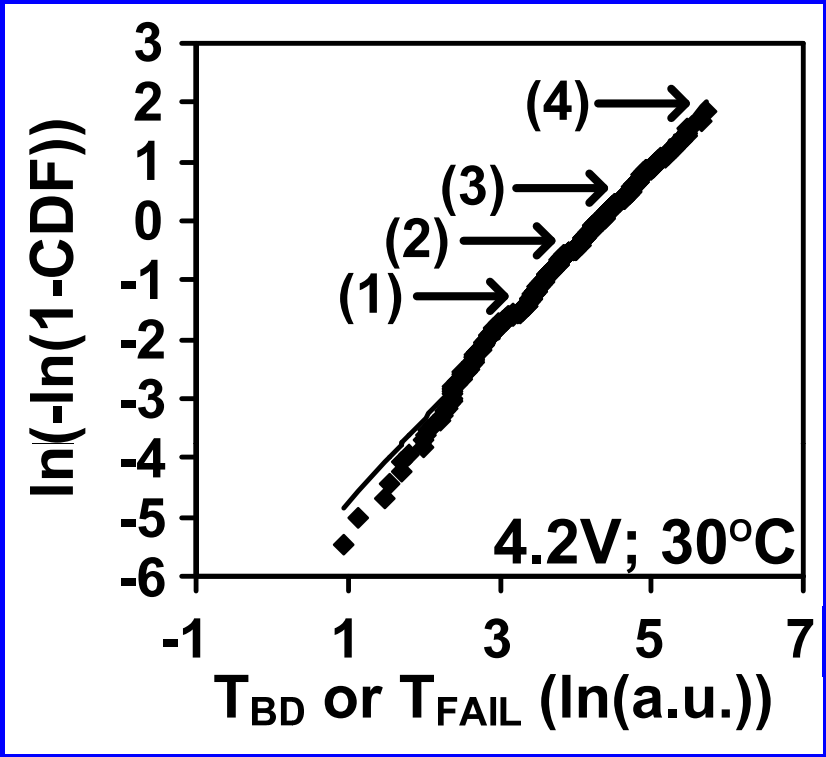
A_1 and A_2 : 2 gate dielectric areas

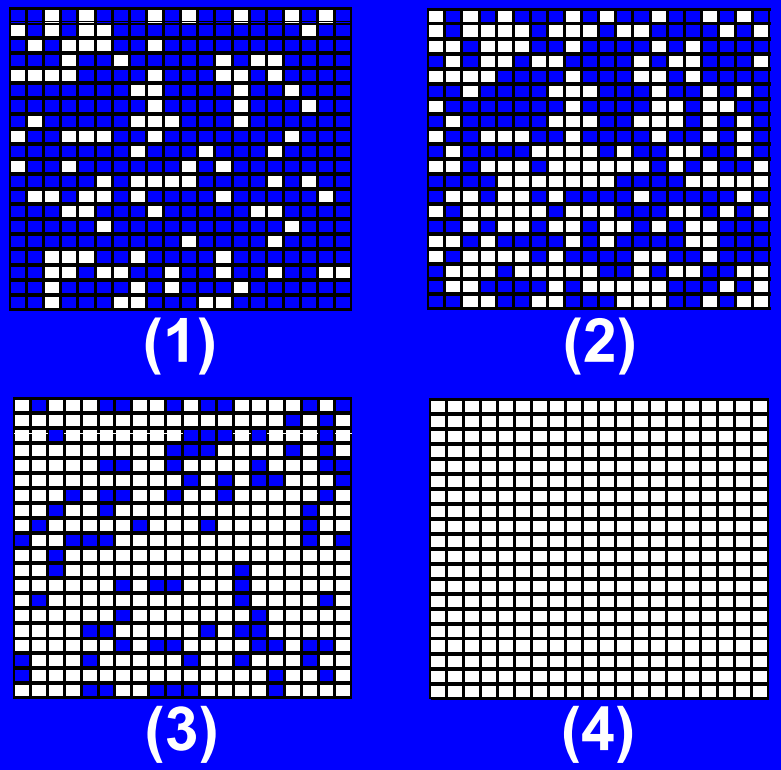
β : Weibull slope



- Select smallest T_{BD} from cluster of adjacent DUTs
  - Measured results match well with the weakest-link theory
  - Helps justify the use of Weibull statistics
- Can be used to determine β with fewer experiments
  - Do stress experiments on DUTs with large area ratio
  - Low sensitivity to statistical variation

Measured T_{BD} Spatial Distribution





- Array format facilitates study of any spatial correlation
- 4 diagrams correspond to 4 divisions of the CDF, each representing 25% of the cells in a 20x20 array.
- No spatial correlation was detected

Conclusions

- Implemented a 32x32 array of TDDB test cells for efficient characterization of T_{BD} statistics
- Stress cell design presented to avoid aging in supporting circuitry
- 16b result easily stored in spreadsheet for processing
- Reduces test time by a factor proportional to # of DUTs
- Design is capable of tracking R_{GATE} progression with ≤1.4% error up to the onset hard breakdown
- Measurement results from a number of stress conditions demonstrate circuit flexibility