A Voltage Scalable 0.26V, 64kb 8T SRAM with V_{min} Lowering Techniques and Deep Sleep Mode

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***Abstract*- A voltage scalable 0.26V, 64kb 8T SRAM with 512 cells per bitline is implemented in a 130nm CMOS process. Reverse short channel effect was utilized to improve cell write margin and read performance. A marginal bitline leakage compensation scheme was used during read operation to lower V_{min} down to 0.26V. Floating write bitline and read bitline, auto wordline pulse width control, and a deep sleep mode minimize the active and standby leakage power consumption.**

I. INTRODUCTION

Subthreshold logic circuits are becoming increasingly popular in ultra-low power applications where minimal power consumption is the primary design constraint [1][2][3][4]. Subthreshold static CMOS logic can operate while consuming roughly an order of magnitude less power than in the normal strong-inversion region. However the MOS current becomes an exponential function of gate and threshold voltage in the subthreshold regime. This leads to an exponential increase in MOS current variability under Process-Voltage-Temperature (PVT) fluctuations.

SRAMs that can operate under a wide range of supply voltages are necessary for achieving high-performance during normal modes while minimizing the power consumption during low voltage modes [5]. For reliable operation from the super-threshold region down to the deep sub-threshold region, key memory design metrics such as noise margin, speed, and power consumption need to be examined at different supply voltages and accounted for as such. In the subthreshold region, conventional 6-T SRAMs fail to deliver the density and yield requirements due to the reduced Static Noise Margin (SNM), poor writability, limited number of cells per bitline, and reduced bitline sensing margin. Decoupled SRAM cells have been proposed to make the read mode SNM equal to the hold mode SNM by isolating the SRAM cell nodes from the bitline [6][7][8][9]. Writability has been improved in prior designs by using a higher supply voltage for the write access transistors at the cost of generating and routing the extra supply voltage [6].

In this work, we demonstrate a 64kb SRAM with several circuit techniques that can be activated at ultra low voltages to expand the operating range: (i) 8T SRAM cell utilizing Reverse Short Channel Effect (RSCE) for improved writability and read performance, (ii) Marginal Bitline Leakage Compensation (MBLC) scheme for improved read sensitivity and precharge elimination, (iii) floating Read BitLines (RBL) and Write BitLines (WBL) to minimize bitline leakage, (iv) deep sleep mode, and (v) automatic read wordline pulse width control for power reduction and improved bitline sensing margin.

II. V_{min} LOWERING CIRCUIT TECHNIQUES

A. 8T SRAM Cell Utilizing Reverse Short Channel Effect

Reverse Short Channel Effect (RSCE) becomes pronounced at lower supply voltages due to the significantly reduced Drain Induced Barrier Lowering (DIBL) effect [9]. This increases the current drivability per width as the channel length increases at sub-0.6V. The proposed 8T SRAM cell uses 3X longer channel length in the write access devices and 2X longer channel length in read path devices (Fig. 1). This improves the write margin from -90mV to 70mV and the read performance by 52% at 0.2V without increasing bitline capacitance. The proposed 8T SRAM cell utilizing RSCE has an area overhead of 20% compared to conventional 8T cells [10].

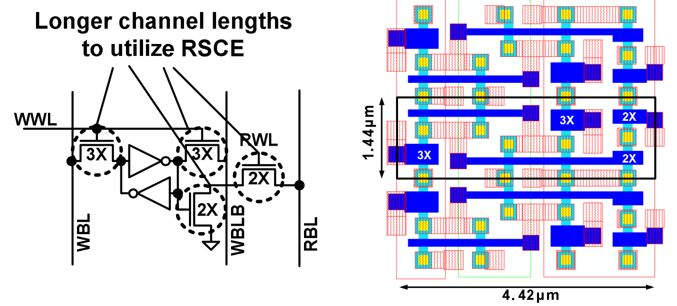

Figure 1. Schematic and layout of the proposed 8T SRAM cell utilizing Reverse Short Channel Effect (RSCE).

B. Marginal Bitline Leakage Compensation (MBLC) Scheme

A Marginal Bitline Leakage Compensation (MBLC) scheme shown in Fig. 2 compensates for the RBL leakage in the unaccessed cells. The RBL voltage is tuned to settle just above the Sense Amplifier (SA) trip point by progressively turning on the marginal compensation devices, which is based on a replica bitline circuit. When a logic '0' is read, only a small swing is required to change the SA output, which is beneficial when a cell current is comparable to the bitline leakage current. The logic level of RBL during read operation is decided by the balance between the cell read current, the pull-down leakage current, and this marginal compensation current. The marginal compensation current should be large enough to produce logic '1' for the worst case pull-down leakage current, while still being small enough to produce logic '0' for the pull-down cell current and the smallest bitline leakage. The optimal compensation current is generated by the replica bitline. A feedback loop charges RBL_REPLICA up to a point where the SA output switches to '1'. The worst case data pattern is hardwired in the replica bitline. Initially, the SA output is '0' because PCHG<3:0> is initialized with '1's, turning off all marginal precharge devices. An increasing

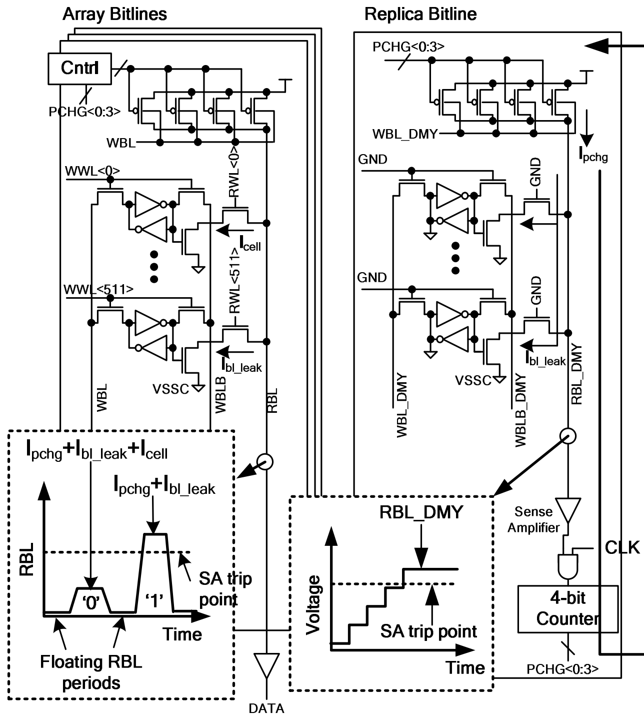

Figure 2. Marginal Bitline Leakage Compensation (MBLC) scheme.

number of pull-up devices are then turned on until the SA output switches to '1'. Additional margin can be given by providing added compensation current through selectively turning on extra devices in the accessed bitline. The optimal compensation current depends on the data pattern in a column, since the amount of bitline leakage is related to the column data. This data dependency was accounted for by connecting the body of the compensating PMOS devices to the floating WBL voltage, which is also determined by the data pattern stored in the SRAM column. Increasing the number of cells storing '0' decreases the floating WBL voltage, which in turn increases the amount of marginal compensation current by forward body biasing the PMOS devices.

III. Active Leakage Reduction And Deep Sleep Mode

A. Floating Read/Write Bitlines

Leakage current in inactive memory cells account for most of the SRAM power consumption. Circuit techniques for leakage control are critical for reducing the total power consumption, especially in the sub-threshold region. RBL leakage is one of the most dominant leakage components and is inevitable in conventional memories where bitlines have to be precharged to VDD. In our design, RBL is left floating without being precharged whenever RWL is low. During the read operation, the MBLC scheme provides the compensation pull-up current to generate logic high or low levels in the RBL with large sensing margin. Write bitline (WBL) is also left floating when WWL is low so that it will automatically settle to a level which minimizes the leakage current as shown in Fig. 3. The proposed scheme has no energy overhead during the write operation compared to the conventional scheme. A total SRAM leakage reduction of 44% to 60% can be obtained by using floating RBLs and WBLs.

B. Deep Sleep Mode

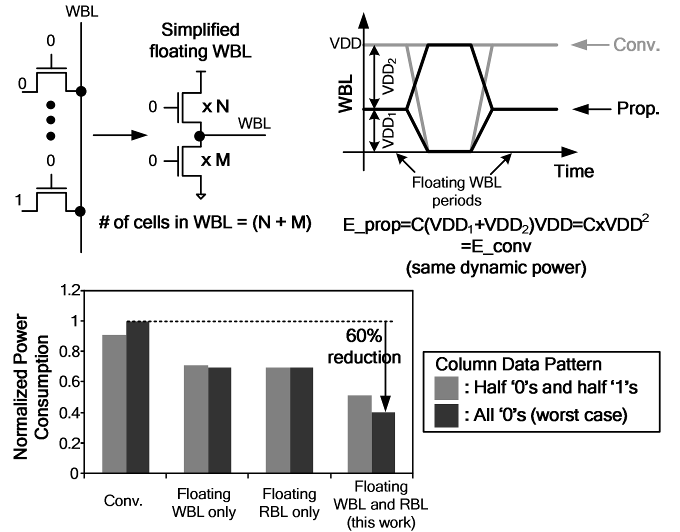

Figure 3. Power reduction using floating read and write bitlines.

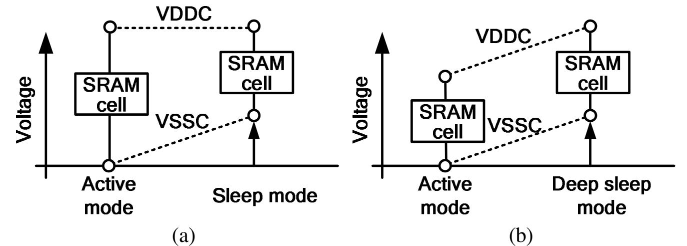

Figure 4. (a) Conventional sleep mode. (b) Proposed deep sleep mode.

Sleep transistors are popular for reducing SRAM leakage current in standby mode by collapsing the virtual supply rails. However, due to the fact that the voltage margin is already close to the functionality limit, it is difficult to use conventional footer sleep transistors for subthreshold designs. In this work, we propose a deep sleep mode illustrated in Fig. 4 to reduce the standby leakage in subthreshold memory designs. During sleep mode, the proposed scheme raises both VDDC and VSSC while keeping the cell voltage, VDDC-VSSC, constant to reduce leakage while maintaining the same cell stability in deep sleep mode. SRAM cell leakage is reduced due to the negative VGS in the write access transistors and the increased threshold voltage of the pull-down NMOS devices due to the reverse body bias. Raising the VDDC and VSSC too high may increase the WBL and WBLB levels because they are decided by the column data pattern and the SRAM cell node voltages. If both VDDC and VSSC are raised excessively, the pull-up path in the interfacing circuit becomes leaky and current starts to flow from WBL and WBLB to VDDP. Fig. 5 demonstrates the leaky current path and the normalized SRAM leakage current reduction obtained by using the proposed deep sleep mode. By applying an optimal supply voltage (VDDC=0.83V, VSSC=0.60V), 87% reduction in cell leakage was obtained during a deep sleep mode.

C. Automatic Wordline Pulse Width Control

The pulse width of wordline signals should be carefully controlled to avoid access failures while minimizing the delay and power overhead. Due to the fact that read speed is highly dependent upon the PVT conditions, a scheme to

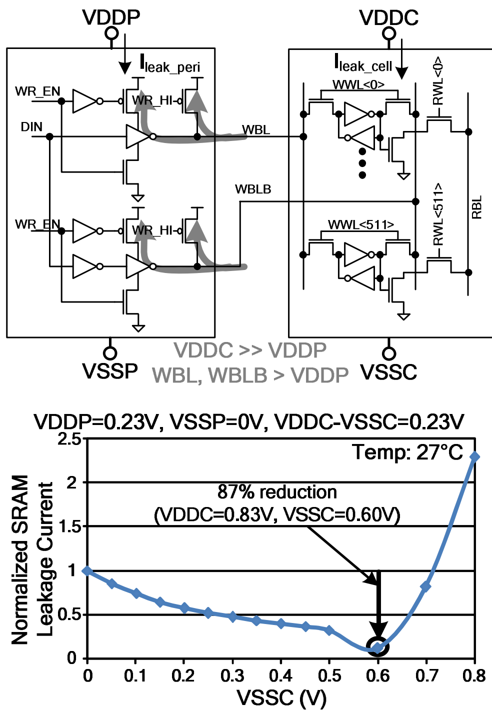

Figure 5. Deep sleep mode and simulated leakage reduction.

automatically adjust the read wordline pulse width based on PVT variations is proposed (Fig. 6). A replica bitline is used to generate the amount of delay necessary for the SA to capture the read data. The delayed SA output RD_FIN from the replica bitline disables the read wordline and shuts off the marginal precharge devices. Added delay, which can be trimmed, takes care of the within die variations. The proposed wordline pulse width control scheme also reduces the unnecessary read power consumption by minimizing the wordline enable time.

IV. EXPERIMENTAL RESULTS

A 64kb SRAM was fabricated in a 130nm CMOS technology with a nominal supply voltage of 1.2V. Fig. 7 shows the measured power consumption and leakage current. We observed SRAM cells functional down to 0.23V running at 100kHz and consuming 4.3μW (Fig. 7 (a)). At 0.4V, the operation frequency was 6.7MHz with a power consumption of 10.8μW. The measured SRAM leakage currents from different dies are shown in Fig. 7 (b). Variation in leakage current was 2.0X at 0.3V due to its exponential dependency on device threshold voltage. The normalized leakage current measured at different temperatures is shown in Fig. 7 (c). The leakage current at 110°C is 3.4X larger than that at 27°C when the supply voltage is 0.23V. Fig. 7 (d) illustrates the normalized leakage current reduction achieved using the proposed deep sleep mode. The total SRAM leakage including the array and peripheral components was reduced by 69% in deep sleep mode by raising the VSSC to 0.45V while maintaining a cell voltage of 0.23V. The initial leakage reduction is large when raising VSSC due to the strong negative Vgs effect in conjunct with the reverse body biasing

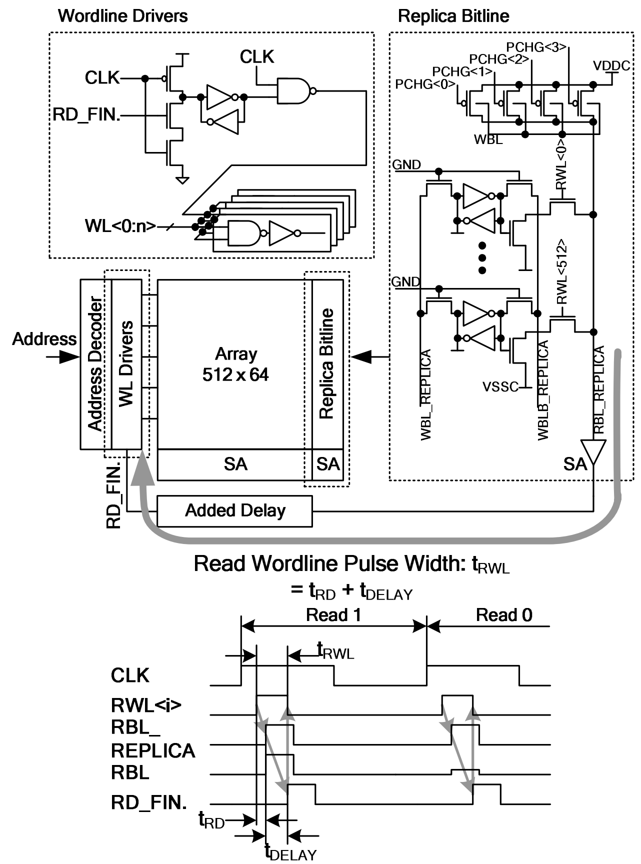

Figure 6. Read wordline pulse width control for PVT tracking.

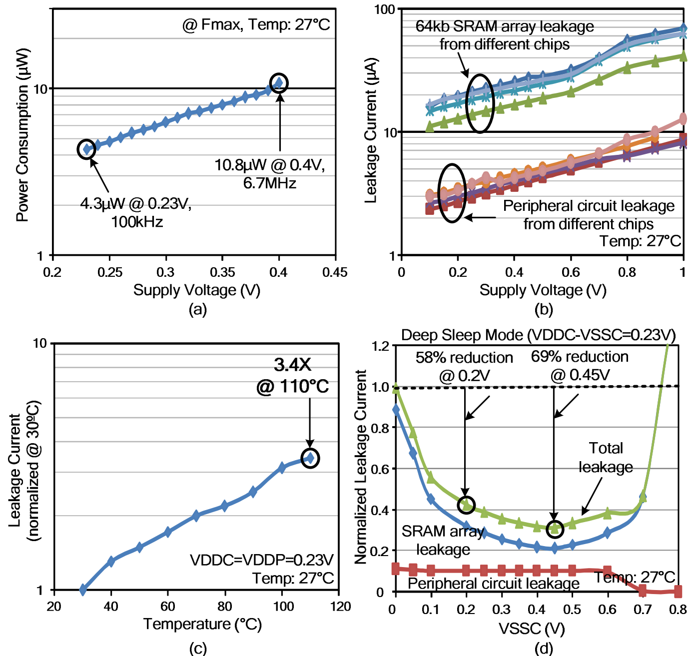

Figure 7. (a) Measured SRAM total power consumption. (b) SRAM leakage current varying supply voltage. (c) Normalized leakage current at different temperature. (d) Leakage current reduction in deep sleep mode.

effect. 58% leakage reduction was achievable using a VSSC of 0.2V during deep sleep mode. The smaller offset in VDDC and VSSC improves the efficiency and area overhead of the

charge pumps that generate the boosted voltages. In this test chip, we used an external supply for the higher supply voltages needed during the deep sleep mode.

Fig. 8 (a) shows the shmoo plot when the proposed MBLC scheme is on and off. When the MBLC scheme is off, a conventional fixed precharge device is used. The V_{min} of the implemented SRAM is reduced from 0.28V to 0.23V by activating the MBLC scheme. V_{min} map for read and write operations for an 8-by-8 subarray is shown in Fig. 8 (b). We have also tested the feedback control circuit for the MBLC scheme which compensates the bitline leakage on-the-fly. The 4 bit counter used in the MBLC requires up to 16 clock cycles to generate the optimal precharge strength. Fig. 9 shows SA

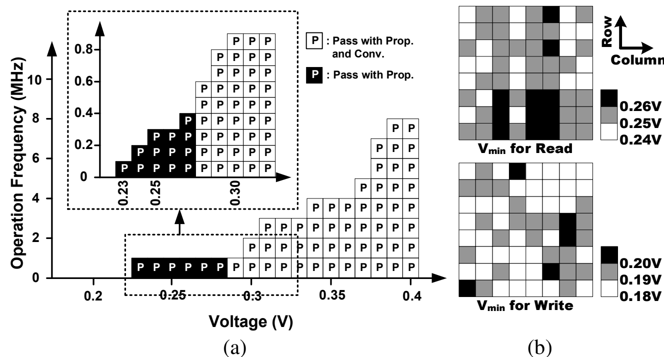

Figure 8. (a) Shmoo plot for an SRAM cell with a 0.23V V_{min}. (b) V_{min} for read and write from an 8-by-8 subarray.

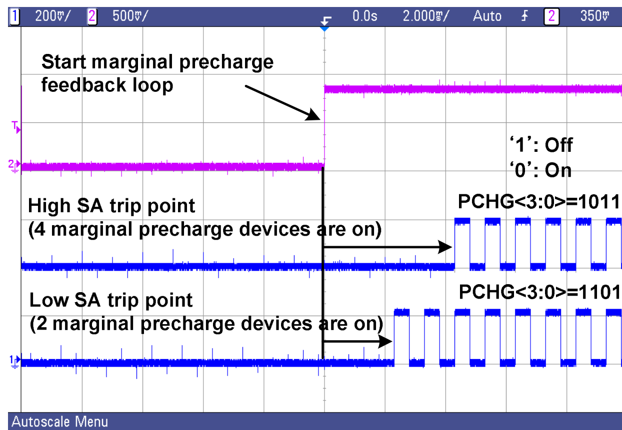

Figure 9. Output waveforms from marginal bitline leakage compensation control circuit.

Technology	130nm 8-metal CMOS
SRAM Area	0.72x0.85mm^2
VCC	≥0.26V
Size	64kb
Performance	100kHz @ 0.23V, 27°C 15MHz @ 0.60V, 27°C
Power Consumption	4.3µA @ 0.23V, 27°C 34µA @ 0.60V, 27°C
Deep Sleep Mode Leak.	69% reduction

Figure 10. Chip microphotograph and performance summary.

outputs with two different trip points. It is shown that a SA with a higher trip point requires additional cycles to turn on more number of compensation devices. Similarly, more devices should be turned on for a larger bitline leakage current due to process variations. The die photo and chip performance summary are given in Fig. 10. The proposed MBLC and read wordline pulse width control scheme incur an area overhead of 1.3%.

V. Conclusions

A 64kb SRAM was fabricated in a 130nm CMOS technology with 512 cells per bitline. The SRAM was functional down to 0.23V running at 100kHz and consuming 4.3µW. RSCE was utilized in the read and write port of the SRAM cell to improve write margin and read performance. The MBLC scheme was proposed to expand V_{min} down to 0.23V. Floating read and write bitline scheme was proposed to eliminate RBL leakage current during non-read operation and minimize write bitline leakage current during non-write operation. Deep sleep mode for subthreshold memories was proposed to further reduce the leakage current during standby mode. The total SRAM leakage including the array and peripheral components was reduced by 69% in deep sleep mode by raising the VSSC to 0.45V while maintaining a constant cell voltage. An automatic read wordline pulse width control scheme improves readability and reduces wasted read power by tracking the PVT variations.

References

[1] H. Kim, H. Soeleman, K. Roy, "An ultra-low power DLMS filter for hearing aid applications", IEEE Trans. VLSI Systems, Volume 11, , pp. 1058-1067, Dec. 2003.

[2] A. Bryant, J. Brown, P. Cottrell, et al., "Low-power CMOS at Vdd=4kT/q", Device Research Conference, pp. 22-23, 2001.

[3] B. Zhai, S. Hanson, D. Blaauw, D. Sylvester, "Analysis and mitigation of variability in subthreshold design", International Symposium on Low Power Electronics and Design, pp. 20-25, Aug. 2005.

[4] A. Wang, A.P. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology", IEEE J. of Solid-State Circuits, Volume 40, pp. 310-319, Jan. 2005.

[5] L. Chang, Y. Nakamura, R.K. Montoye, J. Sawada, et al., "A 5.3GHz 8T-SRAM with operation down to 0.41V in 65nm CMOS", VLSI Circuits Symposium, pp. 252-253, June 2007.

[6] B.H. Calhoun, A. Chandrakasan, "A 256kb Sub-threshold SRAM using 65 nm CMOS," International Solid-State Circuits Conference, pp. 628-629, Feb. 2006.

[7] L. Chang, D.M. Fried, J. Hergenrother, J.W. Sleight, et al., "Stable SRAM cell design for the 32 nm node and beyond," Symposium on VLSI Technology, pp. 128-129, June 2005.

[8] J. Chen, L. T. Clark, T. Chen, "An Ultra-Low-Power Memory with a Subthreshold Power Supply Voltage," IEEE J. of Solid-State Circuits, Volume 41, pp. 2344-2353, Oct. 2006.

[9] T. Kim, J. Liu, J. Keane, C. Kim, "A high-density subthreshold SRAM with data-independent bitline leakage and virtual ground replica scheme", International Solid-State Circuits Conference, pp. 330-331, Feb. 2007.

[10] T. Kim, J. Liu, C. Kim, "An 8T Subthreshold SRAM Cell Utilizing Reverse Short Channel Effect for Write Margin and Read Performance Improvement", Custom Integrated Circuits Conference, pp. 241-244, Oct. 2007.