# Utilizing Reverse Short-Channel Effect for Optimal Subthreshold Circuit Design

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***Abstract*—The impact of the reverse short-channel effect (RSCE) on device current is stronger in the subthreshold region due to reduced drain-induced barrier lowering (DIBL) and the exponential dependency of current on threshold voltage. This paper describes a device-size optimization method for subthreshold circuits utilizing RSCE to achieve high drive current, low device capacitance, less sensitivity to random dopant fluctuations, better subthreshold swing, and improved energy dissipation. Simulation results using ISCAS benchmark circuits show that the critical path delay, power consumption, and energy consumption can be improved by up to 10.4%, 34.4%, and 41.2%, respectively.**

***Index Terms*—Circuit optimization, process variation, reverse short-channel effect (RSCE), subthreshold operation.**

## I. Introduction

EMERGING ultralow-power applications such as portable devices, medical instruments, and wireless sensor networks demand extremely low supply voltages in order to meet stringent power budgets. Subthreshold circuits, which operate at supply voltages lower than the threshold voltage $(V_{\rm th})$, are considered to be promising candidates for ultralow-power systems where operating speed is not the primary design concern. Recently, a significant amount of research has been done dealing with subthreshold circuits. Soeleman *et al.* analyzed various logic styles for subthreshold operation [1]. The impact of PVT variations on subthreshold circuits was investigated in [2] and [3]. Circuits such as analog voltage references, subthreshold SRAMs, tiny-XOR circuits, and adaptive filters for hearing-aid applications have been demonstrated [4]–[8]. New transistor scaling trends specifically for subthreshold circuits have been suggested in [9].

Short-channel devices have been optimized for regular superthreshold circuits to meet various device objectives such as high mobility, reduced drain-induced barrier lowering (DIBL), low leakage current, and minimal $V_{\rm th}$ roll-off. However, a transistor that is optimized for superthreshold logic may not be optimal for achieving high performance and low power in the subthreshold region where effects such as DIBL, $V_{\rm th}$ roll-off, and electron/hole tunneling are much less significant. For example, the reduced DIBL effect in the subthreshold region, due to the low drain voltages, can eliminate the need for high doping in the channel which was traditionally used to overcome the short-channel effect (SCE) [10]. Although it would be ideal to have a dedicated process technology optimized for subthreshold circuits, mainstream CMOS technology will continue to scale aiming at optimal performance in conventional superthreshold circuits. In order to design optimal subthreshold circuits using CMOS devices that are targeted for superthreshold operation, it is crucial to develop techniques that can utilize the side effects that appear in this new regime. The main contribution of this paper is utilizing one such mechanism-the pronounced reverse SCE (RSCE)-to achieve optimal performance in subthreshold circuits.

SCE (or $V_{\rm th}$ roll-off) is an undesirable phenomenon in short-channel devices where $V_{\rm th}$ decreases as the channel length is reduced. Variation in critical device dimensions translates into a larger variation in the threshold voltage as SCE worsens with increasing DIBL [11]. Typically, nonuniform HALO doping is used to mitigate this problem by making the depletion widths narrow and hence reducing the DIBL effect [10]. As a byproduct of HALO, a short-channel device shows RSCE behavior where the $V_{\rm th}$ decreases as the channel length is increased [12], [13]. In subthreshold circuits, the SCE mechanism is not as strong as in superthreshold circuits because the drain-to-source voltage is very small. On the other hand, RSCE is still significant enough to affect the subthreshold performance. Moreover, current becomes an exponential function of $V_{\rm th}$ in this regime, which makes it possible to use longer channel-length devices that utilize RSCE for improving drive current. Unlike the case in superthreshold circuits, using a longer channel length in subthreshold does not have a significant impact on the load capacitance. This is due to the reduced depletion capacitance under the gate.

This paper describes a sizing method that utilizes RSCE to improve performance and power consumption in subthreshold circuits. In Section II, we will illustrate general transistor sizing considerations for subthreshold circuits. Section III describes the proposed method utilizing the RSCE to improve drive current, capacitance, process variation, subthreshold swing, and improved energy dissipation. Experimental results on a simple chain of gates as well as ISCAS benchmark circuits are presented in Section IV. Finally, we draw our conclusions in Section V.

## II. Gate-Sizing Considerations for Subthreshold Circuits

Conventional superthreshold logics require special modifications in order to achieve optimal performance and power consumption in subthreshold operation. For example, the pMOS-to-nMOS width ratio (PN ratio) and stacked device sizing need to be reevaluated for subthreshold operating voltages [14]. The optimal PN ratio for equal current drivability of pMOS and nMOS is roughly 2.5 in superthreshold logics, which comes from the

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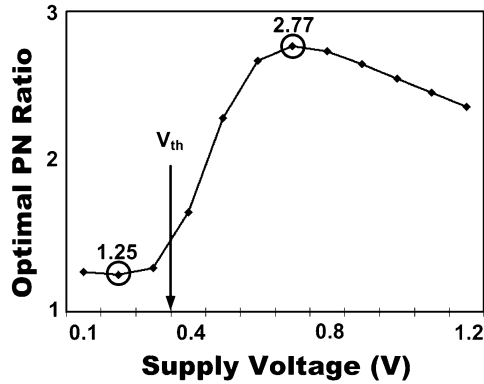


Fig. 1. PN ratio as a function of supply voltage.

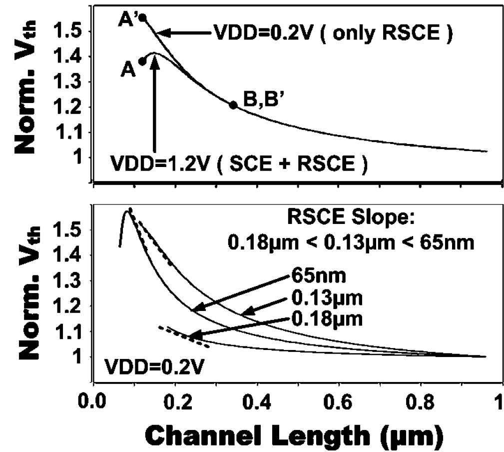


Fig. 2. Dependency of normalized $V_{\rm th}$ on channel length for $\rm VDD = 1.2~V$ and $\rm VDD = 0.2~V$.

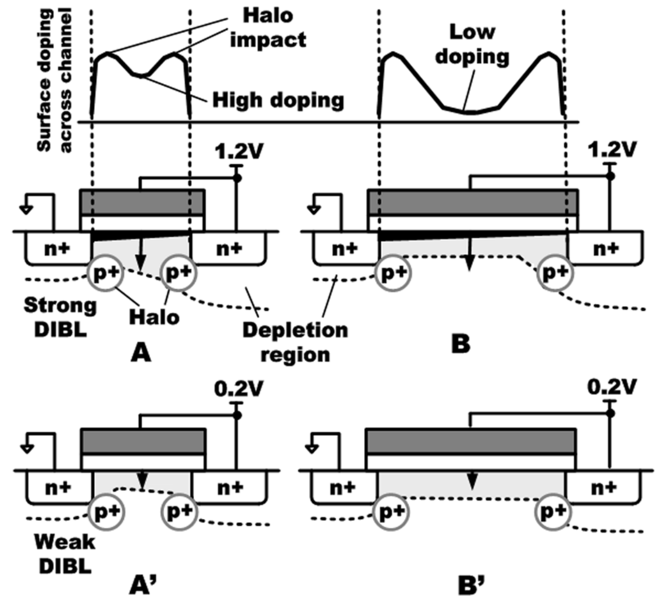


Fig. 3. Device cross sections corresponding to A, A', B, and B' in Fig. 2. Surface doping across the channel is shown to illustrate the RSCE.

mobility and threshold voltage difference. This ratio changes in the subthreshold region because the weak-inversion current is an exponential function of threshold voltage, which differs in pMOS and nMOS devices. The weak-inversion current is also a function of the subthreshold slope and is significantly affected by other secondary effects such as the narrow width effect, SCE, and RSCE. Fig. 1 shows the optimal PN ratio at different supply voltages. The significant reduction in the optimal PN ratio with a lower supply voltage can be attributed to the difference in $\rm V_{th}$ and subthreshold slope. The mobility difference between electrons and holes remains the same as in the superthreshold region. Selection of the proper effective width of stacked transistors is also crucial for achieving optimal performance. The effective width of a transistor in a stack of n devices is roughly $1/n$ in the strong-inversion region. This means that, in order for an n-stack to conduct the same amount of current as a single transistor, the devices in the stack must each be sized up by a factor of $n$. Simulation results indicate that stacks need to be sized up by a larger amount in the subthreshold region due to the weak stack currents. For example, a single-unit nMOS transistor is equivalent to a two-stack with transistor widths of 2.259 at 0.2 V, 2.413 at 0.3 V, and 1.6 at 1.2 V in the 0.13-$\mu$m process technology used here. Consequently, the sizing methods that were used to obtain maximum performance in the superthreshold region must be reformulated in the subthreshold region due to these different device characteristics.

Previous sizing methods for subthreshold logics were based on the traditional assumption that the minimum channel length is still optimal for speed and power. This is true in the superthreshold region, but it does not hold true in subthreshold logic since a device with a longer channel length and a fixed channel width can have higher on-current due to RSCE. The PN ratio will also have to be adjusted when we change the device channel lengths due to its dependency on nMOS and pMOS threshold voltages, which shift with those lengths. Therefore, a new sizing method suitable for subthreshold circuits which considers the impact of RSCE on drive current, device capacitance, and subthreshold slope is indispensable.

## III. Proposed Transistor-Sizing Method Utilizing RSCE

### *A. RSCE*

Fig. 2 (top) shows the threshold voltages as a function of channel length at $\rm VDD = 1.2~V$ and $\rm VDD = 0.2~V$. In the superthreshold region (1.2 V), a strong $V_{\rm th}$ roll-off behavior is observed at the minimum channel length due to the high DIBL effect (point A in Fig. 2). To compensate for the worsening $V_{\rm th}$ roll-off caused by DIBL in small dimensions, nonuniform p+ doping in the source–body and drain–body boundaries, called HALO implants, are used. These regions reduce the amount of control the drain has over the channel by making the depletion layer width narrow. HALO implants can also suppress the body punchthrough [10], [15]. However, as a byproduct of using those implants, the threshold voltage decreases as the channel length increases. This phenomenon is known as the RSCE [12], [13]. The larger distance between the highly doped HALO regions in longer channel devices decreases the surface doping level across the channel, which in turn causes the threshold voltage to decrease.

Fig. 3 (top) illustrates this trend by showing the effective surface doping in the longitudinal direction. RSCE becomes more significant with process scaling due to the higher HALO doping

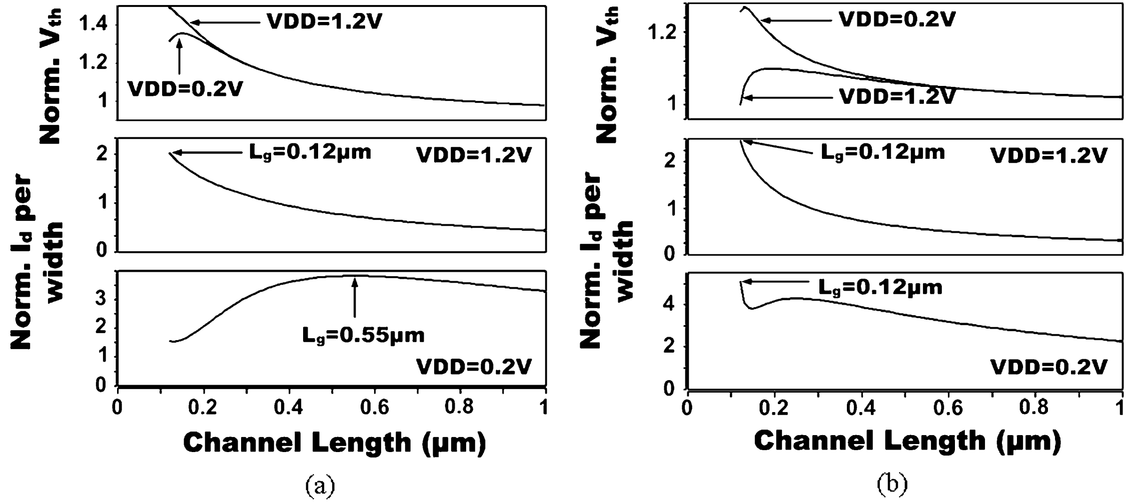


Fig. 4. Dependency of normalized $V_{\rm th}$ and current per width on channel length. (a) nMOS. (b) pMOS.

required to negate the aggravating $V_{\rm th}$ roll-off as shown in Fig. 2 (bottom). The combination of SCE and RSCE causes the $V_{\rm th}$ to peak at a channel length slightly longer than the minimum value in superthreshold devices. RSCE is not a major concern in conventional superthreshold designs since SCE is dominant in minimum channel-length devices in that region. However, in the subthreshold region, only the RSCE effect is present due to the significantly reduced DIBL [10]. This causes the $V_{\rm th}$ to decrease monotonically and operating current to increase exponentially, with longer channel length.

### *B. Optimal Channel Length for Maximum Current Per Width*

As the $V_{\rm th}$ behavior changes significantly in the subthreshold region, the optimal channel length yielding maximum current-per-width changes accordingly. This is illustrated in Fig. 4, where $V_{\rm th}$ and current per width are plotted versus channel length in the subthreshold and superthreshold regions. Maximum current per width is obtained at the minimum channel length (0.12 $\mu$m) for $\mathrm{VDD} = 1.2$ V because the effect of maximized $W/L$ is stronger than that of reduced threshold voltage on the current. However, the optimal channel length for an nMOS at $\mathrm{VDD} = 0.2$ V increases to 0.55 $\mu$m since the lower $V_{\rm th}$ caused by RSCE provides an exponential increase in current [see Fig. 4(a)]. Current is also proportional to $W/L$, which makes it eventually decrease at channel lengths longer than the optimal. In this process technology, only nMOS device lengths are adjusted to utilize RSCE. The nMOS threshold voltage is reduced by 45% when changing the channel length from 0.12 to 0.55 $\mu$m. However, RSCE in pMOS devices is not strong enough in the given technology to provide current gain by increasing channel length, as can be seen in Fig. 4(b). The pMOS threshold voltage is reduced by only 23% which is around 50% of the nMOS threshold voltage change when applying the same channel-length change. The effectiveness of our proposed sizing scheme depends on how strong the RSCE is. pMOS devices can also utilize the pronounced RSCE in future scaled process technologies where stronger RSCE effect is observed, as shown in Fig. 2 (bottom) [16].

Here, we will derive the optimal channel length for maximum current per width in the subthreshold region. The RSCE-affected threshold voltage can be expressed as

$$V_{\rm th} = V_{\rm th0} + K_1 \left( \sqrt{1 + \frac{K_2}{L_{\rm eff}}} - 1 \right) \sqrt{\Phi_s} \tag{1}$$

where $V_{\rm th0}$ is the zero-bias threshold voltage of a long channel device, $K_1$ and $K_2$ are technology parameters that are positive numbers, $L_{\rm eff}$ is the effective channel length, and $\Phi_s$ is the surface potential. The DIBL effect is omitted because its effect is negligible in the subthreshold region. Body effect is ignored for simplicity. The optimal channel length can be obtained by taking the derivative of the current equation

$$I_D = I_{D0} \frac{W}{L_{\rm eff}} e^{\frac{V_{\rm GS} - V_{\rm th}}{m V_1}} \left( 1 - e^{\frac{-V_{\rm DS}}{V_t}} \right) \tag{2}$$

$$\frac{\partial I_D}{\partial L_{\rm eff}} = 0. \tag{3}$$

Here, $m$ is a technology parameter and $V_t$ is the thermal voltage. By solving (3), we can derive the optimal channel length for maximum current per width as

$$L_{\rm eff}^2 + K_2 L_{\rm eff} + K_3 = 0 \tag{4}$$

$$L_{\rm eff} = \frac{-K_2 + \sqrt{K_2^2 - 4K_3}}{2} \tag{5}$$

$$K_3 = -\frac{K_1^2 \Phi_S}{m^2 V_t^2} K_2. \tag{6}$$

The optimal channel length calculated using the analytical expression in (5) is 0.58 $\mu$m, which is very close to 0.55 $\mu$m from simulation. We can also compare the current at the optimal channel length given by (5) with that at minimum channel length for validation. The maximum current per width is 2.5 times larger than that at the minimum channel length in this process technology. However, using a longer channel length can have a negative impact on device capacitance, which can affect

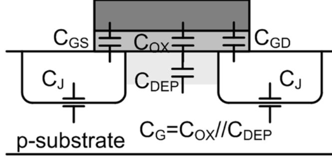


Fig. 5. Capacitance in a subthreshold MOS device.

the $CV/I$ delay. In Section III-C, we derive the optimal channel length for maximum performance considering the RSCE and device capacitance behavior in the subthreshold region.

### C. Optimal Channel Length for Maximum Performance

We have shown that, for subthreshold circuits, the maximum current can be obtained at a channel length that is significantly longer than the minimum defined by the technology node. This phenomenon is attributed to the effect of RSCE on threshold voltage and current. Another factor to consider when increasing the channel length for optimal subthreshold sizing is the increase in device capacitance. Delay and power consumption increases linearly with capacitance.

Fig. 5 shows the different components of device capacitance in the subthreshold region. Each component can be described as follows:

$$C_{\text{DEP}} = \frac{\varepsilon_{si}}{W_{\text{DEP}}}$$

$$C_{\text{OX}} = \frac{\varepsilon_{\text{OX}}}{t_{\text{OX}}} \tag{7}$$

$$C_{\text{GD}} = C_{\text{GS}} = WC_{\text{OV}} \tag{8}$$

$$C_J = WC_j + (2W + L_j)C_{jsw} \tag{9}$$

where $W_{\text{DEP}}$ is the depletion width, $t_{\text{ox}}$ is the oxide thickness, $W$ is the device width, $C_{\text{OV}}$ is the overlap capacitance per width, $C_j$ is the junction capacitance per width, $L_j$ is junction length, and $C_{jsw}$ is the junction sidewall capacitance.

In order to illustrate the effectiveness of increasing the channel length, the capacitances of a transistor having a constant current is plotted versus channel length in Fig. 6. Note that the device width can be reduced as the channel length is increased since RSCE lowers the $V_{\text{th}}$ and exponentially increases the device current. This was not the case for superthreshold circuits, where the decrease in $W/L$ had a larger impact on current than the reduction in $V_{\text{th}}$ due to RSCE. Increasing the channel length alone has no effect on junction capacitance $(C_J)$ because $C_J$ is only proportional to device width. However, since the device width is reduced simultaneously for constant current, the junction capacitance also goes down with a longer channel length, as shown in Fig. 6. Simulation results showed that the junction capacitance can be reduced by 50%. The increase in gate capacitance $(C_G)$ is moderate between channel lengths of 0.12 and 0.36 $\mu$m for two reasons. First, the reduction in width makes the increase in gate area smaller. In this design, the gate area is increased by 50%. Second, the RSCE associated with longer channel length makes the depletion capacitance $(C_{\text{DEP}})$ smaller since the depletion layer width under gate increases as the channel length increases, which is shown in Fig. 3 (bottom).

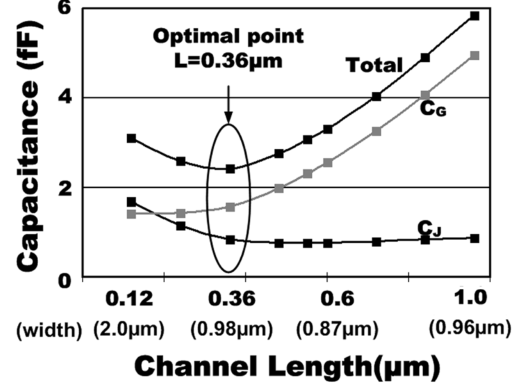


Fig. 6. Capacitance versus channel length for constant current.

At channel lengths longer than 0.36 $\mu$m, however, $\text{C}_\text{G}$ increases rapidly since the RSCE becomes weaker, and gate area is increased to drive the same current. As a result, there exists a minimum point in total capacitance for iso-current at a channel length of 0.36 $\mu$m. By using this optimal channel length, we can reduce delay and power consumption and therefore obtain maximum performance in subthreshold circuits.

### D. Effect of Supply Voltage on Optimal Channel Length for Maximum Current Per Width

The drive current in the subthreshold region is an exponential function of the supply voltage and threshold voltage. This is not the case in the moderate and strong-inversion regions where the current is governed by different equations. As can be seen in (5), optimal channel length for maximum current per width is independent of supply voltage in the subthreshold region. It is a function only of process parameters. However, in the strong-inversion region, the gain in current obtained by utilizing the RSCE becomes smaller due to the reduced impact of $V_{\text{th}}$ on current and the larger increase in device capacitance. As a result, the minimum channel length becomes the optimal channel length. This can be shown analytically as follows.

Current in strong-inversion can be modeled as

$$I_{D_\text{STRONG}} = K\frac{W}{L_{\text{eff}}}(V_{\text{GS}} - V_{\text{th}})^{\alpha} \tag{10}$$

where $\alpha$ and $K$ are technology parameters, $V_{\text{GS}}$ is the gate-to-source voltage, and $V_{\text{th}}$ is the threshold voltage. Note that $V_{\text{th}}$ is also a function of $L_{\text{eff}}$ [see (1)]. In short-channel devices, $\alpha$ is between 1 and 1.5. Using (1), the derivative of the device current with respect to the channel length can be expressed as

$$\begin{aligned}\frac{\partial I_{D_\text{STRONG}}}{\partial L_{\text{eff}}} &= \frac{\partial\left[K\frac{W}{L_{\text{eff}}}(V_{\text{GS}} - V_{\text{th}})^{\alpha}\right]}{\partial L_{\text{eff}}}\\ &= KW\frac{\frac{d(V_{\text{gs}}-V_{\text{th}})^{\alpha}}{dL_{\text{eff}}}L_{\text{eff}} - (V_{\text{gs}} - V_{\text{th}})^{\alpha}\frac{dL_{\text{eff}}}{dL_{\text{eff}}}}{L_{\text{eff}}^2}\\ &= C_1\left[-\frac{C_2 L_{\text{eff}}}{\sqrt{1 + K_2/L_{\text{eff}}}} - (V_{\text{gs}} - V_{\text{th}})\right]\end{aligned} \tag{11}$$

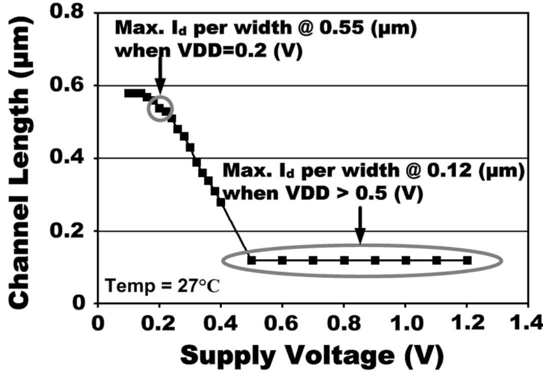


Fig. 7. Effect of supply voltage on the channel length providing maximum current per width.

where $C_1$ and $C_2$ are positive constants. $K_2$ was given in (1) as a positive constant and, since $V_{\rm gs} - V_{\rm th}$ is also positive, the following inequality holds true:

$$\frac{\partial I_{D_{\rm STRONG}}}{\partial L_{\rm eff}} < 0. \tag{12}$$

Therefore, $I_{D_{\rm STRONG}}$ decreases monotonically as the channel length increases for a fixed channel width. Since the SCE was omitted in (1), it is important to note that the above derivation is only applicable for longer channel lengths where RSCE is dominant over SCE. However, it is trivial to show that a shorter channel length gives a higher current for channel lengths where SCE is stronger than RSCE; a lower $\rm Vth$ and a higher $W/L$ ratio at a shorter channel length together increases the device current. Hence, we can conclude that, even with a strong RSCE, the minimum channel length is optimal for maximum current in the superthreshold region.

Fig. 7 shows simulation results on the optimal channel length for different supply voltages. Three different regions can be observed. In the subthreshold and strong-inversion regions, the optimal channel length does not depend strongly on the supply voltage, as was expected from our derivations. Therefore, we can use the optimal channel length obtained from (5) which is independent of supply voltage in the deep subthreshold region. In the moderate-inversion region, however, the optimal channel length varies depending on the supply voltage. For the 0.13-$\mu$m process technology used in this study, the optimal channel lengths in the subthreshold and superthreshold region are 0.55 and 0.12 $\mu$m, respectively.

### E. Impact of Process Variation

Random dopant fluctuation (RDF) causes random parameter mismatches even between devices with identical layout in close proximity. The standard deviation $(\sigma)$ of the threshold voltage distribution caused by RDF is proportional to $(WL)^{-1/2}$. Using the proposed sizing method, the sample gate area for optimal performance increases from 0.24 $\mu$m$^2$ (= 2 $\mu$m $\times$ 0.12 $\mu$m) to 0.35 $\mu$m$^2$ (= 0.98 $\mu$m $\times$ 0.36 $\mu$m) with identical current drivability and reduced device capacitance, as shown in Fig. 6. This interesting characteristic leads to less threshold voltage variations for the proposed sizing scheme. To verify this, statistical studies were carried out using Monte Carlo simulation. Fig. 8 shows the delay and power consumption distribution of a static inverter chain designed using the proposed and conventional scheme. The four-stage inverter chains are simulated at room temperature with the input switching at 100 MHz. A supply voltage of 0.2 V was used. Delays of the third-stage inverters were measured. Power consumption was measured for the cycle time of the inverter chain implemented using the conventional sizing scheme and includes both the active and static leakage power components. The $\sigma/\mu$ ratios of the delay and power consumption distributions are reduced by 37.5% and 70%, respectively, resulting in a squeezed distribution for the proposed sizing scheme. Simulation results show a 13% improvement in average delay while simultaneously achieving a 31% reduction in average power dissipation.

### F. Subthreshold Swing and Ion-to-Ioff Ratio

Subthreshold swing $(S)$ is a critical parameter that determines the relationship between subthreshold current and the gate voltage. It is defined as the amount of $V_{\rm GS}$ required to change the subthreshold current by an order of magnitude. $S$ has generally been considered to be a process-dependent parameter. A small $S$ is preferred in order to achieve higher on-current for a given off-current value. Our proposed sizing scheme utilizes a longer channel length which reduces $S$ and therefore improves the Ion-to-Ioff ratio.

The subthreshold swing can be represented as

$$S = m\frac{kT}{q}\ln 10\ (\text{mV/dec}) \tag{13}$$

where

$$\begin{aligned} m &= 1 + \frac{C_{\rm DEP}}{C_{\rm OX}} \\ C_{\rm ox} &= \frac{\varepsilon_{\rm ox}}{t_{\rm OX}} \\ C_{\rm DEP} &= \frac{\varepsilon_{si}}{W_{\rm DEP}} \end{aligned} \tag{14}$$

and $kT/q$ is the thermal voltage.

As we explained in Section III-C, RSCE increases the depletion width underneath the channel and lowers the depletion capacitance $C_{\rm DEP}$ for long-channel devices. This alters the value of $m$ in (14) and reduces $S$. $I$–$V$ characteristics of a conventional minimum channel device and an optimal longer channel device are shown in Fig. 9. The subthreshold swing of the proposed method is 71 mV/dec, which is 16 mV lower than that of the conventional minimum channel device. The improved subthreshold slope reduces the off-current by 30% for the same on-current.

Improved Ion-to-Ioff ratio can be achieved by the reduced $S$. Ion-to-Ioff ratio is a critical factor in subthreshold digital circuits and subthreshold SRAMs [5]. The inherently small Ion-to-Ioff ratio limits the number of transistors connected per node. Fig. 10 shows the Ion-to-Ioff ratio for the conventional and proposed scheme at different supply voltages. At 0.2 V, the Ion-to-Ioff ratio was 484 for the proposed scheme, which is a 2.5 times improvement over the conventional minimum channel device.

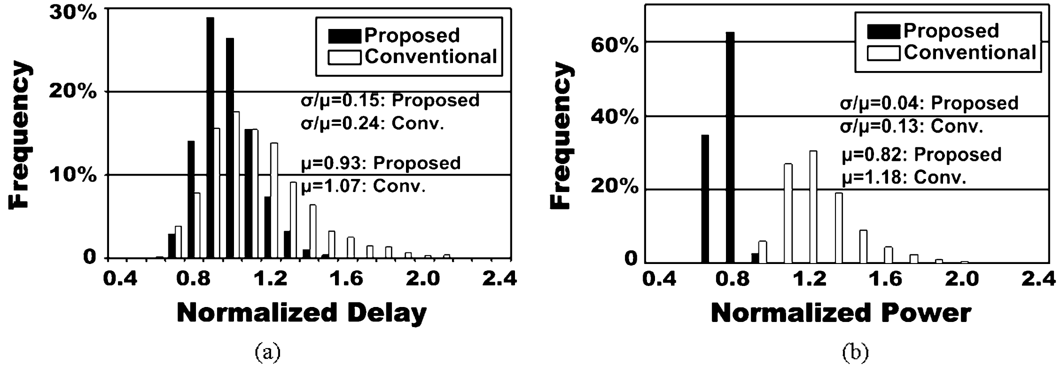


Fig. 8. Statistical comparison of a static inverter chain. (a) Delay distribution. (b) Power consumption distribution.

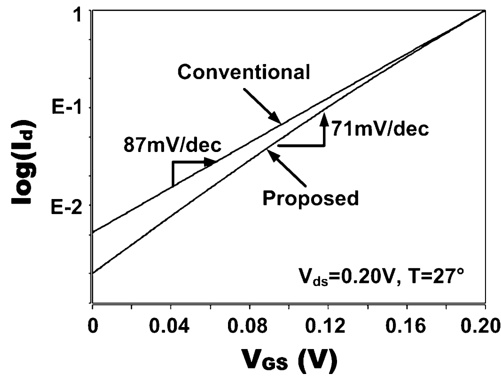


Fig. 9. Subthreshold swing comparison for conventional and proposed sizing scheme.

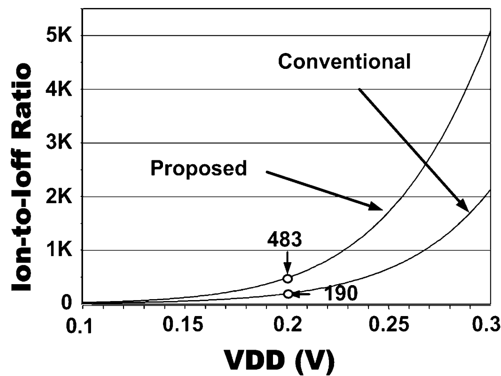


Fig. 10. Ion-to-Ioff ratio as a function of supply voltage.

## G. Improvement in Delay, Power Dissipation, and Energy

The proposed scheme offers a simultaneous improvement in circuit delay and power consumption which leads to a significant reduction in energy dissipation which is the product of delay and power consumption. Energy consumption is a critical metric in applications such as portable devices, medical instruments, and wireless sensor networks where subthreshold circuits can be widely applied. In the superthreshold region, using a larger device for reducing the circuit delay always causes the power consumption to increase due to the increase in gate and junction capacitance. The energy dissipation would increase accordingly. The proposed scheme, on the other hand, reduces the junction capacitance without deteriorating the performance because a smaller device width can be used for the same current drivability. Since we obtain a reduction in both delay and power consumption using the proposed scheme, a large improvement in energy consumption is achieved. Energy consumed in the subthreshold region can be expressed as

$$\begin{aligned} E_{\text{SWITCHING}} &= \alpha \cdot C \cdot \text{VDD}^2 \\ E_{\text{LEAK}} &= \text{VDD} \cdot I_{\text{LEAK}} \cdot t_d \\ &= \beta \cdot \text{VDD} \cdot C e^{\frac{-V_{\text{th}}}{mVt}} \cdot \frac{\text{VDD}}{e^{\frac{\text{VDD}-V_{\text{th}}}{mVt}}} \\ &= \beta \cdot C \cdot \text{VDD}^2 e^{\frac{-\text{VDD}}{mVt}} \\ \therefore E_{\text{TOTAL}} &= E_{\text{SWITCHING}} + E_{\text{LEAK}} \\ &= \alpha \cdot C \cdot \text{VDD}^2 + \beta \cdot C \cdot \text{VDD}^2 \cdot e^{\frac{-\text{VDD}}{mVt}} \quad (15) \end{aligned}$$

where $\alpha$ is the activity factor, $\beta$ is a technology-related constant, $C$ is the switching capacitance, VDD is the supply voltage, $I_{\text{leak}}$ is the leakage current, and $t_d$ is the propagation delay. At a fixed supply voltage, the total energy is a function of device capacitance. The proposed scheme reduces both $C$ and $t_d$ in (15). Simulations using ISCAS benchmark circuits show an energy reduction as large as 41.2%.

## IV. Experimental Results

A delay chain composed of inverters, two-input NANDs and two-input NORs was used in simulations to verify the effectiveness of the proposed sizing scheme. For accurate SPICE simulations, a postlayout netlist was extracted including the *RC* parasitics. The layout of the sample delay chain is shown in Fig. 11. The conventionally sized gates have a taller layout than the gates sized using the proposed scheme. This is due to the fact that "fat" devices in the proposed scheme have longer channel lengths and narrower widths. As mentioned in Section III-B, minimum channel length is used for the pMOS devices since the strength of RSCE was not sufficiently pronounced to provide current gain at a longer channel length for those transistors in this particular technology. In future technology nodes where RSCE is severe in both pMOS and nMOS devices [16], our proposed sizing scheme can be applied in general subthreshold circuit design. The layout area of the proposed scheme is 18% smaller compared with that using

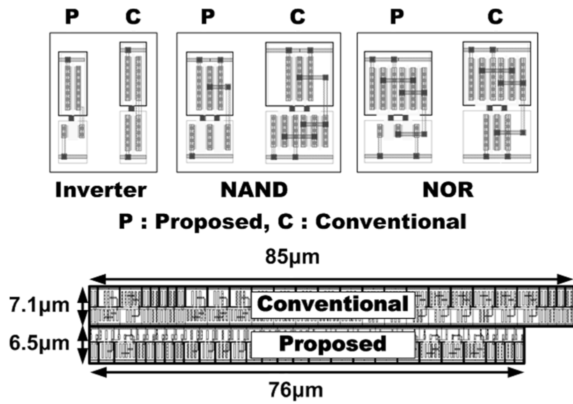


Fig. 11. Layout comparison for basic logic gates and sample delay chain.

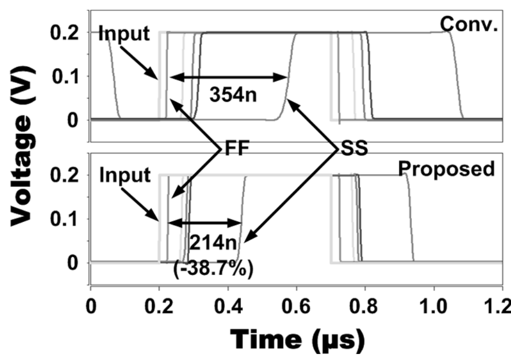


Fig. 12. Simulation waveforms using corner parameters showing improved tolerance to process variation using proposed scheme.

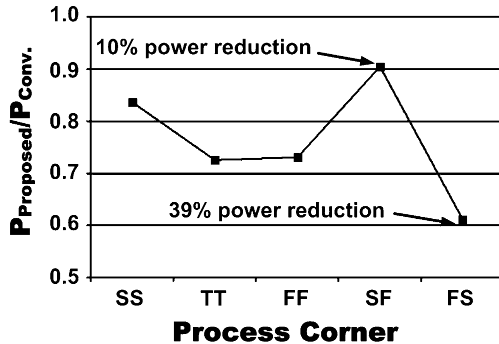


Fig. 13. Comparison of average power for corner parameters.

TABLE I
CRITICAL PATH DELAY COMPARISON FOR ISCAS BENCHMARK CIRCUITS

| CIRCUIT | 0.2V, TEMP = 27C° | | |
|---|---|---|---|
| | Conv. (ns) | Prop.(ns) | Improvement (%) |
| C6288 | 119 | 107 | 10.1 |
| C1355 | 443 | 397 | 10.4 |
| 74283 | 231 | 207 | 10.4 |
| 74L85 | 121 | 110 | 9.1 |
| 74182 | 103 | 95 | 7.8 |

TABLE II
POWER COMPARISON FOR ISCAS BENCHMARK CIRCUITS

| CIRCUIT | 0.2V, TEMP = 27C° | | |
|---|---|---|---|
| | Conv.(μW) | Prop.(μW) | Improvement (%) |
| C6288 | 2.24 | 1.50 | 33.0 |
| C1355 | 0.64 | 0.42 | 34.4 |
| 74283 | 1.60 | 1.38 | 13.8 |
| 74L85 | 0.38 | 0.26 | 31.6 |
| 74182 | 0.40 | 0.38 | 8.4 |

TABLE III
POWER COMPARISON FOR ISCAS BENCHMARK CIRCUITS

| CIRCUIT | 0.2V, TEMP = 27C° | | |
|---|---|---|---|
| | Conv. (μW nS) | Prop. (μW nS) | Improvement (%) |
| C6288 | 266.56 | 160.50 | 39.8 |
| C1355 | 283.52 | 166.74 | 41.2 |
| 74283 | 369.60 | 285.66 | 22.7 |
| 74L85 | 45.98 | 28.60 | 37.8 |
| 74182 | 41.20 | 36.10 | 12.4 |

conventional sizing in this delay chain. Fig. 12 shows simulated waveforms of the simple logic chain using corner parameters. It can be seen that the delay variation of the proposed scheme is 38.7% smaller than that of the conventional method. The reduction in power dissipation is shown in Fig. 13 for each process corner. The power savings range from 10% to 39%, mainly depending on the current of the conventional scheme which is sensitive to process variations.

We tested our sizing method in more general logic paths by synthesizing a number of ISCAS benchmark circuits, as well as different component circuits used in that suite. Two cell libraries were created; a conventional library optimized for superthreshold operation and a new library based on our proposed sizing scheme. Each library contains inverters, two-input NANDs, and two-input NORs. Digital logic gates in the conventional library use the minimum channel length of 0.12 $\mu$m in this process technology. The proposed library uses the optimized channel length of 0.36 $\mu$m for nMOS devices and 0.12 $\mu$m for pMOS devices. Critical path delays, power consumption, and energy consumption obtained from HSPICE simulations are compared in Tables I–III. Increasing the number of switching internal nodes and activity rate will result in more dynamic power savings compared with the leakage power savings. In this simulation, internal nodes which are connected to the switching input signal contribute dynamic power savings and the static nodes contribute to leakage saving. Improvements in delay range from 7.8% to 10.4% depending on the type of logics used in the critical path. In addition, a simultaneous power reduction of 8.4% to 34.4% is achieved with the proposed scheme. As a result, reductions of energy ranging from 12.4% to 41.2% are obtained. Finally, the effect of activity rate on power savings is shown in Fig. 14 for the four-stage inverter chains used in Section III-E. The proposed sizing scheme reduces the leakage power and dynamic power simultaneously. Leakage power reduction from the improved subthreshold slope is larger than the dynamic power reduction. Therefore, as the activity rate decreases, the power savings improves and

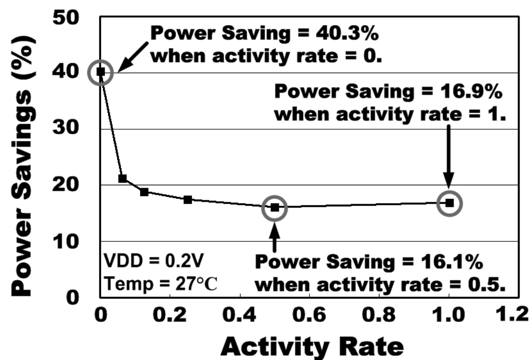


Fig. 14. Effect of activity rate on power savings in the four-stage inverter chain used in Section III-E.

converges to the leakage power savings, as can be seen in Fig. 14.

## V. Conclusion

As process technologies are scaled down, RSCE becomes stronger due to the increased HALO doping. RSCE is not a major concern in superthreshold designs since it does not affect the electrostatics of minimum channel length devices which are optimal for high performance and low power. Rather, DIBL and $V_{\rm th}$ roll-off were the main considerations for minimum channel length devices. However, in the subthreshold region, where DIBL is reduced and current depends exponentially on threshold voltage, RSCE must be considered for optimal device sizing. In this study, we show that using minimum channel length is not optimal for subthreshold circuits in the process technologies where strong RSCE effect can be observed. We propose a novel device-size optimization scheme which can achieve high drive current, low device capacitance, and high Ion-to-Ioff ratio by utilizing the RSCE. Circuits using the proposed sizing scheme are more robust against RDF because of the increased gate area at the optimal performance point. The proposed sizing scheme reduces delay and power dissipation simultaneously, which is not possible using conventional sizing schemes. As a result, a significant improvement in energy is obtained. Average delay in ISCAS benchmark circuits was improved by 13% while average power dissipation and energy dissipation were reduced by 31% and 40%, respectively. The proposed scheme also offers a tighter delay and power consumption distribution by improving the $\sigma/\mu$ ratios by 37.5% and 70%, respectively.

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