Sleep Transistor Sizing and Control for Resonant Supply Noise Damping

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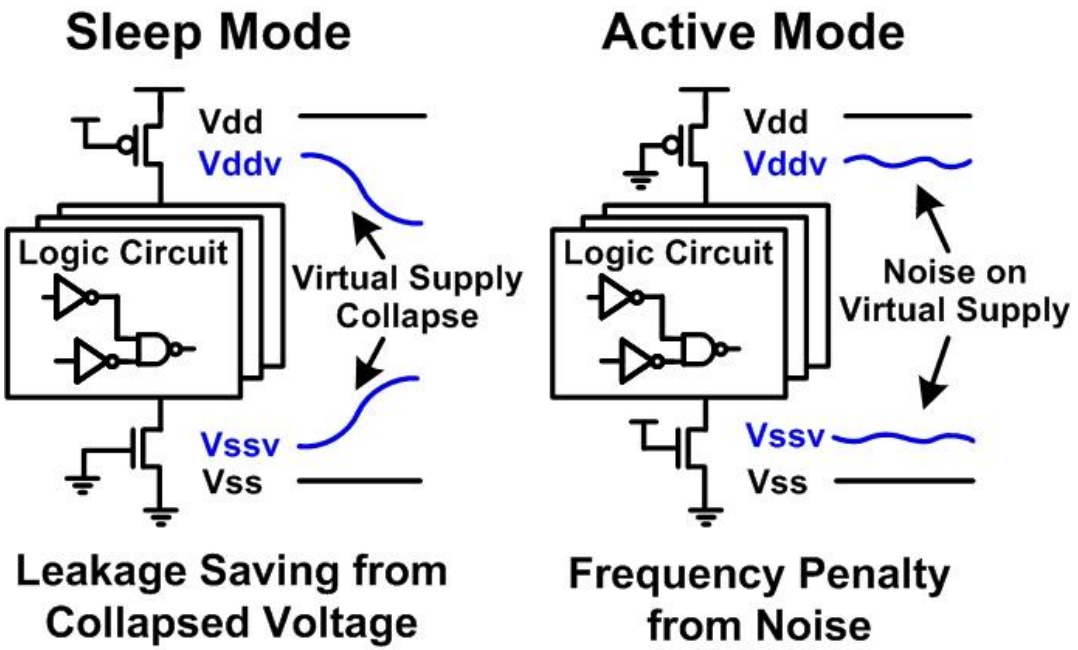
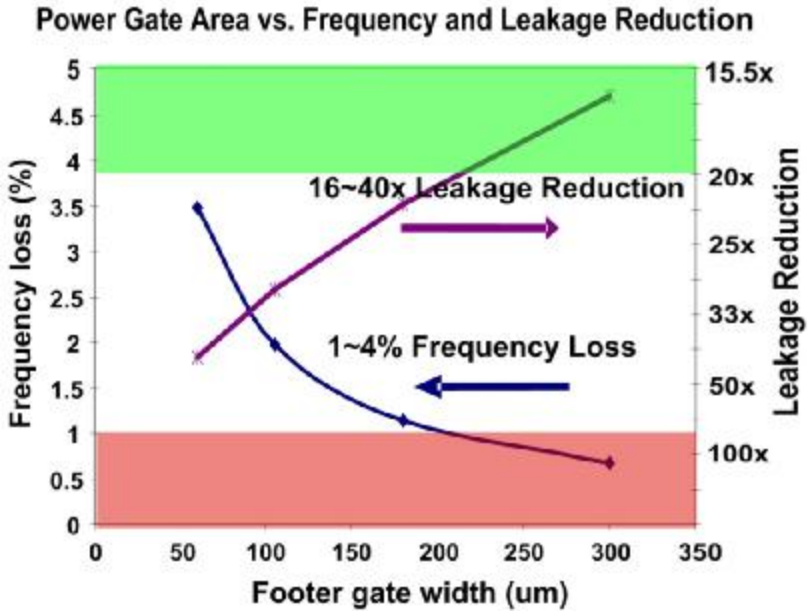
Outline

- Introduction
- Conventional Sizing of Sleep Transistors
- Sleep Transistor Sizing Considering Resonant Supply Damping
- Adaptive Sleep Transistor Circuit
- Conclusions

Sleep Transistor Sizing

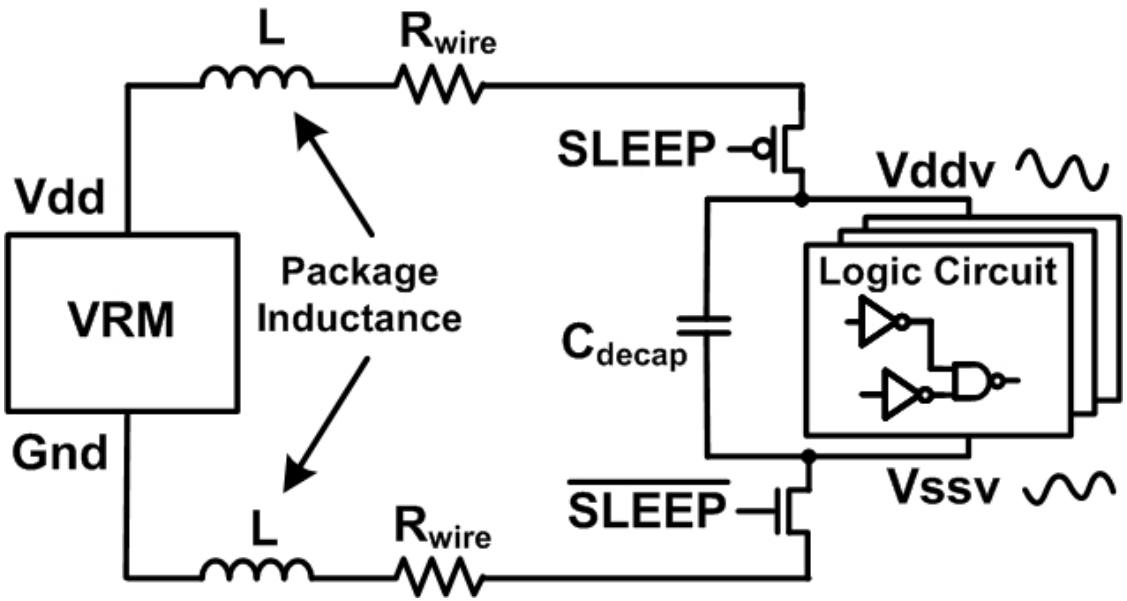


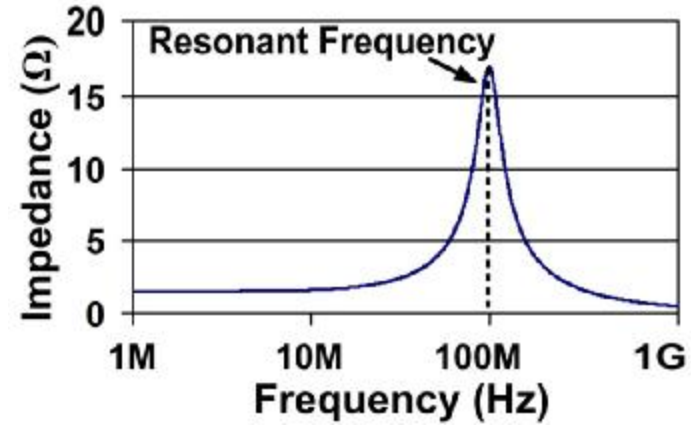


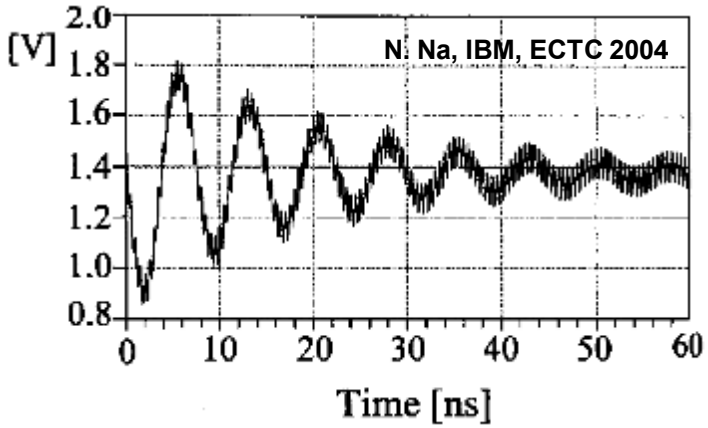
R. Puri, et al., IBM, DAC 2005

- Tradeoff between performance, leakage and area
- Conventional wisdom: use larger sleep transistors to improve performance
- Considers only IR droop
- Ignores the Ldi/dt noise, especially resonant supply noise

Resonant Noise of Supply Network



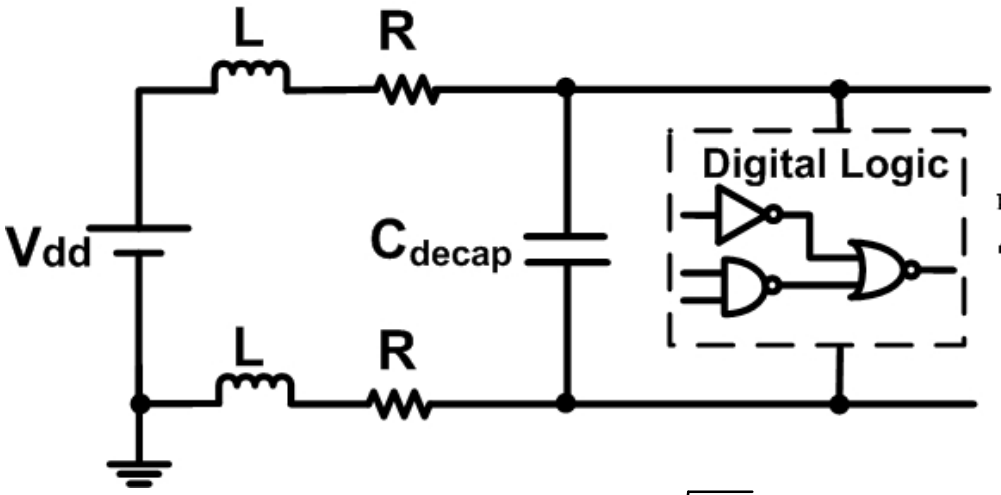




- Resonant noise has largest magnitude and longest duration
- Causes severe timing violation and reliability issues
- Excited by μP loop operation or large current transient

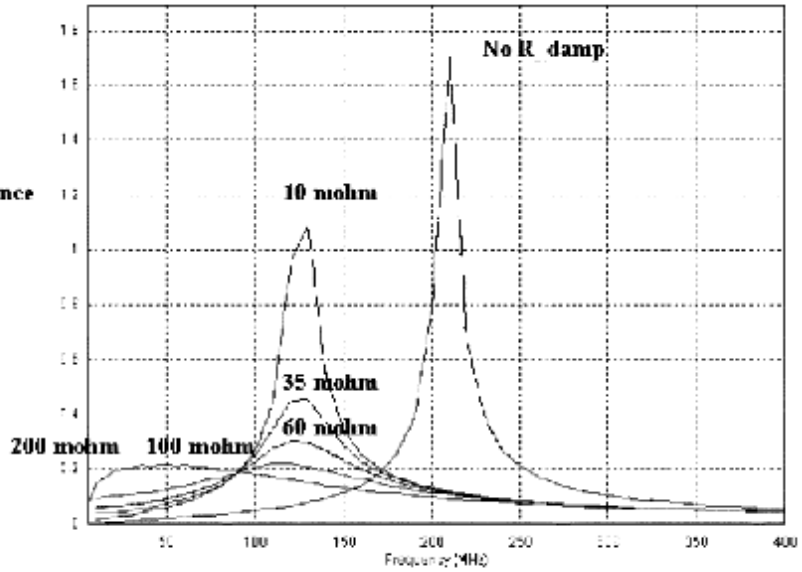
Passive Suppression of Resonance

Add on-chip decap



$$Q = \frac{1}{R_{wire}} \bullet \sqrt{\frac{L}{C}}$$

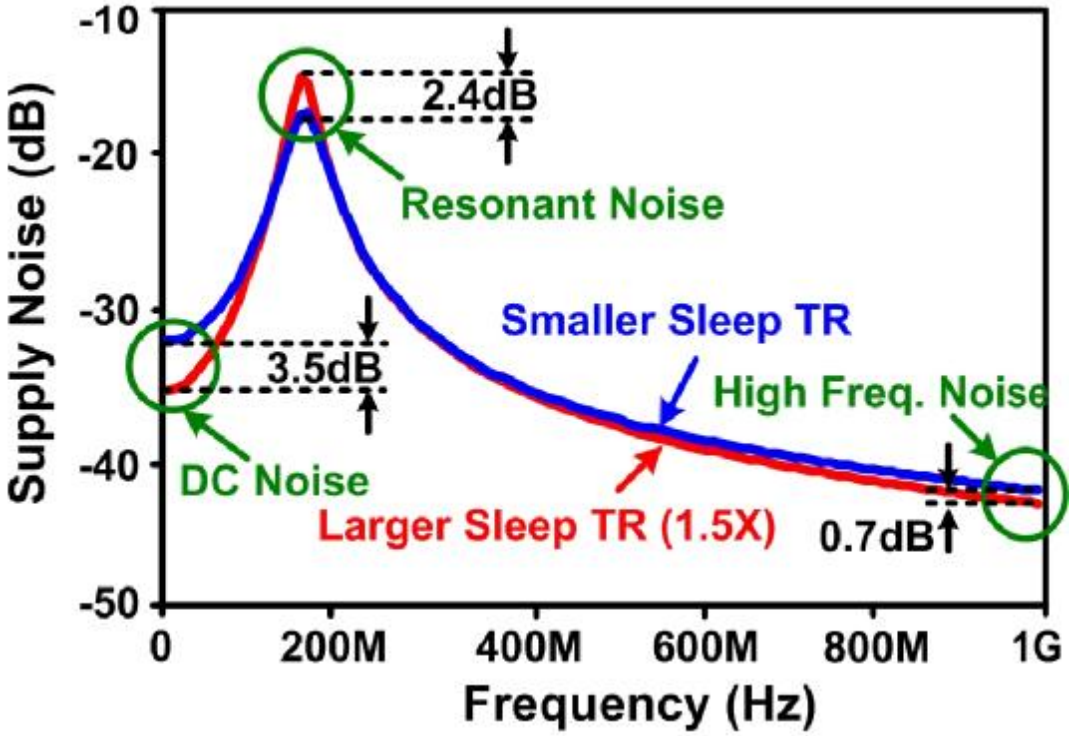
Add on-chip resistance



G. Ji, et al., Intel, T. Adv. Packaging, 2005

- Decap consumes large leakage and area
- Adding resistors results in extra IR droop and power
- Damping effect of sleep transistors is not considered

Sleep TR Sizing Considering Resonance

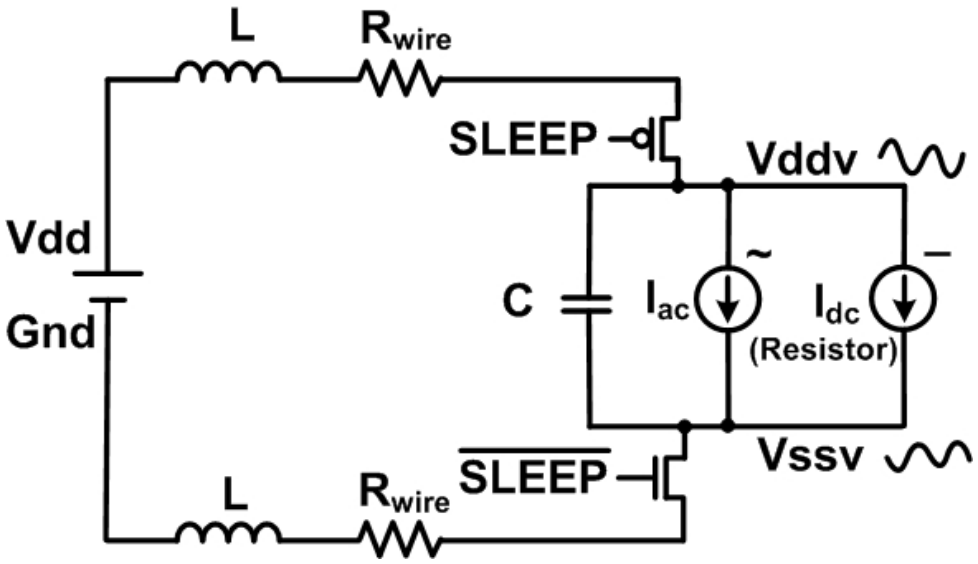


- **Conventional Sizing: DC Noise**
- **Proposed Sizing: DC Noise + Resonance**
- **Sizing has little impact on high freq noise**

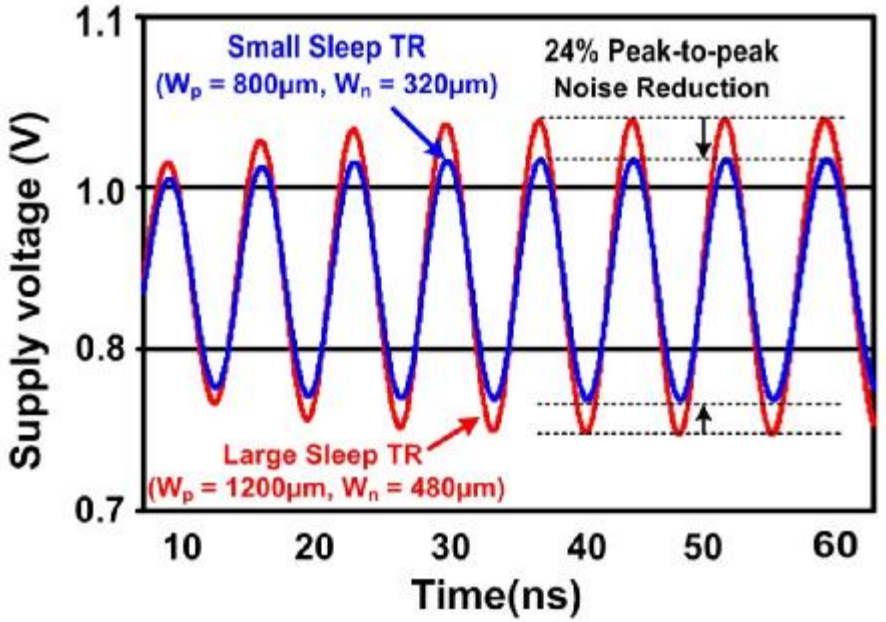
$$Z(\omega) = (R_{wire\&sleep\_tr} + \omega L) // (\frac{1}{\omega C})$$

Dominant in DC and Middle Freq **Dominant in High Freq**

Simulation Setup and Waveforms

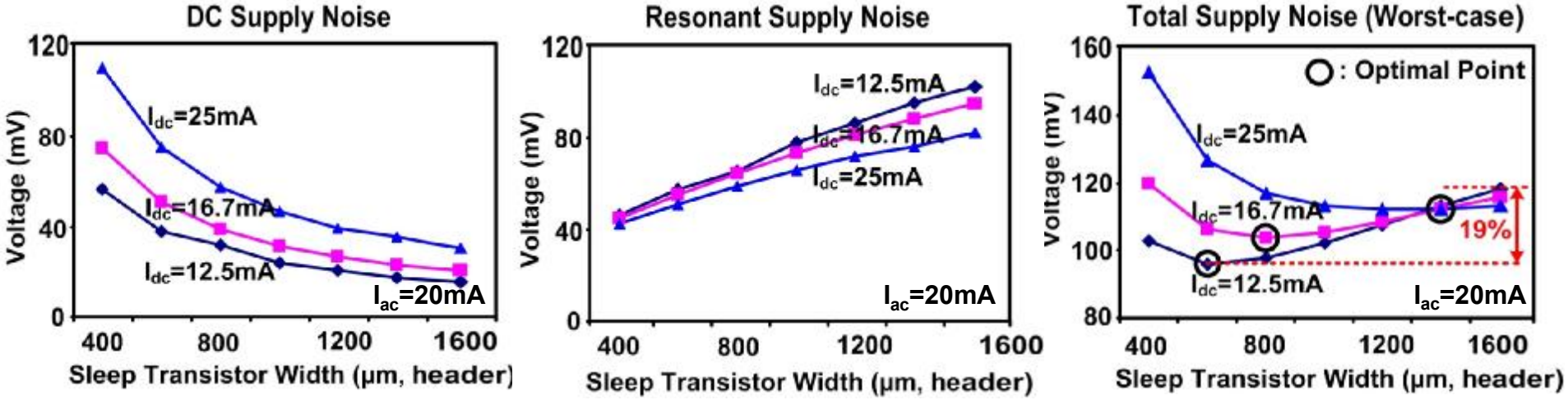


PTM 32nm CMOS, 0.9V



- Resistor used to generate DC noise
- Ideal current source used to generate AC noise
- 33% smaller sleep TR helps damp resonant noise by 24%

Sizing Results for Both DC and Resonant Noise

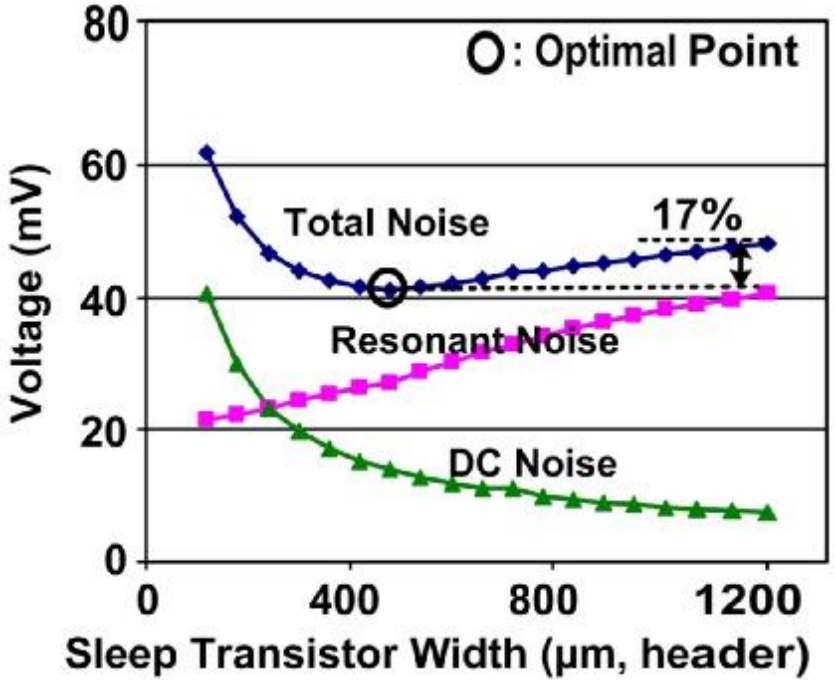


$$V_{total\_noise} = V_{dc\_noise} + V_{ac\_noise} = I_{dc} \cdot R_{sleep\_tr} + I_{ac} \cdot \frac{L}{R_{sleep\_tr} \cdot C} \xrightarrow{\textit{Minimum Noise}} R_{sleep\_tr} = \sqrt{\frac{I_{ac}}{I_{dc}} \cdot \frac{L}{C}}$$

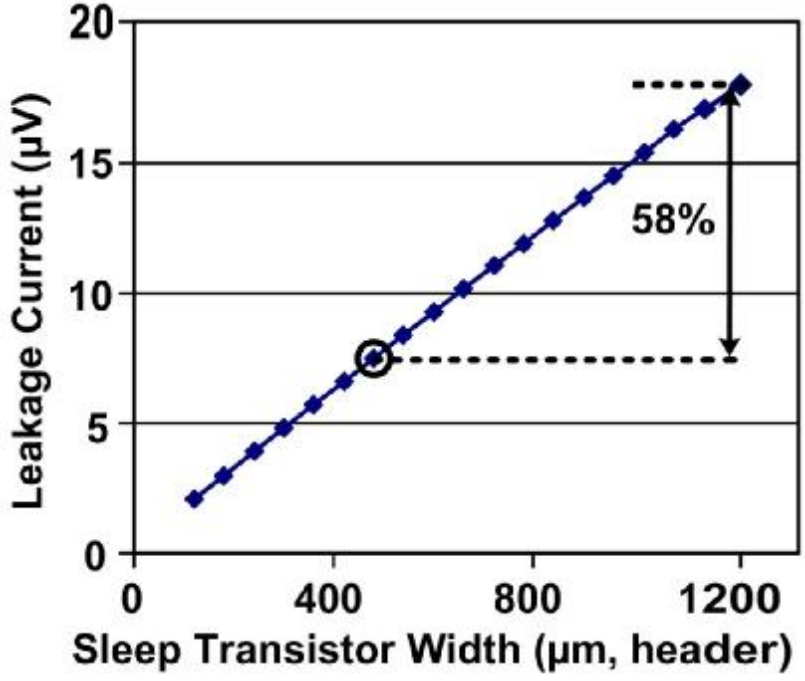
- Largest size is no longer optimal for minimum noise
- Proposed optimal sizing leads to
  - 19% less worst-case noise
  - 69% less area overhead
- Optimal point depends on the ratio of DC and AC current

Test on Benchmark Circuit

Noise in Active Mode

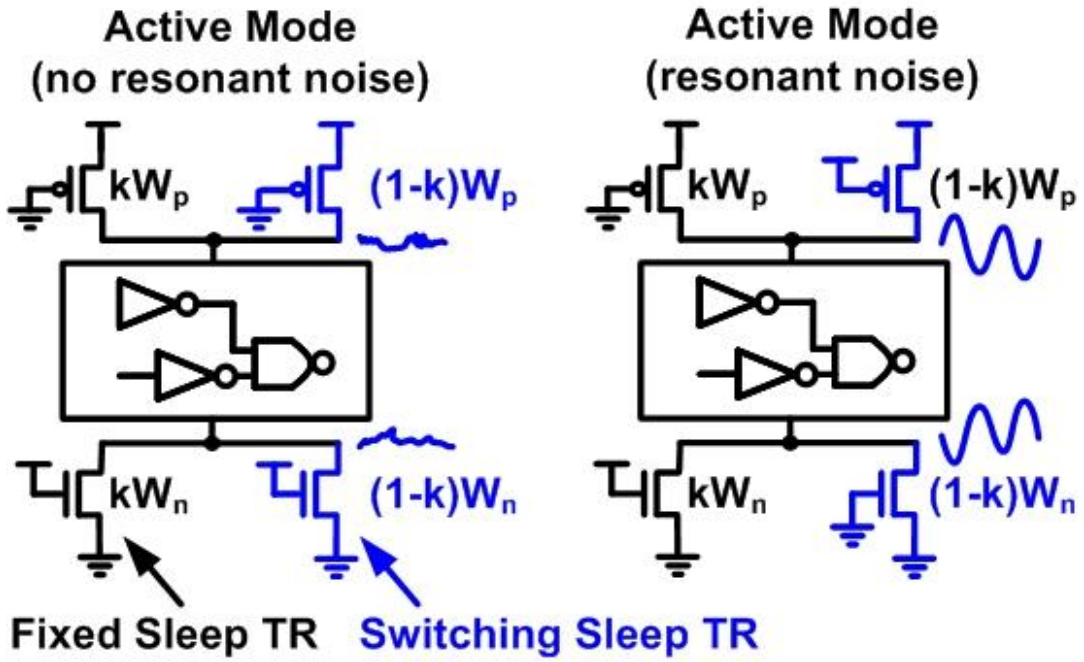


Leakage in Sleep Mode



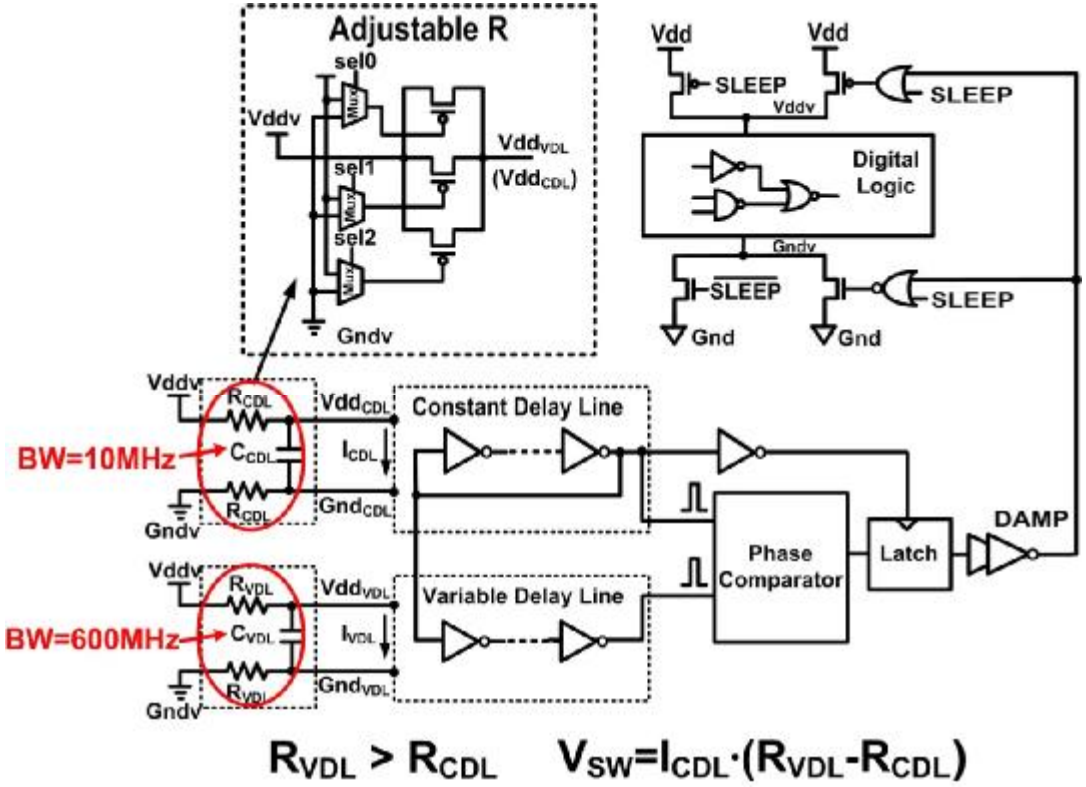
- 30 x 8-bit ALU (C880, ISCAS85, 383 gates) at 100MHz
- Proposed optimal sizing leads to
  - 17% less worst-case noise
  - 58% less leakage in sleep mode
  - 60% smaller area overhead

Adaptive Sleep Transistors

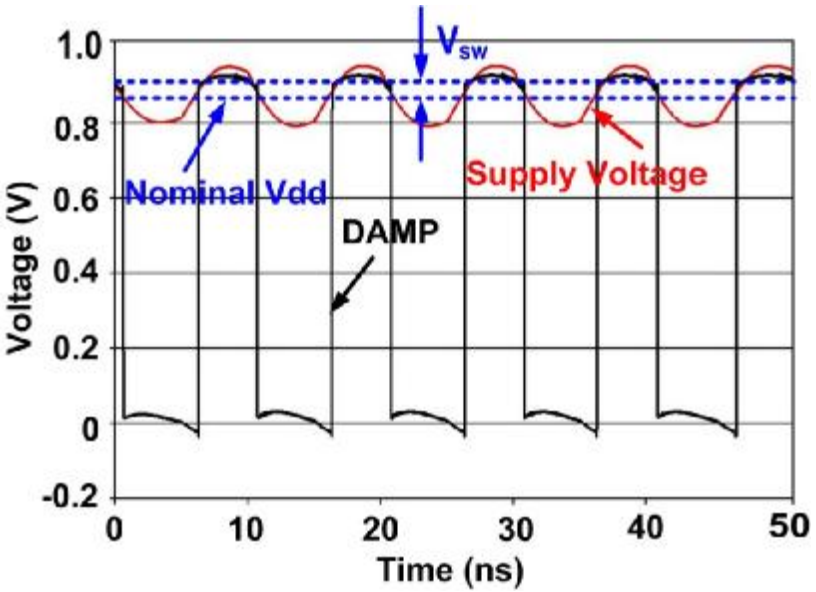


- **Fixed Sizing**
  - **Sacrifices DC supply noise**
  - **May lose the average performance if resonant noise is sporadic**
- **Adaptive Sizing**
  - **Reduces size only when resonance is detected**
  - **Minimizes both DC and resonant supply noise**

Digital Resonant Detection for Adaptive Sizing

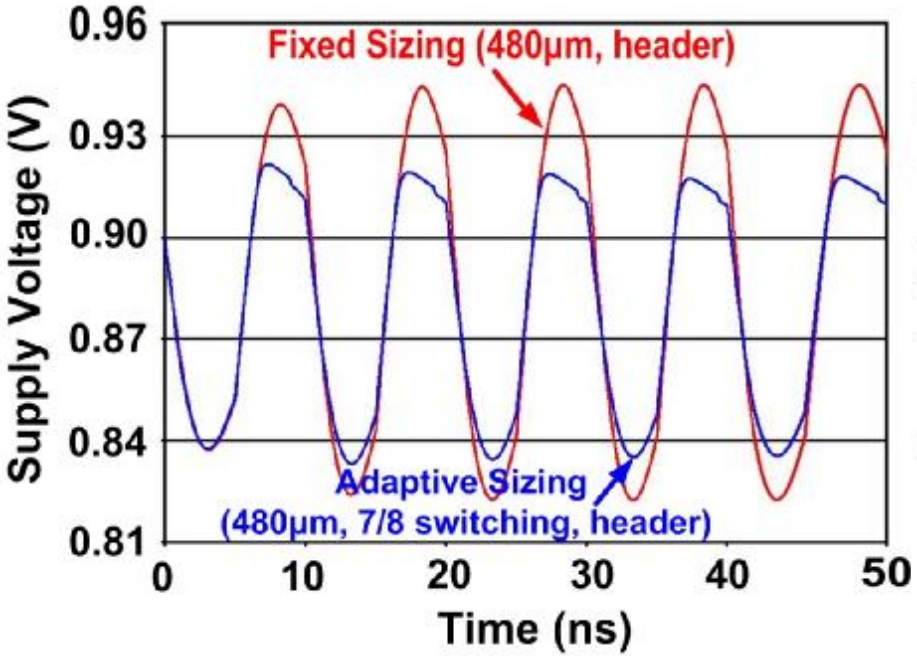


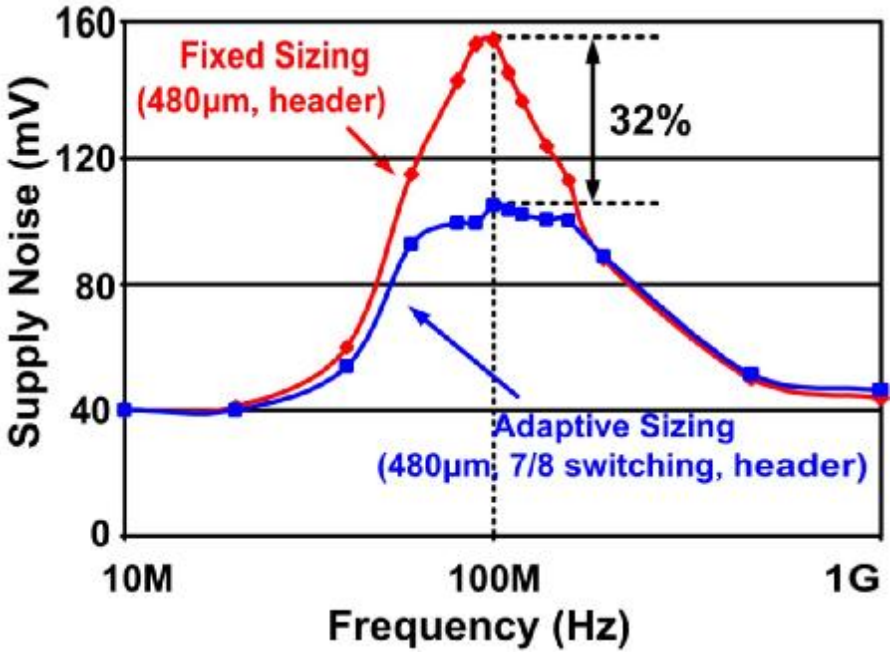
$R_{VDL} > R_{CDL}$ $V_{SW}=I_{CDL}\cdot(R_{VDL}-R_{CDL})$



- Noise detection BW: 10MHz~600MHz, over power: 0.36mW
- Responds to supply overshoot only to avoid IR droop
- Adjustable switching threshold V_{SW}

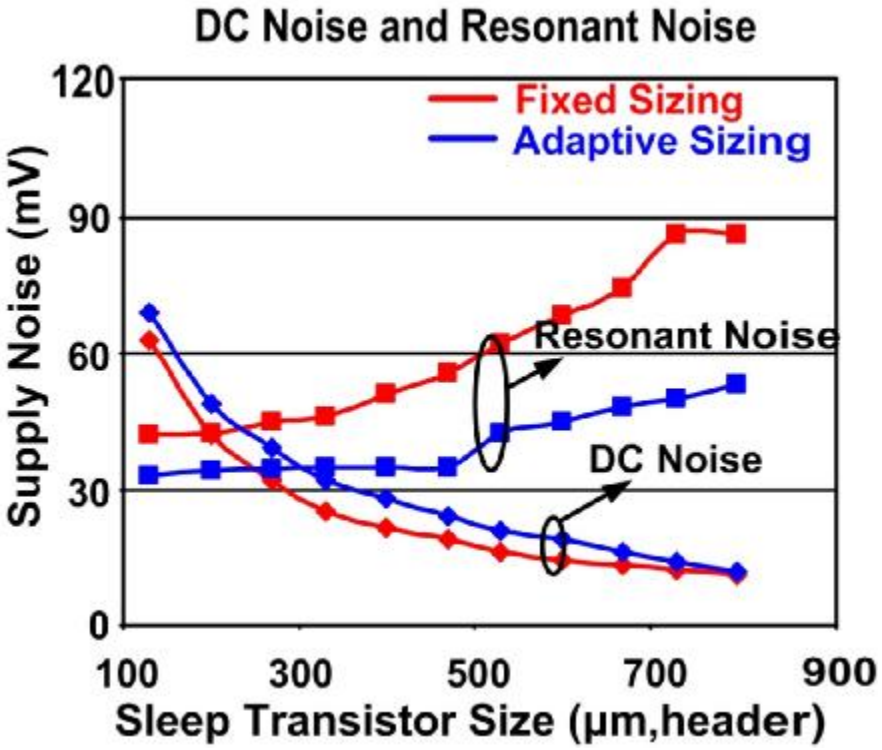
Noise Reduction by Adaptive Sizing

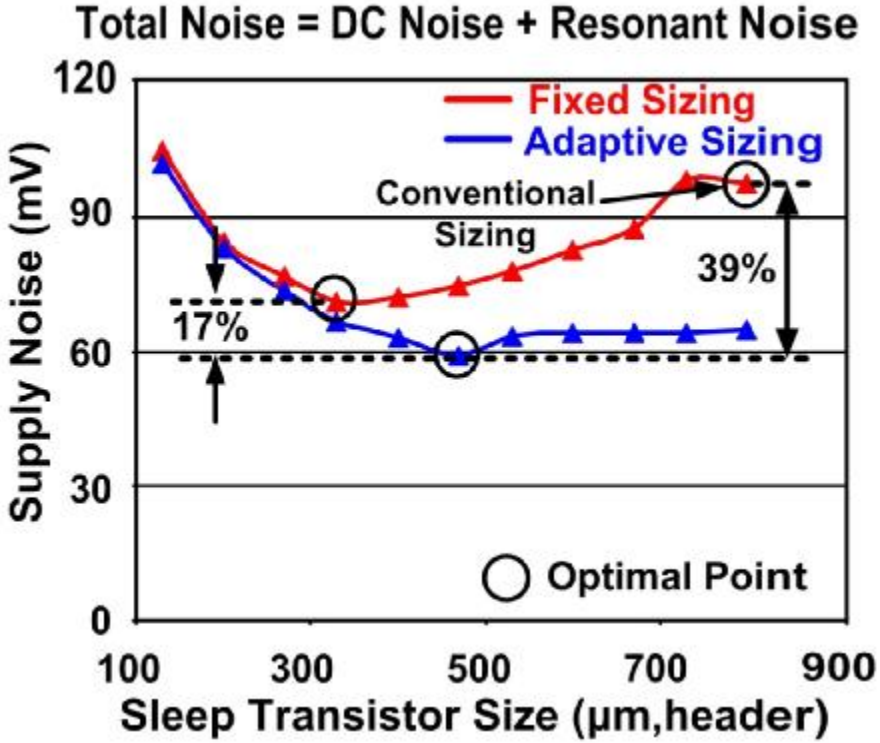




- Suppression in both undershoot and overshoot
- 32% resonant noise reduction
- No increase in DC noise when resonant noise is absent

Noise Reduction by Adaptive Sizing





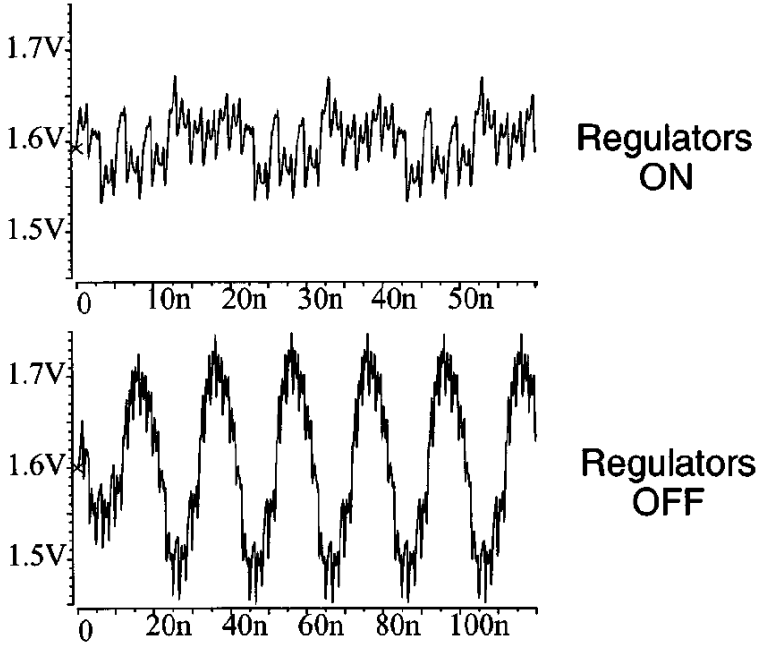
- 17% noise reduction from adaptive sizing over fixed sizing
- 39% reduction over conventional sizing
- Design overhead is offset by decap saving (20%)

Conclusions

- Conventional sleep TR sizing does not consider the resonant noise which represents the worst-case noise
- This work proposes a sizing scheme considering both DC IR noise and resonant supply noise with:
  - 19% less worst-case supply noise
  - 42% leakage reduction
  - 69% smaller sleep transistor overhead
- An adaptive sleep transistor circuit is proposed:
  - Removes DC noise penalty of fixed sizing with sporadic resonant noise
  - Leads to 32% less resonant noise
  - Achieves 17% less worst-case supply noise compared to fixed sizing

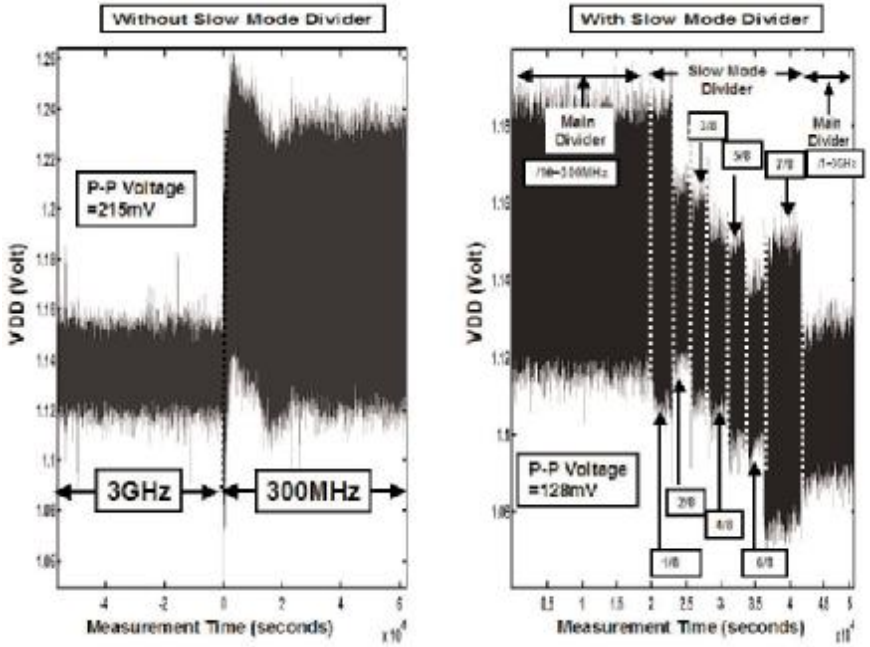
Resonance Suppression by Circuits

Switched decap regulator



R. Heald et al., Sun Microsystem, JSSC 2000

Clock frequency ramping



E. Hailu et al., IBM, ISSCC 2006

- **Circuits techniques are costly in terms of power (i.e. 0.5A for switched decap regulator), die area, and design complexity**
- **Sleep transistor for damping has not been considered**