Sleep Transistor Sizing and Control for Resonant Supply Noise Damping

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ABSTRACT
A fact that has generally been unnoticed is that sleep transistors for leakage reduction can significantly damp the resonant supply noise due to their series resistance. This paper describes an optimal sleep transistor sizing method considering the dominant resonant supply noise. We show that a smaller sleep transistor can offer a smaller worst case supply noise due to the increased damping. We also propose an adaptive sleep transistor technique which automatically dampens the resonant noise only when it is detected. Simulations in 32nm CMOS show that the resonant noise is reduced by 32% using the proposed technique.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles - *Microprocessors and microcomputers; VLSI (very large scale integration)*

General Terms
Management, Performance, Design,

Keywords
Resonant supply noise, sleep transistor, damping

I. INTRODUCTION

Leakage power has become a major issue due to the exponential increase of subthreshold and gate leakage current with aggressive CMOS technology scaling. Many circuit level solutions have been proposed so far to address this issue. One of the most widely used methods for reducing leakage current in VLSI systems is the power gating techniques. Power gating is realized by sleep transistors which disconnect the power supply from the circuit when the chip is in idle mode [1]. The optimal sizing of sleep transistors is targeted at meeting a number of opposing requirements such as minimizing the performance penalty, reducing the standby leakage current, and minimizing the area overhead.

Power supply noise has become a major design concern in recent years. The current density and current swing increases with scaling while the power supply impedance does not scale as desired. Excessive power supply noise causes timing violations, reliability issues, and self-heating problems. The supply network typically has an impedance peak in the 10s to a couple of 100s of MHz range due the LC tank formed by the bonding/package inductance and the on-chip capacitance [2, 3]. Sub-harmonics of the clock frequency can generate current components in the high impedance band exiting the resonance. Another situation where a large resonance can be excited is when sudden current transients are triggered by the clock or control signals. These resonant noise issues were traditionally addressed by adding large on-chip decoupling capacitors (decap) to lower the ac impedance over a wide range of frequencies [4]. However, the MOS capacitors made of thin-oxide devices dissipate large levels of gate tunneling leakage in scaled technologies. Passive resistors have also been added between the Vdd and Gnd to damp the supply resonance at the cost of static current dissipation and IR-drop [5, 6].

The fact that sleep transistors can add considerable amount of series resistance to the supply network and that this can lead to significant damping of the resonant supply noise has generally gone unnoticed. Prior sleep transistor sizing methods focus only on the IR-drop and ignore the fact that the worst case supply noise is caused by the resonant component. Damping effect of sleep transistors has not been investigated or exploited fully even though it is critical to the power supply integrity. In this paper, we show that opposed to conventional wisdom, a smaller sleep transistor can result in a lesser worst case supply noise. Sleep transistor sizing guidelines are given considering the resonance damping effect. We also propose an adaptive sleep transistor technique where the effective sleep transistor width is varied on-the-fly to damp the resonance noise only when it is detected. By doing so, the IR-drop penalty of the sleep transistor can be eliminated when the resonance noise is not excited.

The remainder of this paper is organized as follows. Section II explains the conventional sleep transistor sizing method. The resonance damping effect of sleep transistors is shown in section III. An adaptive sleep transistor circuit that can reduce the resonant noise without sacrificing the IR noise is presented in section IV. Finally, conclusions are drawn in section V. Simulations throughout this paper are based on a 32nm Predictive Technology Model (PTM) with a nominal supply voltage of 0.9V [7].

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II. CONVENTIONAL SLEEP TRANSISTOR SIZING

In active mode, the sleep transistor operates in the linear region and the current through an NMOS sleep transistor can be expressed as

$$I_{circuit} \approx \mu_{eff} C_{ox} \left(\frac{W}{L}\right)_{sleep} (V_{dd} - V_t) V_{VGND} \qquad (1)$$

where μ_{eff} is the carrier mobility, C_{ox} is the oxide capacitance, V_t is the threshold voltage, and V_{VGND} is the virtual ground voltage. From (1), the sleep transistor sizing relates to the circuit current and virtual ground voltage as

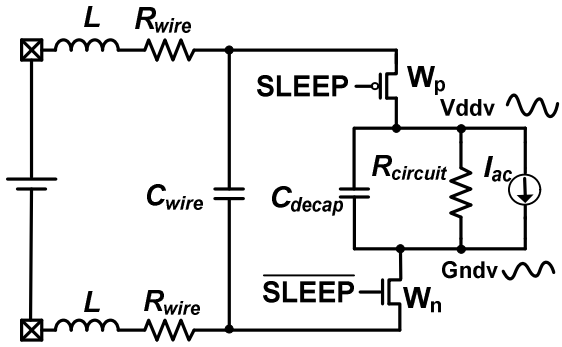
$$\left(\frac{W}{L}\right)_{sleep} \propto \left(\frac{I_{circuit}}{V_{VGND}}\right) \qquad (2)$$

According to equation (2), a larger sleep transistor reduces the V_{VGND} offset for a given current consumption which in turn reduces the performance penalty caused by the sleep transistors. Given the worst case V_{VGND} specification and circuit current consumption, the sleep transistor size can be determined based on (1) and (2) [8, 9]. Conventional sleep transistor sizing methods suggest that the virtual rail drop/rise can be reduced indefinitely by increasing the size of sleep transistor. In this case, the sizing is only limited by the area overhead of the sleep transistors. However, a fact that has been typically overlooked in sleep transistor optimization is that the worst case supply noise is caused by the resonance formed between the bonding/package inductance and the on-chip capacitance. Since sleep transistors act as damping resistors between the circuit and the supply network, the resonant supply noise in the virtual supply rails actually worsens with a larger sleep transistor due to the reduced damping effect. This observation gives the opportunity for a smaller sleep transistor to reduce the total supply noise on the virtual rails. In order to minimize the supply noise in systems with sleep transistors, it is important to consider the resonant damping effect of sleep transistors as well as the IR supply drop.

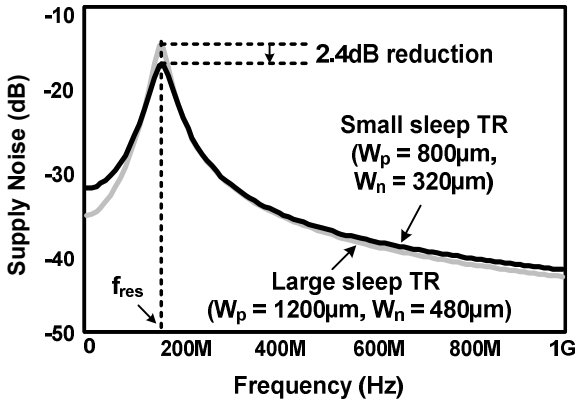
III. SLEEP TRANSISTOR SIZING AND RESONANCE SUPPLY NOISE

In order to study the resonance damping effect of sleep transistors, a simplified model of a power supply mesh is presented in Fig. 1(a). Here, L is the bonding/package inductance, C_{wire} is the supply network capacitance, R_{wire} is the supply network resistance, C_{decap} is the circuit capacitance, and $R_{circuit}$ is the equivalent circuit resistance. The resistance $R_{circuit}$ in the power-supply model comes from the active and leakage currents of the circuit itself which help damp the resonant noise. Further details on damping effect induced by active and leakage currents can be found in [10].

The finite resistance of the PMOS and NMOS sleep transistors provides resonant noise damping that can reduce the total supply noise. Fig. 1(b) shows the frequency response of the power supply noise for two different sleep transistor widths; i.e. header/footer dimensions of 1200µm/480µm and 800µm/320µm. The parameters used for the supply noise simulations are listed in Table 1. The smaller sleep transistor (800µm/320µm) reduces the resonant noise peak by 2.4dB compared to the large sleep transistor (1200µm/480µm) owing to the additional damping provided by the increased resistance. The DC and high frequency noise on the other hand increases due to the larger IR-drop. Typical supply networks are under-damped so once excited, the resonant noise is dominant compared to the IR-drop component. It is possible in these cases for a smaller sleep transistor to result in a smaller supply noise. Decreasing the sleep transistor size to reduce the worst case supply noise can offer additional benefits such as reduced area overhead and smaller standby leakage current. Fig. 2 shows the transient waveforms of the resonant supply noise for the two different sleep transistor sizes. The supply voltage shown in the figure is the differential voltage between the Vddv and Gndv in Fig. 1(a). The peak-to-peak supply noise reduces by 24% using the smaller sleep transistor (800µm/320µm).



(a)



(b)

Fig. 1. (a) Power supply network model of a system with sleep transistors; (b) Frequency spectrum of supply noise for two different sleep transistor widths.

Table 1. Simulation parameters for the supply network model in Fig. 1(a)

Technology	32 nm CMOS	C_{decap}	158pF
C_{wire}	100pF	R_{wire}	0.05Ω

$R_{circuit}$	200Ω	L	2nH
f_{res}	155MHz	I_{ac}	20mA (peak to peak)

The optimal sleep transistor width for minimizing the worst case supply noise depends on the ratio between the resonant noise and the DC noise components. Decreasing the sleep transistor size will be more effective in reducing supply noise when the DC noise is small compared to the resonant noise. This trend is shown in Fig. 3 for different $R_{circuit}$ values. The total power supply noise in the Fig. 3 represents the worst case undershoot which roughly corresponds to the DC noise plus half the peak-to-peak resonant noise. A circuit with higher DC current component is modeled using a smaller $R_{circuit}$. Fig. 3(a) shows that the optimal sleep transistor width increases as the $R_{circuit}$ decreases. This is due to two reasons. First, the DC noise is larger for a smaller $R_{circuit}$ (Fig. 3(b)) making a larger sleep transistor more efficient in reducing this noise component. Second, a smaller $R_{circuit}$ provides additional damping to the resonant noise inherently suppressing the resonant noise peak and depreciating the damping effect of a smaller sleep transistor.

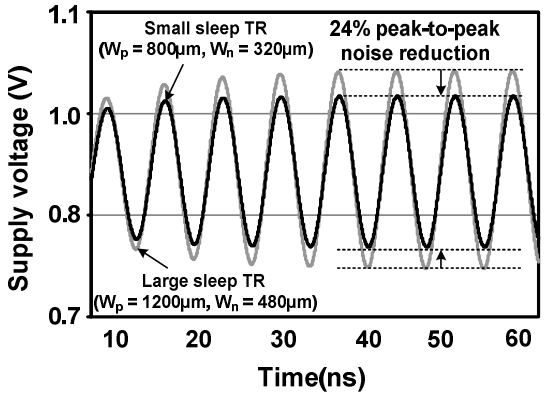


Fig. 2. Simulated supply resonance noise damped by different width sleep transistors.

Smaller sleep transistors for damping the resonant noise in active mode can also provide better leakage reduction in standby mode as the virtual rails will collapse more with the weaker sleep transistors. Fig. 4 shows the standby leakage current as a function of sleep transistor width. In this simulation, $R_{circuit}$ in the previous power supply model is replaced with CMOS digital gates to produce realistic leakage current. Using the 50% smaller sleep transistor (800µm/320µm) which gives a stronger damping effect, 32.3% less standby leakage current can also be achieved. In addition to the reduced standby leakage power, a smaller sleep transistor size also reduces the area overhead.

We have shown in this section that a smaller sleep transistor can minimize the worst case supply noise when the resonant noise is dominant. However, the resonant noise is sporadic in nature and occurs only when there is a current component near the resonant frequency. This means that during periods when resonant noise is not occurring, a larger sleep transistor is preferred for reducing the IR supply noise and improving overall system performance. An adaptive sleep transistor scheme that increases damping only when a resonance is detected can eliminate the IR-drop penalty during non-resonance periods. This scheme can be beneficial for DVS systems where the clock frequency is automatically adjusted based on the actual circuit delay (e.g. Intel's Foxton technology [11]). Such systems are capable of tracking the actual circuit performance using critical path monitors to deliver the highest overall performance for a given power budget. Section IV presents circuit techniques for adaptively controlling the sleep transistor strength using resonant noise sensors.

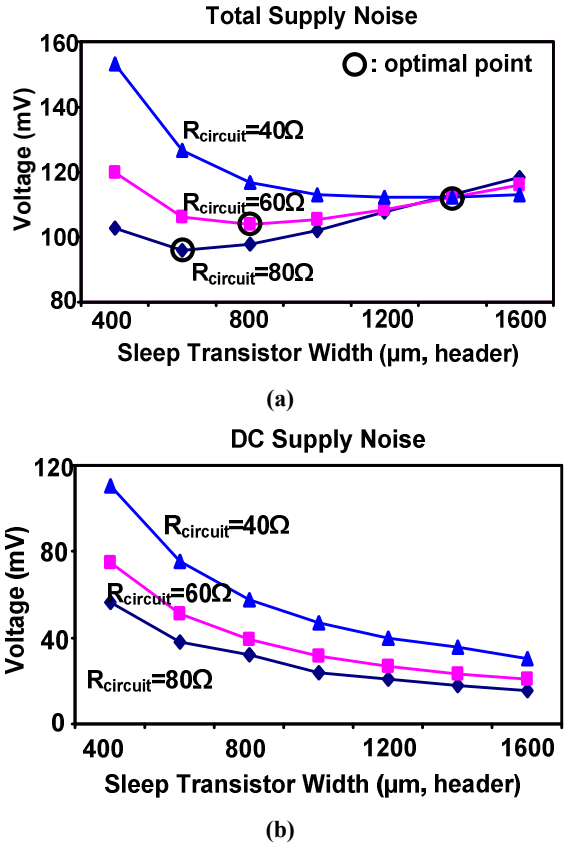


Fig. 3. Simulated power supply noise as a function of sleep transistor size (a) Total power supply noise; (b) DC power supply noise.

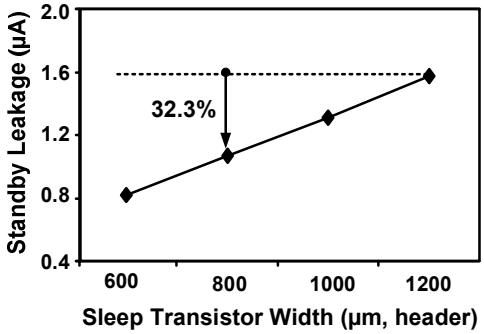


Fig. 4. Standby leakage current versus sleep transistor width.

IV. ADAPTIVE SLEEP TRANSISTORS FOR RESONANT DAMPING

A. Adaptive Sleep Transistor Technique

The objective of this approach is to increase the damping only when a resonance is detected and maintain a small IR-drop at times when there is no resonant noise. Fig. 5 illustrates the concept of the adaptive sleep transistor control scheme. Here, the total width of the sleep transistors (i.e. W_n, W_p) is determined based on the worst case IR-drop following the conventional sizing method. The effective size of the sleep transistor is reduced to kW_n and kW_p when a resonance noise is detected. Here, k is the fraction of the total sleep transistor that is static. Using the proposed scheme, the circuit performance does not need to be sacrificed during periods without any resonant noise. During standby mode, all sleep transistors are turned off to cut off the leakage current.

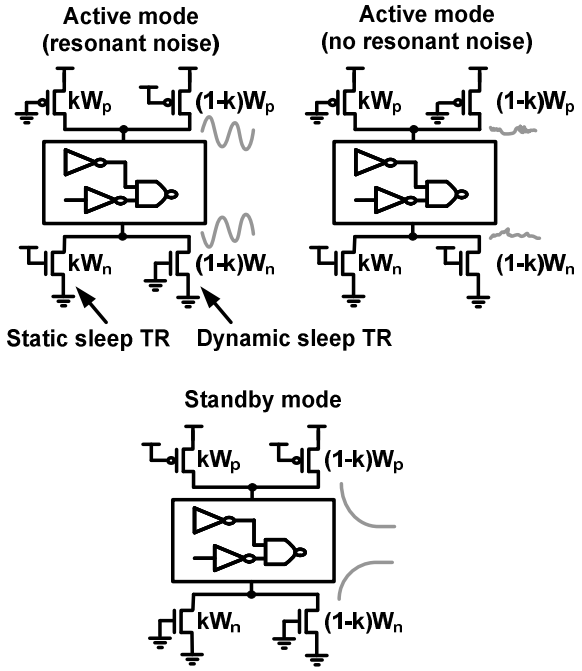


Fig. 5. Conceptual diagram of adaptive sleep transistor control.

Fig. 6 shows the schematic diagram of the proposed adaptive sleep transistor circuit which includes a resonant supply noise sensor to detect the presence of mid-frequency noise. The noise sensor consists of a constant delay line (CDL) and a variable delay line (VDL). RC filter bandwidth for the CDL supply voltage is 10MHz while that of the VDL supply voltage is 600MHz. As a result, only the supply noise components having a frequency between 10MHz and 600MHz affect the delay difference of the two delay lines. This simple RC filtering scheme implements a bandpass filter for detecting the dominant resonant noise. The upper cut-off frequency (600MHz) had to be made higher than the resonant noise frequency to account for the non-ideal passive filter characteristics. In the presence of mid-frequency resonant noise, the delay of VDL varies with supply voltage while the delay of CDL is nearly constant because of the RC filter. The comparator compares the delay of the two lines and switches on/off a portion of the sleep transistors. 7/8 of the total sleep transistor width was used for the dynamic sleep transistor (i.e. k in Fig. 5 is 1/8). During normal condition with no resonant noise, the CDL runs faster than the VDL because a smaller R is used in the RC filer of the CDL by design so that the IR-drop of the CDL is smaller than that of the VDL. In case a resonant oscillation occurs, the supply overshoot increases the speed of the VDL which issues a DAMP signal when the speed of the VDL becomes equal to or faster than that of the CDL. The DAMP signal is used to turn off a fraction of the total sleep transistor which damps the resonant noise. After the overshoot cycle is over, the sleep transistors will return to the normal configuration to avoid additional IR-drop caused by the increased damping resistance. Detecting an overshoot is preferred over detecting an undershoot for the sleep transistor switching as it (i) ensures the detection of resonant oscillation rather than a normal IR-drop in which case increased damping does not help and (ii) prevents additional IR-drop during the undershoot cycle that may be caused by the sensor circuit delay.

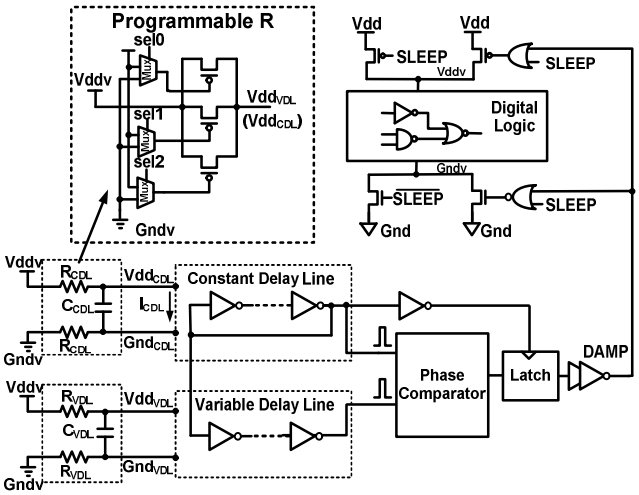


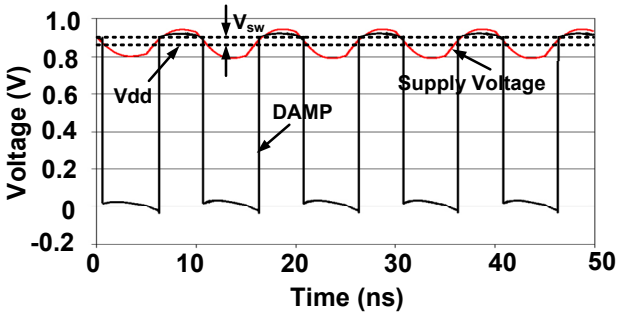
Fig. 6. Schematic of the proposed adaptive sleep transistor scheme including a digital resonant noise detector with two delay lines.

B. Supply Noise Simulation Results

Fig. 7(a) shows the simulated waveforms when a resonant noise occurs in the supply. Vddv and Gndv are the virtual supply rails, Vdd is the fixed external supply voltage, and V_{sw} is the triggering threshold for the supply overshoot. When the supply voltage is below Vdd+V_{sw}, the CDL runs faster than the VDL and thus the DAMP signal is off so all the sleep transistors are turned on to minimize the IR-drop. When the supply voltage is above Vdd+V_{sw}, CDL becomes slower than the VDL and the DAMP signal turns of a fraction of the sleep transistors to damp the resonance. The switching threshold V_{sw} can be determined by equations below assuming both the CDL and the VDL have equal supply voltages and current consumption *I* at the switching threshold.

$$\begin{aligned} V_{dd} + V_{sw} - IR_{VDL} &= V_{dd} - IR_{CDL} \\ V_{sw} &= I(R_{VDL} - R_{CDL}) \end{aligned} \quad (3)$$

R_{VDL} and R_{CDL} are realized by linear mode MOSFET transistors. The effective resistance values are programmable by turning on different number of transistors so that the switching voltage V_{sw} can be adjusted. Programmability of the switching voltage is essential in nanometer CMOS technologies where device variability is severe. Fig. 7(b) shows the outputs of the CDL and VDL during a switching event. As the supply voltage reaches the switching threshold, both lines run at a same speed and the DAMP signal is issued. Fig. 7(c) compares the resonant supply noise with and without the adaptive sleep transistors. A 32% reduction of peak-to-peak noise amplitude has been achieved using the adaptive scheme. Both undershoot and overshoot are smaller with the proposed circuit because of the increased damping of the supply network.



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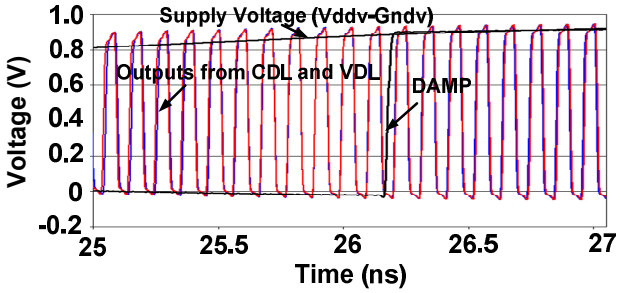

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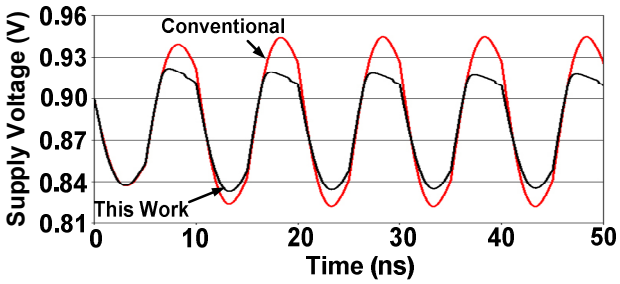

(c)

Fig. 7. (a) DAMP signal for a V_{sw} of 20mV; (b) Outputs of the CDL and VDL with resonant noise; (3) Comparison of supply noise with and without the adaptive sleep transistor scheme.

Fig. 8 shows the supply noise in the frequency domain. The resonance has been significant reduced using the adaptive sleep transistor technique. For frequencies outside of the resonant peak, the performance of the adaptive scheme becomes similar to that of the conventional scheme because adaptive sleep transistors are designed only to respond to large oscillations at the mid-frequency range. Compared to the non-adaptive sizing results in Fig. 1(b), the adaptive sleep transistor eliminates the penalty of additional IR drop at low frequencies.

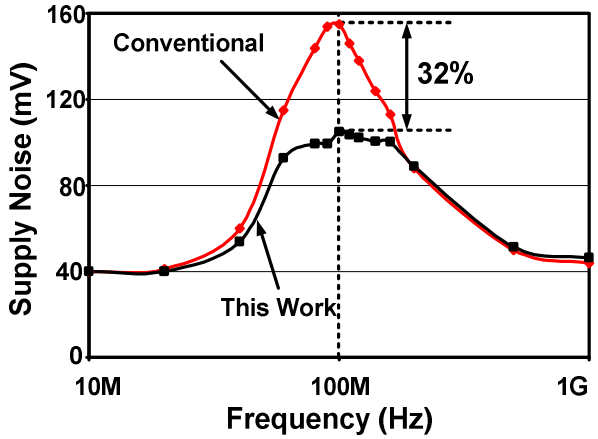

Fig. 8. Supply noise spectrum with and without the adaptive sleep transistor control.

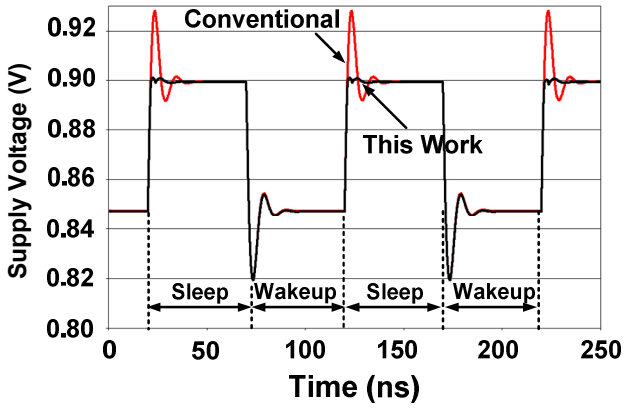

Fig. 9. Simulated noise waveform during 40mA current switching.

Fig. 9 shows the supply noise oscillation during a 40mA current switching event which excites the resonant oscillation. Using adaptive sleep transistors, the overshoot noise is suppressed due to the increased damping from the smaller effective sleep transistor. The magnitude of the undershoot noise is not reduced in this case because adding damping is not effective in preventing the voltage undershoot when the noise is caused by an abrupt excitation.

The proposed adaptive sleep transistor technique can achieve a lower supply noise compared to the fixed sizing scenario presented in section III because it reduces the resonant supply noise without having to trade off the IR-drop. Both the worst case noise during a sporadic resonance and the average non-resonant case noise can be simultaneously minimized offering maximum circuit performance. Fig. 10 shows the IR noise, resonant noise, and total supply noise with and without the adaptive sleep transistors for different total sleep transistor

widths. Equal amount of DC and AC current is used in this test to generate the DC noise and resonant noise. The total noise in the figure represents the worst case undershoot which is the sum of DC noise and resonant noise. The figure shows that adaptive sleep transistors slightly increase the DC noise but significantly reduces the resonant noise. Overall, a 17% reduction in worst case supply undershoot is achieved compared to a fixed sizing scheme. The proposed technique increases the optimum sleep transistor width from 330µm to 470µm as the extra damping can be provided by turning off a fraction of the total sleep transistor.

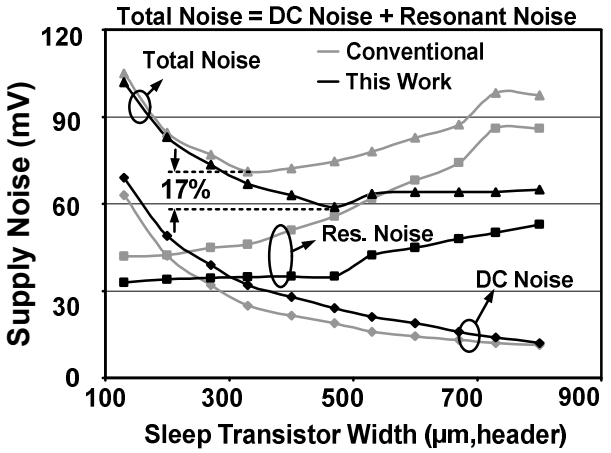

Fig. 10. Worst case supply noise comparison between the proposed and conventional sleep transistors. Equal DC and AC currents were used to generate the DC noise and resonant noise.

Table 2. Results of the proposed adaptive sleep transistor circuit**.**

Technology	32nm CMOS	**Static Current Overhead**	0.4mA
Bandwidth	10MHz to 600MHz	**Design Overhead**	31pF*
Equivalent Decap Saving	120pF	**Area Saving**	17%

* The C_{CDL} and C_{VDL} used in the RC filters dominate the total overhead area. The actual circuit area overhead for the adaptive sleep transistor is ignored for the sake of simplicity.

Table 2 summarizes further details of the proposed adaptive sleep transistor circuit. The total static power consumption was only 0.4mA because a low-power fully-digital resonant sensor was used for the noise detection. The proposed circuit introduces an area overhead mainly due to the 31pF capacitance in the RC filters. However, the adaptive sleep transistor circuit is equivalent to a 120pF decap in terms of supply noise which translates into an overall decap saving of 17% (an internal decap of 315pF is present in the circuit).

V. CONCLUSIONS

In this work, we show the importance of considering resonance supply noise for optimal sleep transistor sizing. Unlike conventional wisdom, a smaller sleep transistor can reduce the worst case supply noise due to the strong damping of the dominant resonant noise. Simulations show that 24% reduction in peak-to-peak resonant noise can be achieved using a 50% smaller sleep transistor. Resonant noise happens irregularly so a small sleep transistor for maximum resonant suppression will impose a delay penalty at times when there is no resonant noise. To mitigate this issue, an adaptive sleep transistor circuit is proposed to reduce the effective sleep transistor size only when a resonance is detected. The proposed technique achieves 32% reduction of resonant noise and 17% reduction of total supply noise without having to trade off the IR-drop.

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