An On-Chip NBTI Sensor for Measuring PMOS Threshold Voltage Degradation

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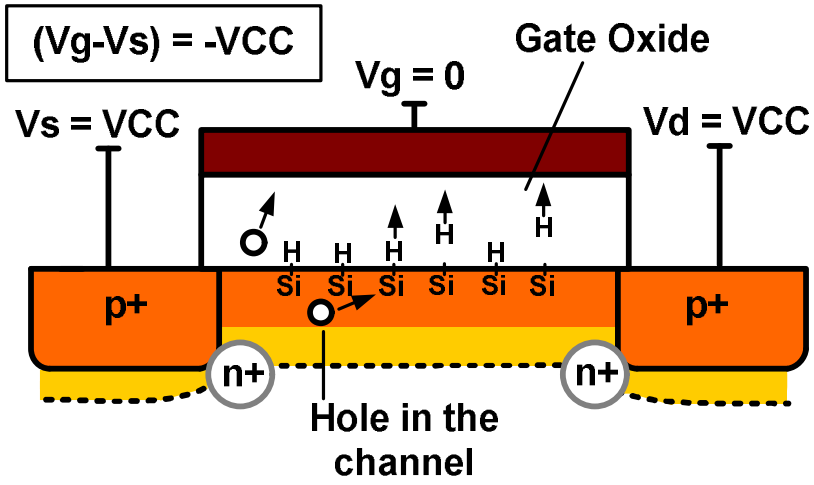
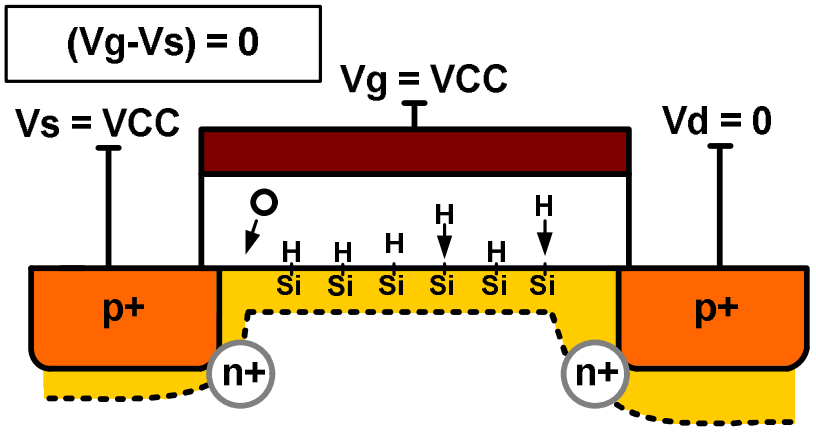
Presentation Agenda

- Introduction to Negative Bias Temperature Instability (NBTI)
- Prior NBTI Sensors
- Proposed DLL-Based NBTI Sensor
- Measurement Results
- Conclusions

Introduction to NBTI

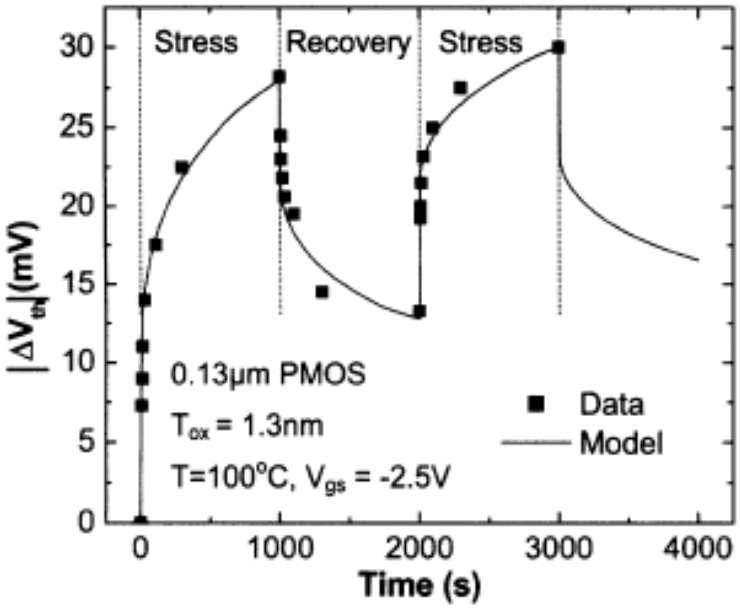


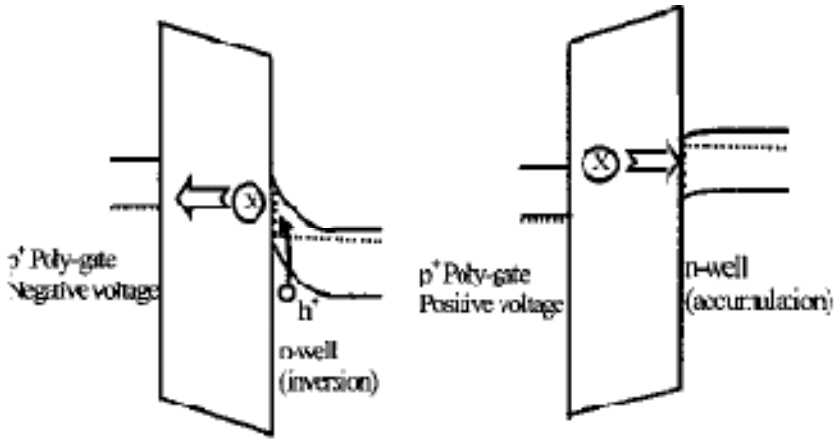


Stress Conditions **Recovery**

- **Channel holes interact with Si-H bonds at interface**
  - **Interfacial traps and oxide trapped charges are created**
- **Causes an increase in |Vtp|**
  - **Expect up to ~20-30% increase in ten years**
- **Partial recovery occurs when PMOS is turned off**
  - **Dangling bonds passivated and oxide trapped holes are released**

Stress and Recovery



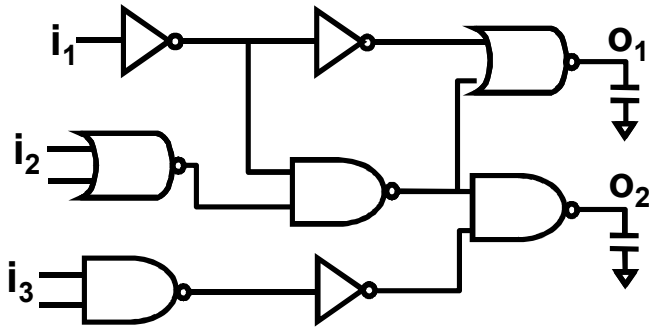


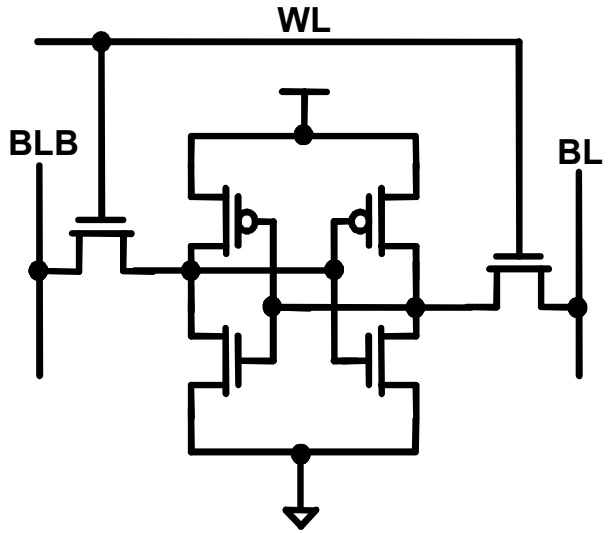
Stress **Recovery**

- **ΔVtp partially recovers when stressed PMOS is turned off**
- **AC stress increases lifetime projection**
  - **Makes measurements more difficult**
  - **Recovery occurs *during* each reading**
- **Increasing field and temperature, reduced gate overdrive reintroduce NBTI concerns in the late 90s**

G. Chen, et al., IRPS 2003
R. Vattikonda, et al., DAC 2006

NBTI Impact on Digital Circuits





Logic circuits

- F_{MAX} degrades
- Leakage power reduces
- Critical path can change

Memory circuits

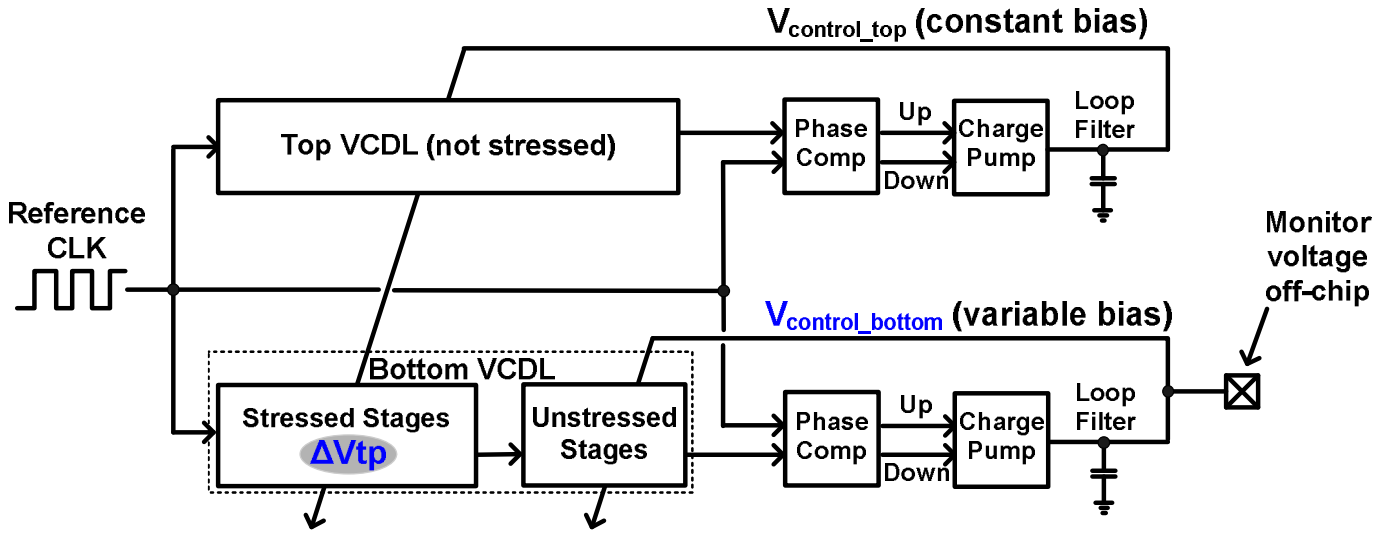
- Read margin worsens
- Write stability improves
- Read delay remains the same

- **NBTI affects critical circuit parameters**
- **Must account for NBTI-induced shifts during the design phase**

Prior NBTI Sensors

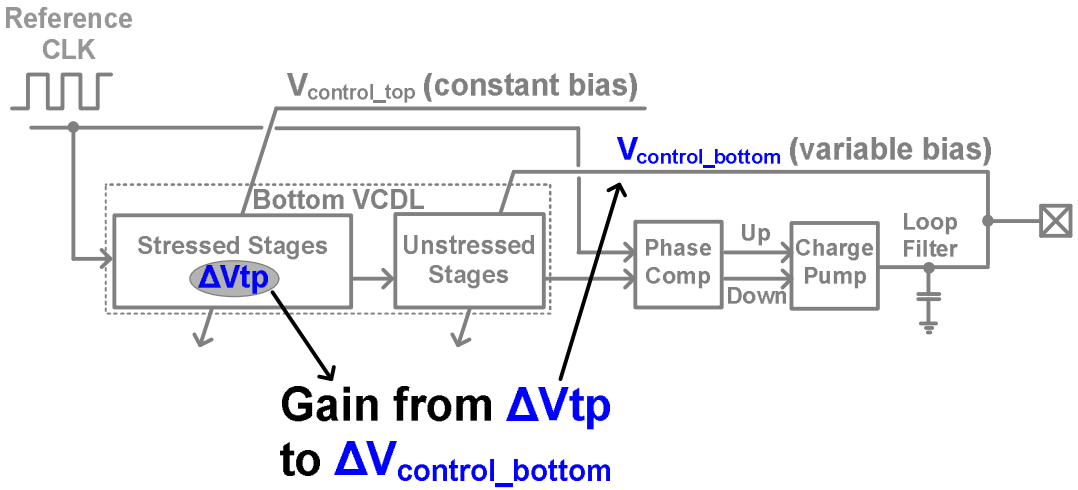
- Fernandez et al. used ROSCs to generate AC stress on-chip for better signal integrity. (IEDM, Dec. ’06)
- Kim et al. detected the beat frequency between stressed and unstressed ROSCs for high resolution and fast measurements (VLSI Circuits Symposium, June ’07)
- Ketchen et al. also used beat frequency concept, and designed ROSCs with a new delay stage for pure NBTI stress (ICMTS, March ’07)
- Shen et al. proposed 100ns I-V measurement (IEDM, Dec. ’06)

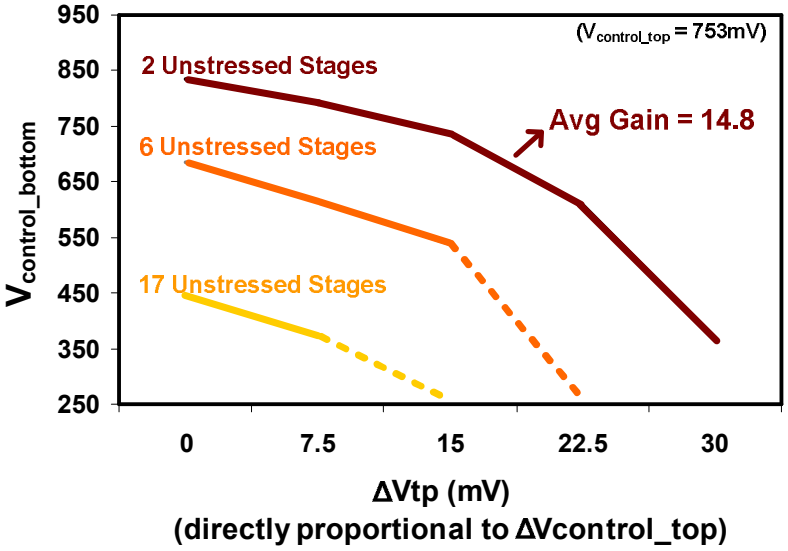
Proposed NBTI Aging Sensor



- DLL control voltage adjusts to lock VCDL into phase with the reference clock
- Stressed Stages slow with NBTI stress; Unstressed Stages must speed up to match reference clock
  - Translate ΔVtp into control voltage of bottom DLL, $\Delta V_{control\_bottom}$
- System facilitates both DC and AC stress, as well as 20us+ measurement times

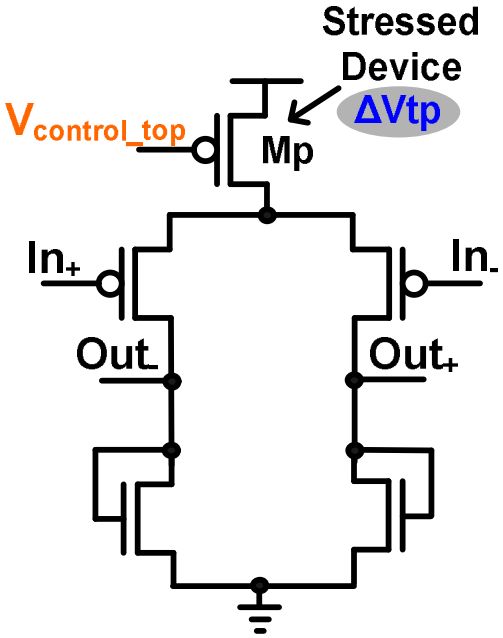
NBTI Measurement Gain

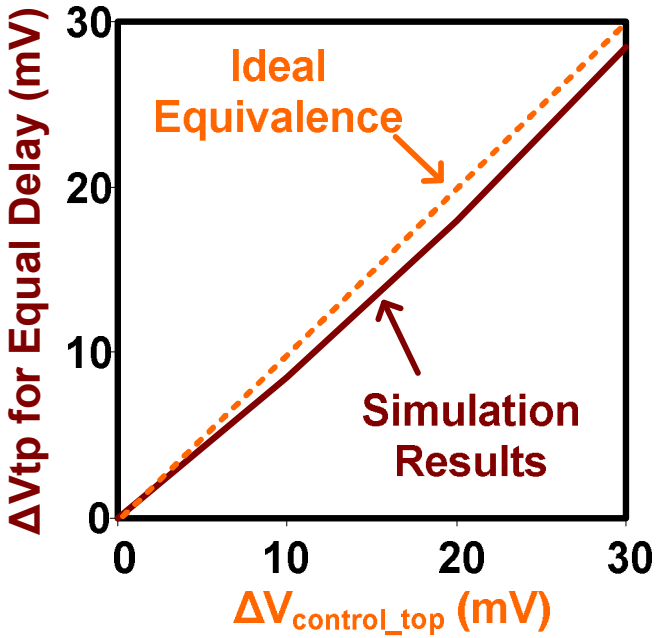




- We achieve a gain of up to 16X in the translation of ΔVtp to $\Delta V_{control\_bottom}$
- Adjust gain by tapping a particular output from the Unstressed Stages
  - Get larger gain with fewer Unstressed Stages
- ΔVtp is directly proportional to $\Delta V_{control\_top}$ with respect to Stressed Stage delay, allowing for system calibration

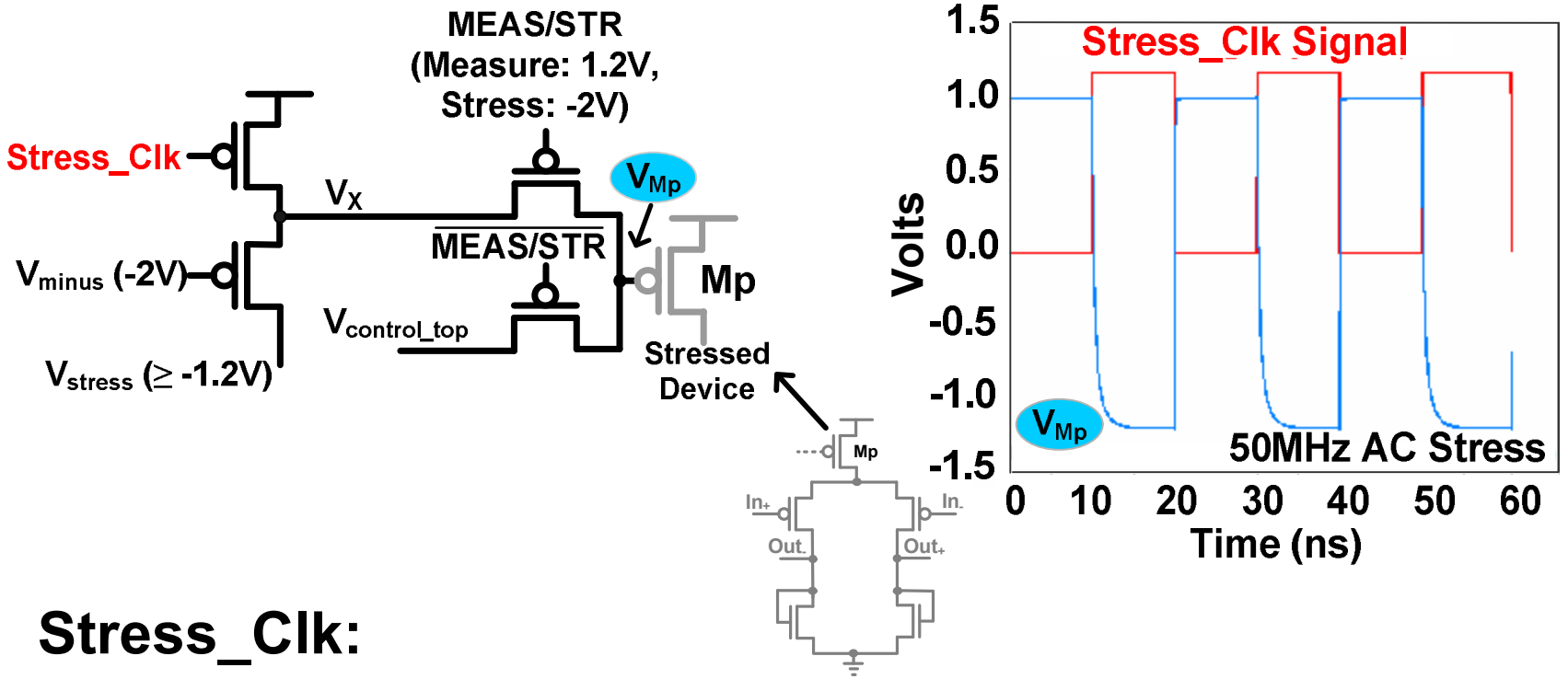
Stressed Stage Buffer Design





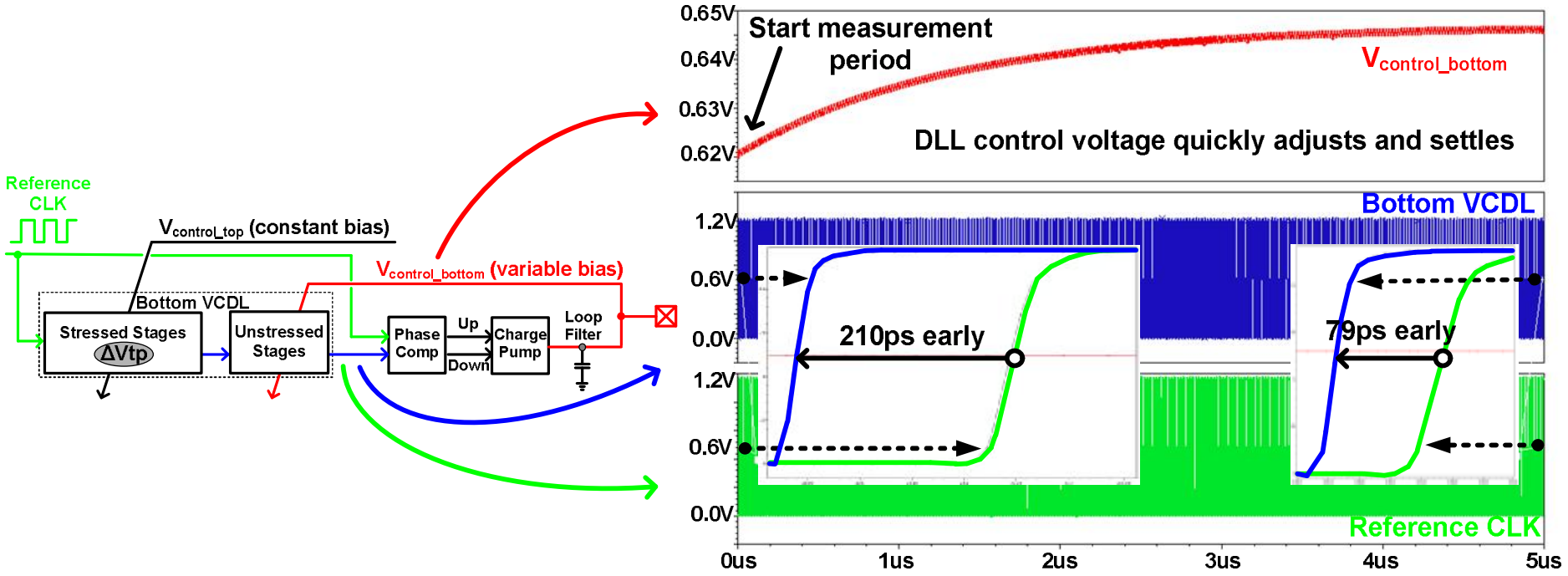
- **ΔVtp is directly proportional to $\Delta V_{control\_top}$**
  - Both have ~same effect on buffer delay
  - Delay ∝ Current ∝ (Vgs –Vtp)
- **This relationship allows us to calibrate the sensor**
  - Turn off top DLL and manually adjust $V_{control\_top}$
  - Monitor the corresponding change in $V_{control\_bottom}$

Stress Switches



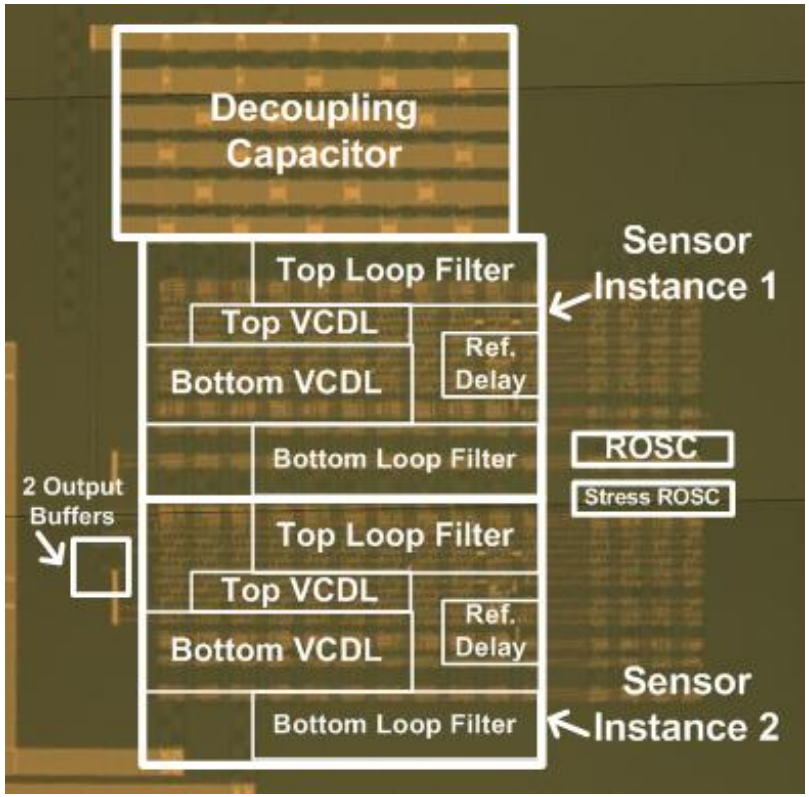
- **Stress_Clk:**
  - 0V during measurement period
  - VCC! during DC stress
  - AC signal up to 50MHz during AC stress
- **V_{minus} is set at -2V to pass the ≥-1.2V V_{stress} signal**
  - Accelerated stress conditions

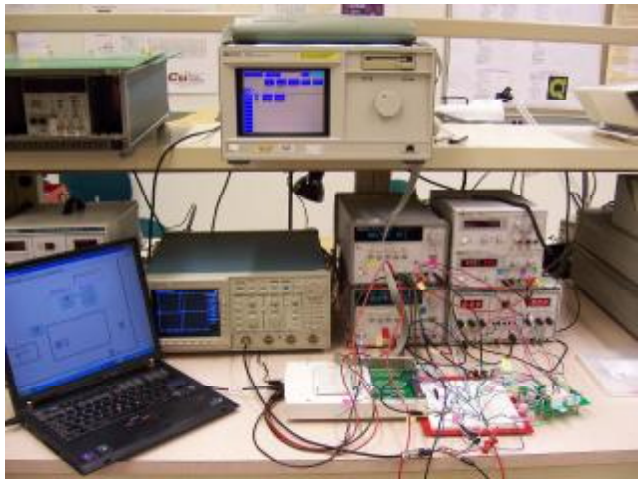
DLL Locking Time



- **Bottom DLL locks quickly (<20µs)**
- **Small phase offset after control voltage settles (<80ps)**
- **Facilitates fast measurements after stress conditions are removed**

Test Chip Characteristics

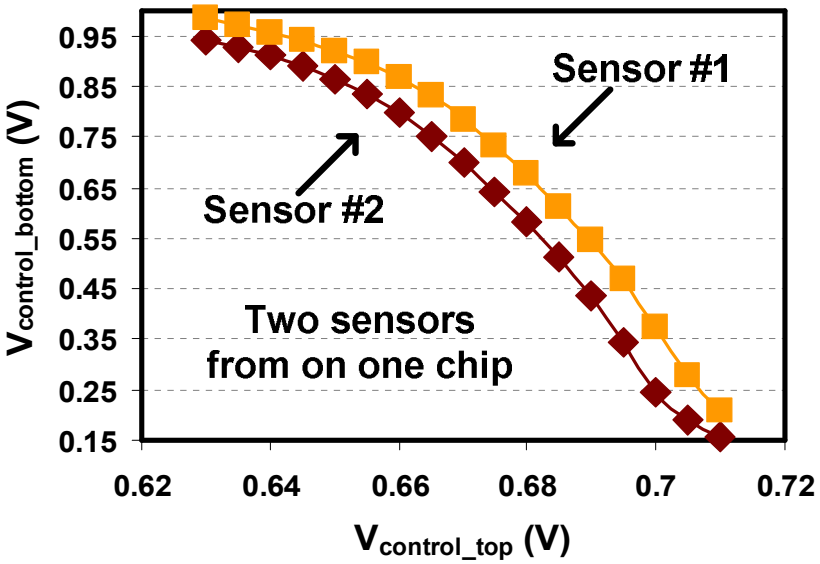


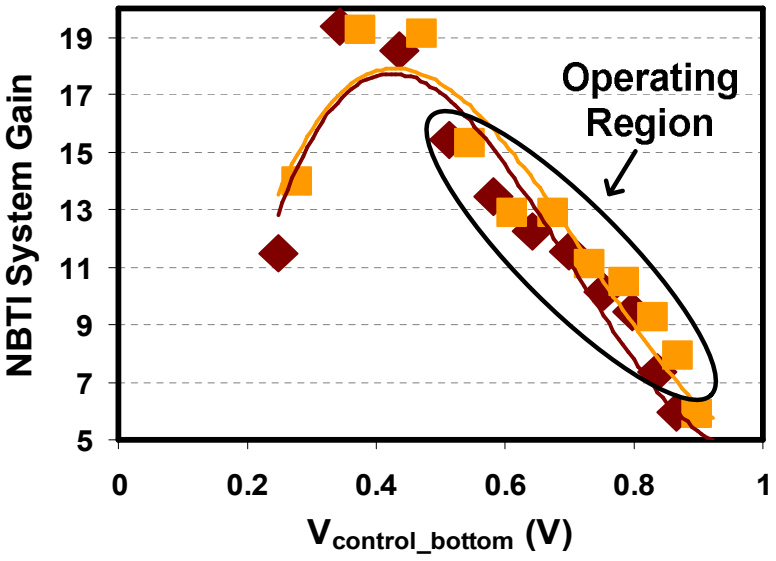


Technology	0.13µm CMOS
Supply	1.2V
Dimensions (2 instances grouped)	545µm x 510µm
Max Sensing Gain	16X

- 130nm test chip fabricated by UMC
- Multiple circuit instances placed on each chip
  - Devices may never fully recover from stress
  - Each system can only be measured once

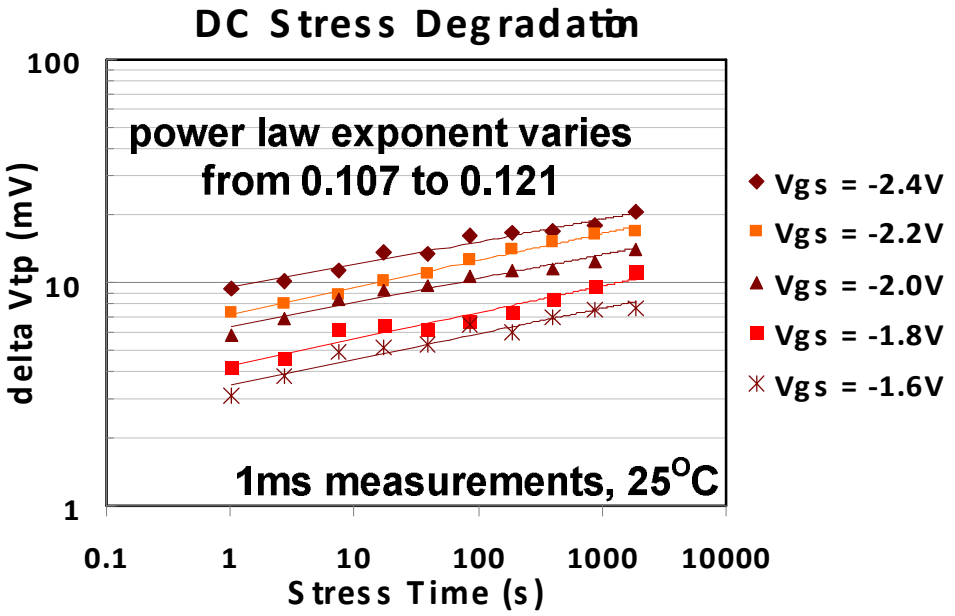
NBTI Test Chip Gain

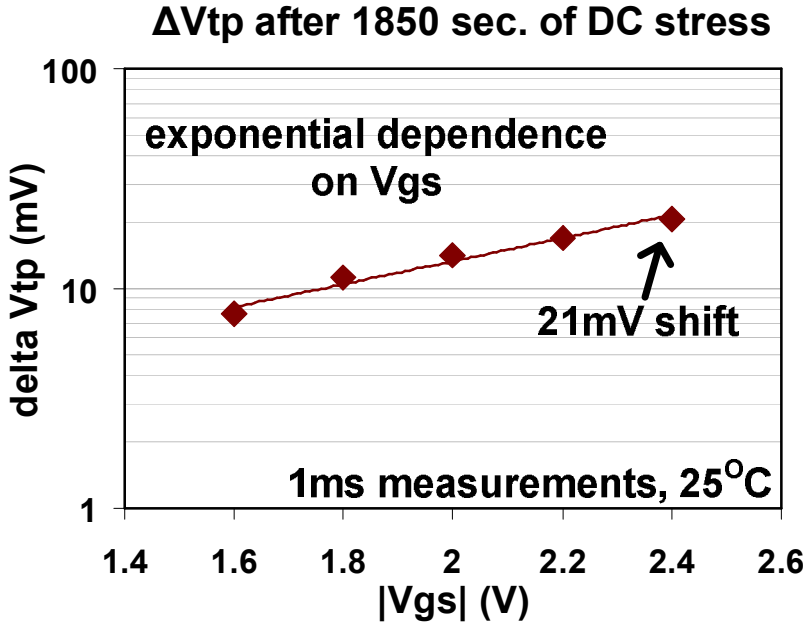




- Recall that ΔVtp in stressed buffers is ∝ $\Delta V_{control\_top}$
- Sweep $V_{control\_top}$ and read $\Delta V_{control\_bottom}$ to find system gain from ΔVtp to $\Delta V_{control\_bottom}$
  - Max gain of 16X in the operating region
- Polynomial fit to the gain plot
  - Used this equation to translate $\Delta V_{control\_bottom}$ reading to ΔVtp for each sensor

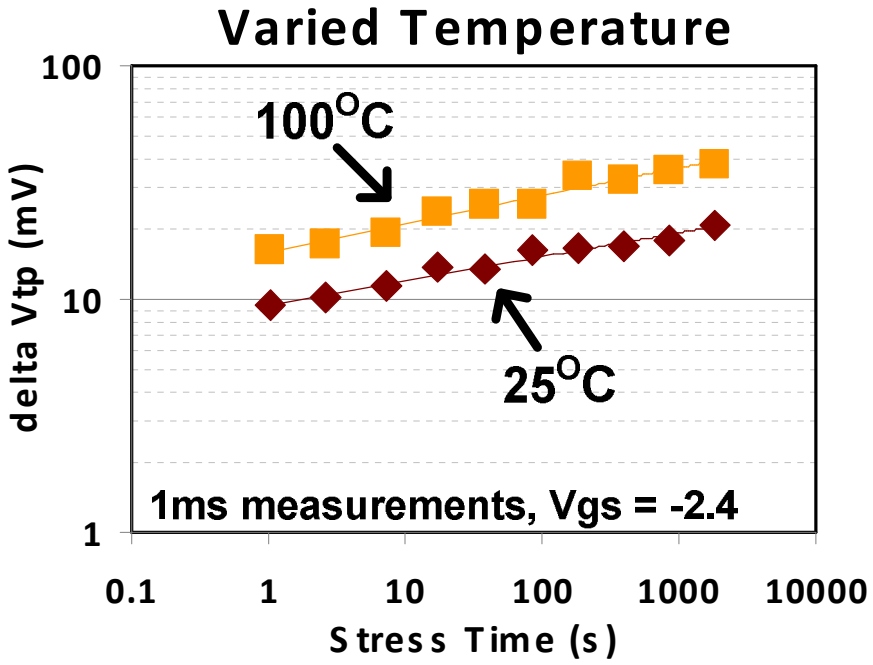
Test Chip Measurements

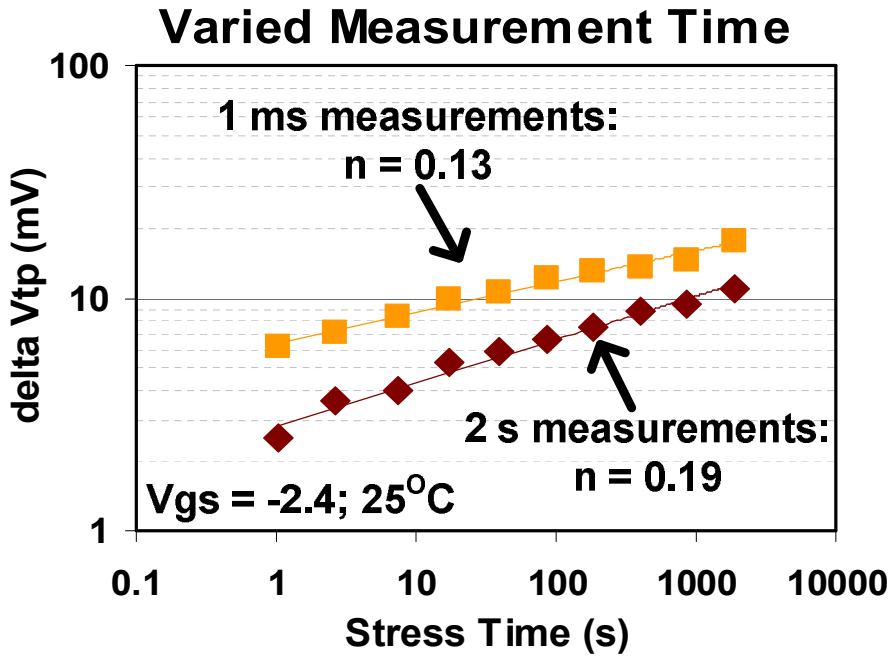




- System facilitates measurements over a range of Vgs
- Power law exponents in 0.1 range match well with recently presented results
- Threshold degradation shows exp. dependence on Vgs

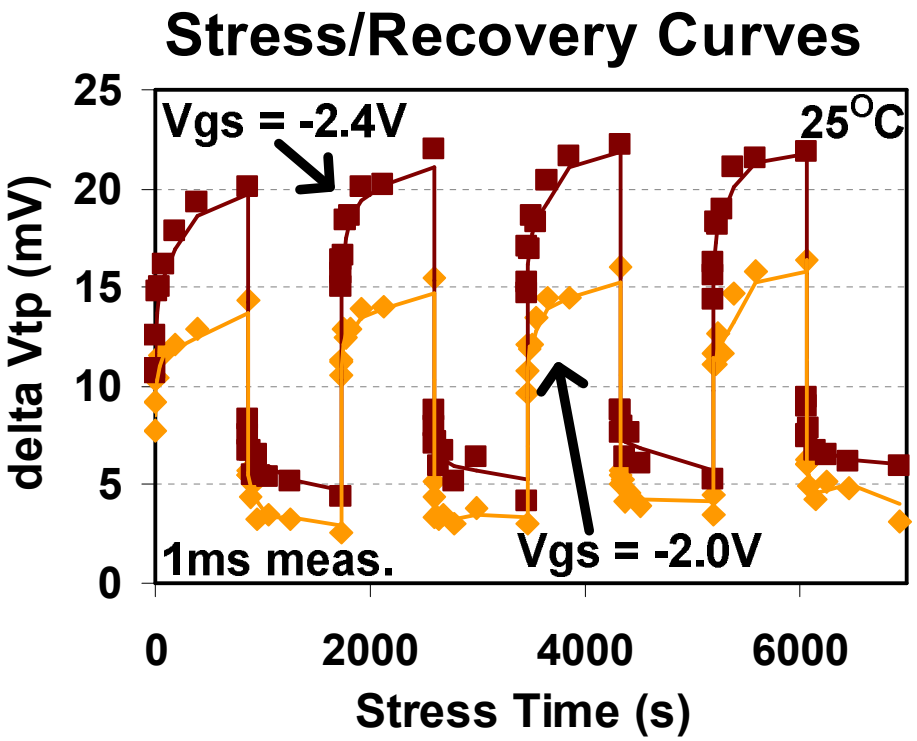
Test Chip Measurements

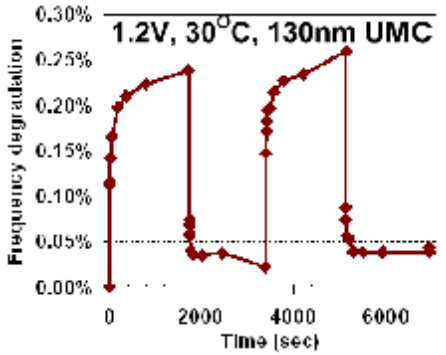




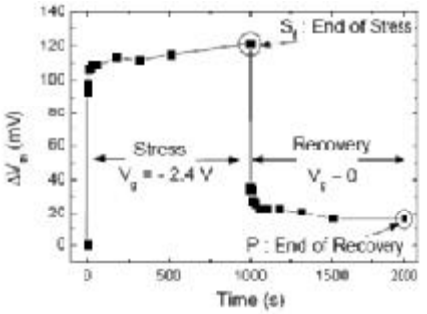
- **Left Plot: Increased degradation with temperature**
- **Right Plot: Increase in power law exponent is observed with longer measurement (recovery) periods**

Test Chip Measurements





T. Kim, VLSI Circuits Symp., 2007



C. Shen, IEDM, 2006

- Stress/Recovery curves demonstrate fast recovery
  - Also found by C. Shen and T. Kim with high-speed measurements
- ΔVtp does not fully recovery in ~1000s at 25C

Conclusions

- There is a great need to develop reliable degradation models to avoid wasteful over-design methods
- Fast measurement times are critical for accurate NBTI characterization
- We have implemented an NBTI degradation sensor capable of measurements in tens of microseconds
  - Directly map the measured parameter to ΔVtp
  - Facilitates DC and AC stress states
  - Max gain of 16X in ΔVtp measurement
  - Measurements demonstrated for a range of stress voltages, temperatures, and measurement times