An On-Chip NBTI Sensor for Measuring PMOS Threshold Voltage Degradation

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ABSTRACT

Negative Bias Temperature Instability (NBTI) is one of the most critical device reliability issues facing scaled CMOS technology. In order to better understand the characteristics of this mechanism, accurate and efficient means of measuring its effects must be explored. In this work, we describe an on-chip NBTI degradation sensor using two delay-locked loops (DLL). The increase in PMOS transistor threshold due to NBTI stress is translated into the control voltage of a DLL for high sensing gain. Measurements from a 0.13µm test chip show a maximum gain of 16X in the operating range of interest, with micro-second order measurement times for minimal unwanted recovery. The proposed NBTI sensor also supports various DC and AC stress modes.

Categories and Subject Descriptors

B.8.1 [**Performance and Reliability**]: Reliability, Testing, Fault-Tolerance

General Terms

Measurement, Design, Reliability, Experimentation

Keywords

NBTI, Aging, Delay Locked Loop

1. INTRODUCTION

As the CMOS IC industry continues to follow an aggressive scaling roadmap, designing reliable circuits has become more complex with each technology node. Several reliability issues that have been recognized for some time are becoming increasingly problematic as more devices are placed on a chip, oxide thicknesses are scaled down to just a few nanometers, and voltage margins are reduced. One complexity that has recently attracted a great deal of attention is Negative Bias Temperature Instability (NBTI) [1-16]. As the oxide thickness of PMOS transistors shrinks, the shift in the threshold voltage caused by NBTI can become a dominant limiting factor in device lifetime. A growing body of research is devoted to further understanding this mechanism in order to equip circuit designers with the knowledge and tools they need to create robust systems in CMOS processes experiencing problematic NBTI degradation.

NBTI is characterized by a positive shift in the absolute value of the PMOS threshold voltage ($|V_{tp}|$), which occurs when the device is placed under stress conditions (V_{gs} = -VCC), especially at high temperatures. The degradation in V_{tp} has a power–law dependency on time, and is a function of the stress voltage level and temperature.

ISLPED'07, August 27–29, 2007, Portland, Oregon, U.S.A.

This threshold shift is generally attributed to the breaking of Si-H bonds at the oxide interface by holes in the PMOS inversion layer. The bond breaking process causes hydrogen species to diffuse into the gate oxide, creating interfacial and bulk traps (Figure 1.a). Those traps are assumed to be positively charged (Q_{int} and Q_{ox}, respectively) or neutral depending on their electron occupancy. The resulting change in positive charge density is related to the increase in V_{tp} in the model proposed in [15] as follows:

$$\Delta V_{tp} = \left(\Delta Q_{int} + \Delta Q_{ox}\right) \bullet \left(d_{ox} / \kappa_{ox}\right).$$

In this equation, κ_{ox} is the oxide permittivity and d_{ox} is the oxide thickness. However, other models have been proposed, and the specific mechanisms used to explain NBTI degradation are still a topic of debate. While the creation of interfacial traps is commonly cited as the root or sole cause of the threshold voltage shift, oxide trapped holes and hydrogen trapping in the oxide have all also been linked to the shift in V_{tp} in a number of works. [1, 2, 13].

When the stress conditions are removed (i.e., V_{gs} = 0), a device enters the *recovery* or *passivation* phase, where H atoms diffuse back towards the oxide/silicon interface and anneal the broken Si-H bonds, thereby reducing $|V_{tp}|$, (Figure 1.b) [3, 5, 6]. Certain works have claimed that the hole detrapping effect in the oxide is the primary origin of this recovery [1, 2]. In any case, the reduction in $|V_{tp}|$ observed when stress conditions are removed leads to a significantly longer device lifetime than would be predicted by DC stress experiments. Projected improvements in lifetime when considering recovery during the device off-state, versus DC stress prediction data, range from 2-3X [3] to an order of magnitude [4, 5]

In order for circuit designers to mitigate the impact of NBTI degradation during the early design phases, without using costly over-design methods such as liberally sizing up stressed devices or excessive guard-banding, accurate predictive models must be developed and incorporated into their suite of design tools. Recent efforts have been devoted to developing such models [3, 6, 7, 15]. However, these models must be solidly corroborated by reliable hardware data. While many measurement methods have been proposed, refining these methods is still an active field of research.

Much of the work examining NBTI degradation in hardware has involved highly invasive measurement systems, or techniques requiring specialized measurement equipment (these and other features of previous methods are explored in Section 2). In this work we propose an on-chip sensor that translates the PMOS threshold degradation caused by NBTI into the control voltage of a delay-locked loop (DLL), which can be readily monitored with standard off-chip scopes. Our design allows us to measure the affects of both DC and AC stress, and is capable to taking measurements within 20µs in order to avoid unwanted recovery. This circuit enables us to thoroughly investigate NBTI recovery behavior, as well as the frequency dependency of AC stress signals, which are both currently topics of interest.

The remainder of this paper is organized as follows. In Section 2 we will examine previously employed techniques for measuring the effects of NBTI degradation. Section 3 presents the design of our proposed measurement system, along with points of interest in selected system components. Section 4 covers the hardware

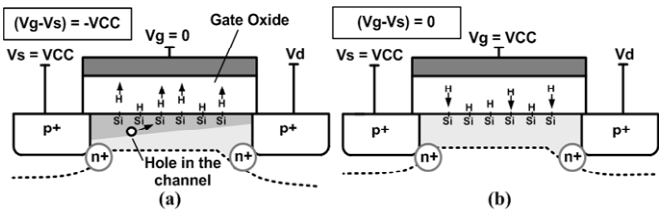


Figure 1. Cross section of a PMOS transistor under NBTI stress conditions (a), and in the recovery phase (b). Note that in addition to the breaking of Si-H bonds at the Si/SiO_2 interface, and the annealing of the traps formed by this process, other mechanisms such as oxide-trapped holes also play a role in NBTI degradation and passivation [1, 2, 13, 15].

implementation and measurement results, and our conclusions are summarized in Section 5.

2. PREVIOUS NBTI MEASUREMENT TECHNIQUES

As stated above, many previous NBTI measurement techniques involved highly invasive experimental setups that required specialized testing equipment and/or access to individual transistors under test. In this section, we will summarize a number of those methods along with their benefits and drawbacks.

Chen et al. were the first to report the partial recovery of PMOS transistor strength when stress conditions are removed, and the longer device lifetime that results from this effect [5]. The authors of that work used an improved direct-current current-voltage (DCIV) measurement technique to monitor the formation of interface traps. This method allowed them to observe a strong correlation between ΔV_{tp} and ΔN_{it}, but required the sensitive monitoring of base and collector currents in a gate-controlled parasitic BJT of a MOSFET.

Denais et al. proposed an on-the-fly measurement technique in order to avoid the recovery inherent in most measurement methods [8]. This unwanted recovery is a product of the periodic removal of stress conditions for some finite time while the desired circuit parameters are extracted. Such measurements will result in overly optimistic degradation results. In their proposed method, the stress voltage is kept quasi-constant, and the linear drain current is measured throughout the stress experiment to monitor device degradation. The authors claim that this technique results in little or no unwanted recovery, leading to a more accurate characterization of NBTI degradation. However, it requires the invasive probing of individual device currents.

In [9], the on-the-fly technique was extended to characterize the recovery after stress conditions are removed. The authors also state that existing methods at that time were not well suited to measure PMOS degradation due to AC stress, and proposed using circuit parameters such as ring oscillator frequency to extract aging information under alternating stress conditions. Aota et al. also proposed a measurement method to minimize unwanted device recovery during the measurement period by using sophisticated fully-automatic wafer probing [10]. The uncontrollable relaxation time in this technique was still 5ms, though. Subsequent research has shown that recovery can become significant in 1ms or less [14], necessitating measurement techniques with even shorter reaction times.

In more recent work, Fernández et al. proposed on-chip circuits for the measurement of device degradation due to AC NBTI stress up to the GHz range [11]. The authors state that most previous FET test structures could not reliably apply a high-frequency stress signal

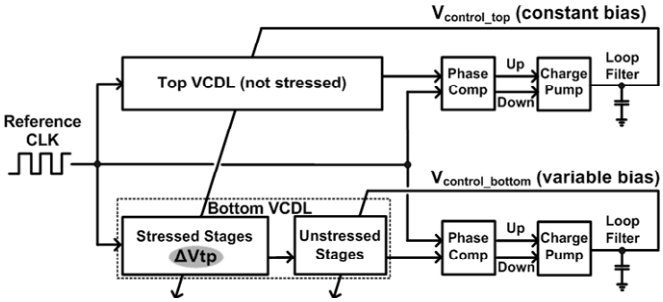


Figure 2. High-level block diagram of the proposed NBTI degradation sensor. This system is primarily composed to two DLLs. The Reference CLK is generated on-chip to maintain signal integrity.

to the devices under test, and therefore detailed knowledge of the frequency dependency of NBTI aging was lacking. In their work, I-V curves of both single transistors under test, as well as inverters placed under stress, were used to extract ΔV_{tp} during stress. An on-chip clock generator was used to create the high frequency stress signals. Finally, Kim et al. introduced an aging monitor which is capable of taking extremely fast and precise degradation measurement by detecting the beat frequency of a pair of ring oscillators, where only one is placed under accelerated stress [16].

In this paper, we propose a new method to monitor the V_{tp} degradation due to NBTI using dedicated on-chip circuits. Our method also facilitates the application of both DC and AC stress signals, but with an increased stress voltage to accelerate experiment times. No specialized measurement equipment is required for the proposed measurement system, which directly amplifies PMOS threshold degradation into a voltage that can be easily monitored off-chip.

3. PROPOSED NBTI SENSOR DESIGN

3.1 System-Level Overview

A high-level block diagram of the degradation measurement system is displayed in Figure 2. The NBTI sensor is composed primarily of two DLLs and an on-chip clock generator. Each DLL contains a voltage controlled delay line (VCDL), and the circuitry needed to adjust the control voltage which locks the VCDL outputs into phase with the Reference CLK. As shown in Figure 2, this control circuitry includes a phase comparator, a charge pump, and a loop filter. The Top DLL is included to provide a roughly constant bias ($V_{control\_top}$), while the Bottom VCDL contains the stages that are periodically placed under NBTI stress, along with a number of Unstressed Stages. The Stressed Stages in the Bottom DLL are biased by the constant $V_{control\_top}$ during measurements (when stress conditions have been removed), so this portion of the VCDL will slow down after periods of accelerated NBTI stress. The Unstressed Stages in this structure are biased by the variable voltage $V_{control\_bottom}$, which will adjust to speed up those buffers in order to compensate for the slower stressed portion. $V_{control\_bottom}$ decreases with stress as shown in Figure 3, for reasons to be explained in Section 3.4.

3.2 System Gain and VCDL Design

Our design was tuned to attain maximal gain from the threshold degradation in the Stressed Stages to the decrease in $V_{control\_bottom}$,

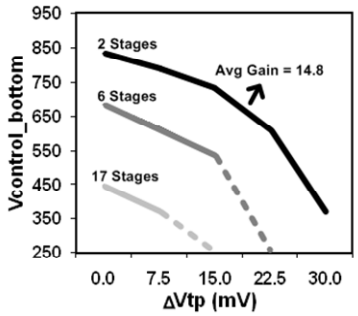


Figure 3. Translation of ΔVtp to $\Delta V_{control\_bottom}$ from simulation. ΔVtp is directly proportional to $\Delta V_{control\_top}$, as shown in Figure 4. The system gain is adjusted by choosing a particular number of Unstressed Stages, as indicated in this plot.

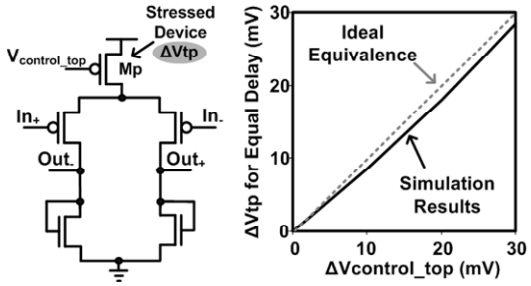


Figure 4. Differential buffer stage design. ΔVtp of Mp in the stressed buffers is directly proportional to $\Delta V_{control\_top}$. This relationship allows us to calibrate the sensor.

since this signal will be measured off-chip and translated into the threshold shift. That gain can be adjusted by selecting the number of delay buffers to use in the Unstressed Stages portion of the Bottom DLL, as well as in the Reference CLK delay structure. An output tap is selected in each case by using a network of MUXs. Figure 3 shows the translation of Vtp degradation in the Stressed Stages to a decrease in $V_{control\_bottom}$ for a number of Unstressed Stages delay line lengths, with $V_{control\_top}$ held constant at 753mV. The average gain across a reasonable threshold degradation range (30mV) when using only two Unstressed Stages is 14.8X. As illustrated in Figure 4, ΔVtp is directly proportional to $\Delta V_{control\_top}$ in the differential buffer structure used for the Stressed Stages. That is, Vtp must be changed by the same amount as $V_{control\_top}$, with the other held constant, in order to cause an equivalent stage delay shift. This relationship can be derived from the standard saturation current equation:

$$I_D = \frac{1}{2}\mu_p C_{OX}\left(\frac{W}{L}\right)\left(V_{control\_top} - VCC - Vtp\right)^{\alpha}.$$

Therefore, the system gain from ΔV_{tp} to $\Delta V_{control\_bottom}$ can be checked during calibration by turning off the Top DLL and manually adjusting $V_{control\_top}$, while monitoring the resulting change in $V_{control\_bottom}$. This curve will directly correspond to the final measured stress curve, allowing us to extract ΔV_{tp}.

3.3 Stress Switch Design

The stress switches used in the bottom VCDL presented unique challenges because they contain devices with gate and/or drain terminals tied to relatively large negative voltages (Figure 5). The

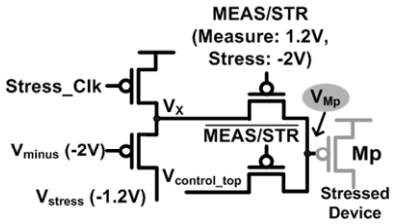


Figure 5. Stress switch capable of driving -1.2V stress signal at V_{Mp}. This structure facilitates DC stress conditions, as well as AC stress up to 50MHz (see Figure 6).

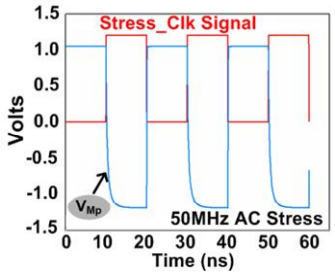
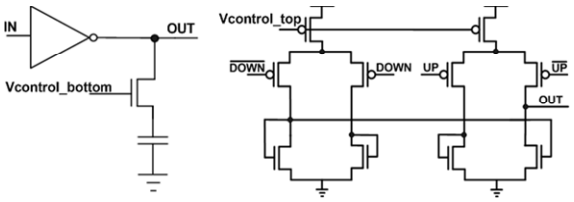


Figure 6. Simulated AC stress waveforms generated by an extracted netlist of the stress switch shown in Figure 5. AC signal remains nearly square up to 50MHz with a ~2.4V swing.

Stress_Clk signal can be held constant at zero or VCC (1.2V). The former is applied during the measurement period to bias V_X at 1.2V, and the latter is used during DC stress measurements. Alternatively, Stress_Clk can swing between these values at frequencies up to 50MHz during a stress period, allowing us to test for the frequency dependency of NBTI degradation (Figure 6). This AC accelerated stress signal is generated by an on-chip ring oscillator to maintain signal integrity. V_{minus} is set at -2V in order to pass the -1.2V V_{stress} signal, due to the fact that PMOS transistors conduct weak low voltages. This setup creates a stress condition of V_{gs} = -2*VCC, which accelerates the NBTI degradation and makes measurement times tractable. However, we can also reduce the voltage stress to monitor the degradation at other biasing conditions. The PMOS biased at V_{minus} is always in strong inversion, so the size of the device stacked above it is skewed up (10µm compared to 0.5µm) in order to drive the internal node voltage (V_X) back up to ~1.2V. The MEAS/STR signal switches between -2V during the stress period and 1.2V when we are taking our measurements (i.e., when the DLL is operating normally).

3.4 Additional System Components

Additional system components are pictured in Figures 7 and 8. The Unstressed Stages in the Bottom DLL are starved inverters driving adjustable capacitance (Figure 7.a). As $V_{control\_bottom}$ drops, the output load of each stage is lowered, thereby decreasing the line delay. The phase comparator asserts equal short duration output pulses for in-phase signals to avoid a dead-band region [17] (Figure 8). An Enable signal was added to the referenced design in order to ensure that neither output is asserted during measurements, which could cause the control voltages to stray from their desired values. In order to take advantage of the short-duration pulses created by the phase comparator for in-phase signals, the charge pump (Figure 7.b) has minimal static phase offset when both input signals from the phase comparator are asserted for equal periods [17].



(a) (b)

Figure 7. Starved inverter used in the bottom VCDL's "Unstressed Stages" (a), charge pump design used in the DLL control circuitry (b) [17].

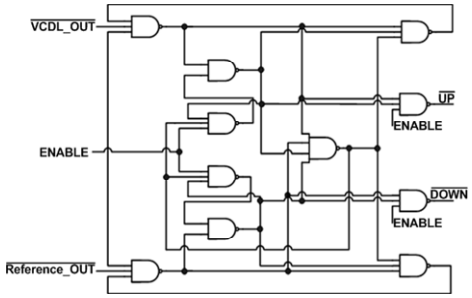


Figure 8. Phase comparator [17], with Enable signal.

3.5 DLL Locking Time and Measurement Delay

Figure 9 demonstrates the ability of the bottom DLL to quickly lock into phase with the Reference CLK after a stress period. We force an initial $V_{control\_bottom}$ value in middle of its anticipated final range to ensure that the DLL locks into the correct frequency. This forced value is gated off automatically when we switch into a measurement period, allowing the control circuitry to determine the final settling value. With the application of proper initial control voltages, locking times are less than 20µs.

4. TEST CHIP MEASUREMENTS

The proposed NBTI sensor was fabricated in a 1.2V, 0.13µm CMOS process. Automated MEAS/STR signal pulses and other control signals were generated with LabVIEW software. This allows us to take fast measurements of $V_{control\_bottom}$ without incurring unwanted recovery in the stressed PMOS devices. A sample-and-hold circuit samples that output signal at the end of the measurement period to ensure a steady reading, even after the NBTI

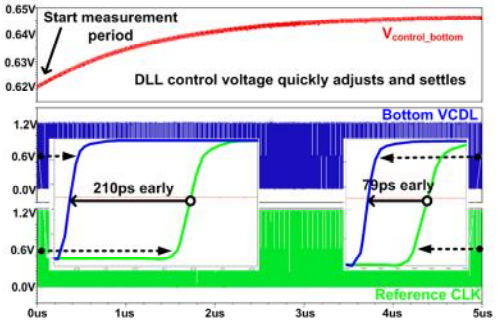


Figure 9. Fast locking action of Bottom DLL (<20µs). Minimal phase offset is observed after the control voltage settles (<80ps delay difference).

stress voltage is reapplied. This enables us to make the measurement period shorter than the reaction time of our measurement equipment, because the sampled value will be available for observation after the test circuit moves back into an accelerated stress state.

Prior to applying NBTI stress, the system is calibrated using a set of variables, including the adjustable number of stages in the Reference CLK delay structure and in the Unstressed Stages of the bottom VCDL. As explained in section 3.2, we find the gain of our measurement system from $\Delta V_{control\_top}$ (and therefore ΔVtp) to $\Delta V_{control\_bottom}$ during calibration by manually adjusting the value of $V_{control\_top}$ and reading out the resulting bottom control voltage. Two example calibration curves are presented in Figure 10.a, and the corresponding gain characteristics are displayed in Figure 10.b. Again, note that we have the ability to place $V_{control\_bottom}$ in the maximum gain region by adjusting the number of Unstressed Stages, as seen in Figure 3.

After measurements are taken, the PMOS threshold degradation is extrapolated from the resulting $V_{control\_bottom}$ curve, and the $\Delta V_{control\_bottom}$ vs. $\Delta V_{control\_top}$ characteristic just described. Two example stress/recovery measurements are presented in Figure 11. During the stress periods, V_{gs} across the stressed PMOS devices was set as indicated in the plot legend, and during recovery, V_{gs} = 0V. Readings were taken during 1ms measurement windows, and faster measurements are possible with high-speed equipment. A threshold degradation of up to 22mV is observed for -2.4V stress, while -2.0V stress results in a 16mV shift in this case. Fast recovery behavior is also apparent. The test chip characteristics are summarized in Table 1, and a chip microphotograph is shown in Figure 12 along with a picture of the measurement lab setup.

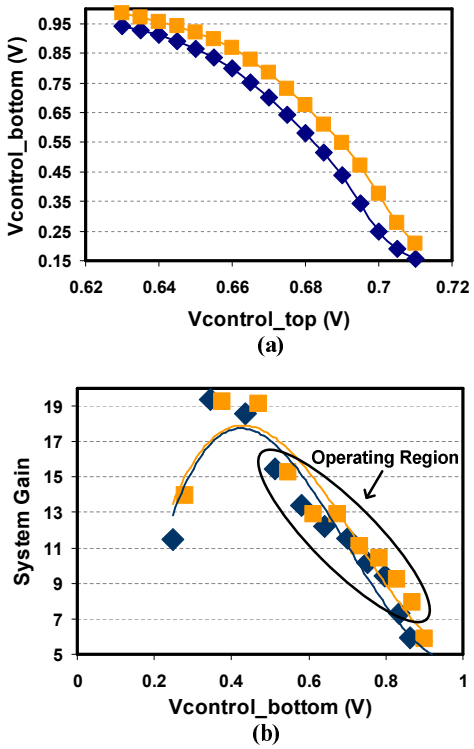


Figure 10. 130nm test chip measurements: (a) the $V_{control\_bottom}$ vs. $V_{control\_top}$ calibration characteristic from two circuit instances; (b) a maximum system gain of 16X was obtained in the operating region (above the threshold voltage of the NMOS devices biased by $V_{control\_bottom}$; see Figure 7.a).

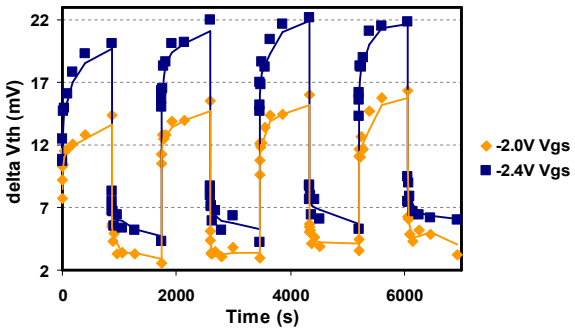


Figure 11. Test chip measurements: Stress/Recovery characteristic for -2V and -2.4V V_{gs} stress. Each measurement shown here was taken during a 1ms window when stress conditions were removed.

5. CONCLUSIONS

Negative Bias Temperature Instability is proving to be a critical reliability issue in nano-scale CMOS technology. Efficient and accurate degradation measurement techniques are therefore in high demand in order to assist in the understanding of this mechanism's effects on real circuits. The knowledge attained through these measurements will allow us to develop accurate models of NBTI degradation, which can be used by designers to mitigate its impact without using costly over-design methods.

In this work, we described an on-chip NBTI degradation sensor using two delay-locked loops. The shift in PMOS threshold voltage due to stress is amplified and translated into the control voltage of one of those DLLs. The proposed measurement system allows us to measure the effects of accelerated DC and AC stress by simply monitoring that control voltage with standard probes. A test chip was fabricated in a 1.2V, 0.13µm CMOS process for concept verification. The hardware implementation demonstrated a system gain from threshold degradation to DLL control voltage of up to 16X in the operating range of interest.

Technology	0.13µm CMOS
Supply	1.2V
Dimensions (2 instances grouped)	545µm x 510µm
Max Sensing Gain (in operating range)	16X

Table 1. Summary of test chip characteristics

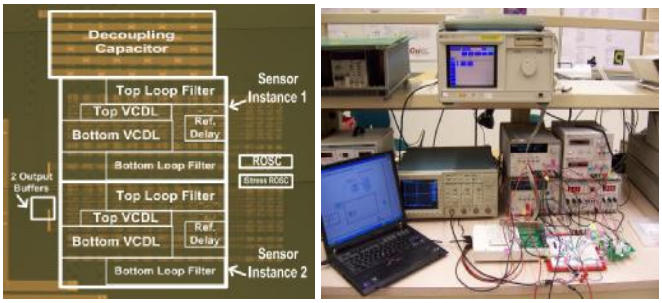


Figure 12. Chip microphotograph and measurement lab setup including LabVIEW software interface

6. ACKNOWLEDGEMENTS

The authors would like to thank Intel and IBM for financial support, as well as United Microelectronics Corporation (UMC) for the foundry design kit and chip fabrication.

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