Width-dependent Statistical Leakage Modeling for Random Dopant Induced Threshold Voltage Shift

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ABSTRACT

Statistical behavior of device leakage and threshold voltage shows a strong width dependency under microscopic random dopant fluctuation. Leakage estimation using the conventional square-root method shows a discrepancy as large as 45% compared to the real case because it fails to model the effective V_T shift in the subthreshold region. This paper presents a width-dependent statistical leakage model with an estimation error less than 5%. Design examples on SRAMs and domino circuits demonstrate the significance of the proposed model.

Categories and Subject Descriptors

B.8.2 [**Hardware**]: Performance and Reliability – *Performance Analysis and Design Aids*

General Terms

Design, Performance

Keywords

Leakage, process variation, random dopant fluctuation

1. INTRODUCTION

Leakage has become one of the major bottlenecks for device scaling in nanometer scale CMOS technologies [1]. Systematic and random process variations also worsen in sub-45nm technologies causing the leakage distribution to become wider. It has been reported that leakage can vary by more than 10X between devices on a same die because of its exponential dependency on threshold voltage (V_T) [2]. The major contributors to intrinsic V_T variations are the doping density variation [3], the gate oxide thickness variation [4], and the device dimension variation [5]. Leakage is also sensitive to environmental factors such as supply voltage and temperature which makes its variation even worse. The intrinsic and environmental leakage variation dictates the amount of power that can be utilized for useful computation which in turn negatively impacts the performance of high-speed VLSI systems.

Leakage and its variation can also cause serious functionality issues in leakage sensitive circuits such as SRAMs and domino gates. SRAM read operation relies on a sufficient on-current to off-current ratio for proper bitline sensing. Increased bitline leakage from the unaccessed cells in large SRAM arrays can lead to a significant bitline delay penalty [6]. In domino circuits, the excessive leakage can cause false evaluations as the keeper may fail to satisfy the robustness requirements under worst-case conditions [7].

To design robust and energy efficient circuits in the presence of large leakage variation, it is crucial for circuit designers to accurately model the statistical leakage behavior. Many mathematical models have been proposed in the past to obtain an accurate leakage distribution based on given process inputs (V_T variation, channel length variation, etc). Chang et al. performed a statistical full-chip leakage analysis considering both inter-die and intra-die spatial correlation using Wilkinson's method [8]. Acar et al. used the inverse gamma distribution to model full-chip leakage distribution and showed a close match between their model and hardware measurements [9]. More recently, Gu, et. al proposed a statistical leakage model for width-quantized FinFET devices [10]. Here, the authors have considered the fact that the number of fins in a single FinFET device affects the leakage modeling results.

An important point that has not been addressed in prior work is the fact that devices with different widths have different V_T means and standard deviations due to the random dopant fluctuation (RDF) within a single device. This so called "random dopant induced V_T shift" has been observed by researchers in the electron devices community through 3D TCAD simulations [11,12]. This phenomenon is due to the following two reasons.

- The placement of dopants is random even within a single device. We refer to this as the "microscopic" RDF. A single device must therefore be regarded as a group of "infinitesimal sub-devices" each having normal V_T distributions.
- Device leakage current is the sum of all the infinitesimal sub-device leakage currents which have a lognormal distribution. The mean and sigma of the sum of lognormal distributions is significantly different from the mean and sigma of the original lognormal distribution.

As a result, a lower mean value and a lower standard deviation value are observed for the V_T of a larger device. Note that the definition of V_T in this discussion is based on the sub-threshold region (i.e. V_{gs} @ I_{ds}=1μA/μm) and not the strong-inversion region (i.e. V_{gs} @ max g_m) [13].

A common way to model the standard deviation for larger devices is using the well-known "square-root method" which states that the standard deviation of V_T is inversely proportional to the square-root of the gate area [14]. However, this method has fundamental limitations. First, the definition of V_T is based on the strong-inversion region and hence the method cannot be applied to estimating leakage distributions which are lognormal variables. Also, it does not account for any spatial correlation within the device [15]. These limitations lead to an inaccurate leakage estimation using the conventional square-root model.

In this work, we propose a simple yet accurate model to account for the random dopant induced V_T shift for statistical leakage estimation. The highlights of this work are as follows.

- For the first time, a statistical leakage model is developed that accounts for the width-dependent V_T shift in CMOS devices caused by microscopic RDF.

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- Unlike previous methods that can only be used for devices with quantized widths, the proposed leakage model can be used for an arbitrary device width. The spatial correlation within a single device can also be handled.
- Estimation accuracies of both the proposed and conventional methods are compared for different device widths, V_T standard deviations, and correlation coefficients.
- Design examples of leakage sensitive circuits using the proposed model are presented.

The organization of this paper is as following. In section 2, the discrepancy between the conventional method and the actual case is discussed to motivate our work. Section 3 proposes a mathematical model to accurately handle the width-dependent leakage and V_T shift. Section 4 presents experimental results to verify the accuracy of the developed model. Design examples of leakage sensitive circuits such as SRAMs and domino circuits are presented in section 5. Finally, section 6 draws a conclusion. A predictive 32nm CMOS technology model was used for this work [16]. It is important to mention that although RDF is assumed to be the major source of variation in this work, the model developed in this paper is actually general to any type of process variation which may include both random and spatial-correlated components.

2. CONVENTIONAL STATISTICAL LEAKAGE MODEL AND ITS LIMITATION

Equation (1) shows the conventional model for statistical V_T estimation which will be referred to as the square-root method. Here, the mean of V_T is a constant and the standard deviation of V_T is inversely proportional to the square-root of the gate area.

$$\mu(V_T) = \text{constant} \qquad \sigma(V_T) \propto \frac{1}{\sqrt{W \cdot L}} \tag{1}$$

Although equation (1) has been widely used as a basis for delay estimation, it cannot properly model the device leakage under the impact of microscopic RDF. To motivate our work, we will first explain why the conventional square-root method fails to capture the actual (golden) case. Fig. 1 (a) shows the simulation setup with progressively sized inverters for the delay and leakage experiments. We assume that the mean and sigma have been given for a reference device with a width of W_0 (60nm) and a channel length of 32nm. The NMOS device of the middle 4x inverter has a width of $4W_0$ and is simulated by putting four reference devices in parallel. The golden results are obtained as described in Fig. 2 by assigning four independent random variables V_T to each reference device to represent the microscopic RDF effect. Monte Carlo simulations are performed in HSPICE to find out the delay and leakage distribution of the middle inverter. The conventional square-root method uses a single effective V_T with the mean and sigma values calculated from equation (1). Leakage variation of the device can be expressed using this single effective V_T as shown in Fig. 2. Monte Carlo simulations were performed in HSPICE for the square-root method as well. Fig. 1(b) and Fig. 1(c) show the simulated results. From Fig. 1 (b), we find that the delay distribution using (1) matches very closely with the golden results. The square-root method was originally developed to model the V_T defined for the strong-inversion current which is a linear combination of the V_T's of sub-devices affected by the microscopic RDF [17]. The concept of sub-devices to account for the RDF inside a larger device is illustrated in Fig. 2 under the golden case. As a result, circuit parameters such as delay which are also approximately a linear function of V_T can be correctly modeled using equation (1). This observation is consistent with the results shown in previous publications [18].

On the other hand, Fig. 1(c) shows a large discrepancy in leakage distributions between the two approaches. The conventional V_T model in equation (1) fails to predict the golden leakage distribution, underestimating the 3σ leakage current by 32%. This tells us that the effective V_T following equation (1) does not work well for estimating the leakage distribution. This discrepancy comes from the fact that leakage current is an exponential function of V_T and therefore the simple solution in equation (1) does not hold true for a sum of lognormal variables considering the microscopic RDF. The above simulation assumes no spatial correlation within a single device. As will be shown in the paper, the conventional scheme shows a poor leakage estimation result when spatial correlation is included.

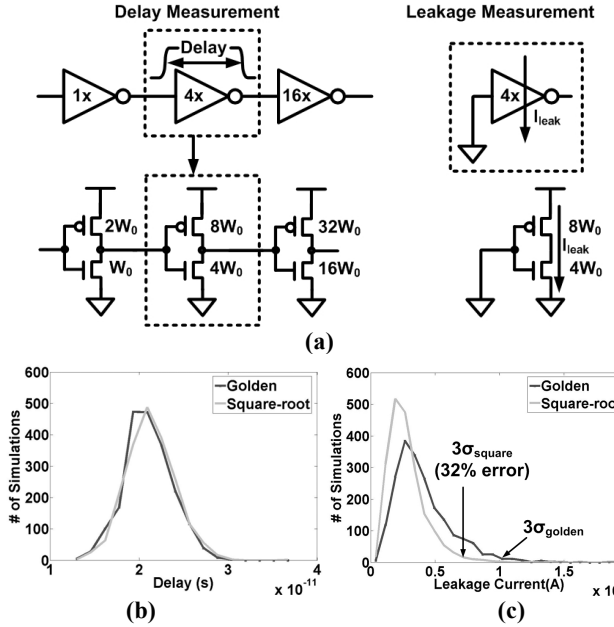

Fig. 1 Comparison between conventional square-root method and the actual (golden) case. (a) Simulation setup; (b) Delay distribution; (c) Leakage distribution.

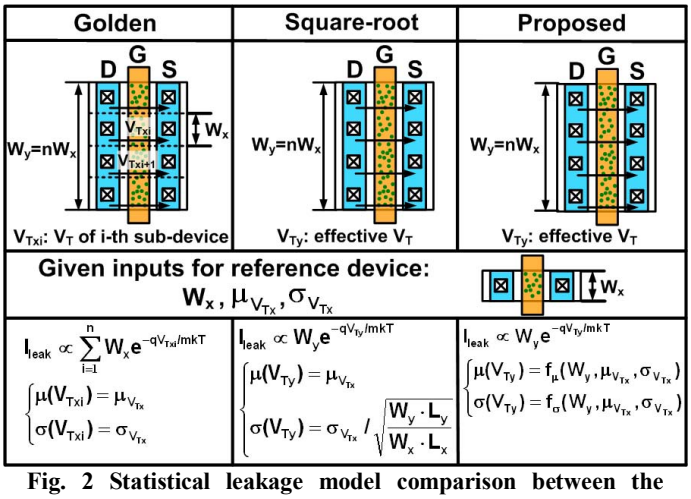

Fig. 2 Statistical leakage model comparison between the golden, square-root method, and proposed method.

Based on the above observations, this paper will focus on developing an accurate leakage distribution model which captures the width-dependent characteristics of the leakage caused by RDF

in a nanoscale CMOS device. One assumption used in this paper is that a large device can be considered as a group of smaller devices by ignoring any fringing effect at the device boundary. This is a reasonable assumption for a relatively large device. For minimum width devices where narrow width effect [19] and other fringing effects may not be ignored, our model can be adjusted to account for those situations. For simplicity, we only consider devices with a fixed minimum channel length in this paper. In a real design, the derived model can be easily expanded to a look-up table for handling circuits with multiple channel lengths.

3. PROPOSED STATISTICAL LEAKAGE MODEL

The goal of a statistical leakage estimation tool is to obtain an accurate leakage distribution of a device, circuit block, or full-chip system based on process inputs such as the V_T mean and V_T sigma of a reference device. Fig. 2 illustrates how the proposed approach is different from the conventional square-root method. Both the proposed and square-root methods introduce an effective V_T to represent the device leakage variation using a single variable. However, unlike the square-root method, the mean and sigma of V_T in the proposed method is expressed as a function of the device width W as well as the two other inputs (mean and sigma of reference device V_T) to match the actual case. The following derivation will show how the actual leakage, which is a sum of lognormal distributions, can be precisely modeled using a single effective V_T parameter with a new mean and sigma.

Leakage current of a MOSFET can be expressed as:

$$I_{leak} \propto We^{-V_T/(mkT/q)}(1-e^{-V_{ds}/(kT/q)}) \cong We^{-B\cdot V_T} \quad (2)$$

where m is the subthreshold slope coefficient, q is the electron charge, T is the temperature, and k is the Boltzmann's constant. The term $e^{-V_{ds}/(kT/q)}$ can be ignored as V_{ds} is greater than 3kT/q which is 78mV at room temperature. For simplicity, a constant B is used to represent q/mkT in the following derivation. V_T is a Gaussian variable determined by the effective length L_{eff}, dopant concentration N_d, oxide thickness T_{ox}, etc. In this work, we also consider the correlation between the V_T of any two devices.

The problem can be now formulated as: *Given the mean $\mu_{V_{Tx}}$ and sigma $\sigma_{V_{Tx}}$ of V_T for a reference device having a width of W_x, find the mean and sigma value of the effective V_T for a device with width W_y that matches the actual (golden) case given in Fig. 2.* We will first derive a leakage model assuming an integer multiplicative factor between W_y and W_x, i.e. $W_y=nW_x$. We will later extend the model to a rational number multiplicative factor case in section 3.2.

3.1 Leakage model for discrete width multiplication ($W_y=nW_x$, n: integer)

Let V_{Ty} be the effective V_T of a device with a width of W_y. $\mu_{V_{Tx}}$ and $\sigma_{V_{Tx}}$ are given parameters where V_{Tx} is the V_T of a reference device with a width of W_x. The total device leakage can be expressed as:

$$\sum_{i=1}^{n} W_x e^{-B\cdot V_{Tx_i}} = W_y e^{-B\cdot V_{Ty}}. \quad (3)$$

W_y is equal to nW_x and V_{Tx_i} represents the V_T of each reference sub-device considering the microscopic RDF. The mean and sigma of V_{Ty} in equation (3) can be expressed using the mean and sigma of V_{Tx} using Wilkinson's method which shows that a sum of lognormal variables can be approximated to another lognormal variable [20]. For simplicity, we define (μ_x, σ_x) as the mean and sigma of the reference device Gaussian variables $(-B\cdot V_{Tx_i})$ and (μ_y, σ_y) as those of the total device Gaussian variable $(-B\cdot V_{Ty})$ in equation (3). We also assume that a correlation coefficient r_x between two reference device Gaussian variables $(-B\cdot V_{Tx_i})$ is given to model the spatial correlation. Wilkinson's method allows us to equate the first moment and second moment of the two lognormal expressions in equation (3) as follows:

$$u_1 = E(S) = \sum_{i=1}^{n} e^{\mu_x+\sigma_x^2/2} = ne^{\mu_x+\sigma_x^2/2} = ne^{\mu_y+\sigma_y^2/2}$$
$$u_2 = E(S^2) = \left(\sum_{i=1}^{n} e^{2\mu_x+2\sigma_x^2} + 2\sum_{i=1}^{n-1}\sum_{j=i+1}^{n} e^{2\mu_x} e^{(2\sigma_x^2+2r\sigma_x^2)/2}\right) \quad (4)$$
$$= ne^{2\mu_x+\sigma_x^2}(e^{\sigma_x^2} + (n-1)\cdot\sigma^{r_x\sigma_x^2}) = n^2 e^{2\mu_y+2\sigma_y^2}$$

Solving equation (4), we find the following relationship:

$$\mu_y = \mu_x + \frac{1}{2}\Delta \quad (5)$$
$$\sigma_y^2 = \sigma_x^2 - \Delta$$

where $\Delta = \sigma_x^2 - \ln\left(\frac{e^{\sigma_x^2} + (n-1)\cdot e^{r_x\sigma_x^2}}{n}\right)$. Δ is a non-negative number. By plugging in the constant B, we obtain the following relationship between the V_{Tx} and V_{Ty}:

$$\mu_{V_{Ty}} = \mu_{V_{Tx}} - \frac{1}{2}\Delta/B \quad (6)$$
$$\sigma_{V_{Ty}}^2 = \sigma_{V_{Tx}}^2 - \Delta/B^2$$

where $\Delta = B^2\sigma_{V_{Tx}}^2 - \ln\left(\frac{e^{B^2\sigma_{V_{Tx}}^2} + (n-1)\cdot e^{r_x B^2\sigma_{V_{Tx}}^2}}{n}\right)$.

Equation (6) shows that the mean value of the effective V_T is reduced by $\frac{1}{2}\Delta/B$, which is consistent with our observation in Fig. 1(c) showing that the golden case has a higher average leakage compared to results from the conventional square-root method. The sigma value goes down according to (6) following a similar trend as the square-root method but giving a closer match with the golden case.

Note that the correlation coefficient r_y between V_{Ty} of two devices is no longer equal to the r_x value of the reference device because the device dimensions have changed. An expression for r_y is needed to extend the model for the continuous width multiplication case in section 3.2. Hence, we show the derivation of r_y in the remainder of this section. Leakage currents of two new devices with equal sizes can be described as:

$$\sum_{i=1}^{n} W_x e^{-BV_{Tx1_i}} = W_y e^{-BV_{Ty1}} \quad (7)$$
$$\sum_{i=1}^{n} W_x e^{-BV_{Tx2_i}} = W_y e^{-BV_{Ty2}}.$$

In order to find the correlation coefficient r_y between V_{Ty1} and V_{Ty2}, we can equate the correlation coefficient of the left-hand sides to that of the right-hand sides in (7). First of all, the correlation coefficient of the right-hand sides of (7) is:

$$r(W_y e^{-BV_{Ty1}}, W_y e^{-BV_{Ty2}}) = \frac{E(W_y e^{-BV_{Ty1}}\cdot W_y e^{-BV_{Ty2}}) - E(W_y e^{-BV_{Ty1}})\cdot E(W_y e^{-BV_{Ty2}})}{\sigma(W_y e^{-BV_{Ty1}})\cdot\sigma(W_y e^{-BV_{Ty2}})} \quad (8)$$
$$= \frac{e^{r_y B^2\sigma_{V_{Ty}}^2} - 1}{e^{B^2\sigma_{V_{Ty}}^2} - 1}$$

Secondly, the correlation coefficient of the left-hand sides of (7) is:

$$r(\sum_{i=1}^{n} W_x e^{-BV_{Tx1_i}}, \sum_{i=1}^{n} W_x e^{-BV_{Tx2_i}}) = \frac{E(\sum_{i=1}^{n} W_x e^{-BV_{Tx1_i}} \cdot \sum_{i=1}^{n} W_x e^{-BV_{Tx2_i}}) - E(\sum_{i=1}^{n} W_x e^{-BV_{Tx1_i}}) \cdot E(\sum_{i=1}^{n} W_x e^{-BV_{Tx2_i}})}{\sigma(\sum_{i=1}^{n} W_x e^{-BV_{Tx1_i}}) \cdot \sigma(\sum_{i=1}^{n} W_x e^{-BV_{Tx2_i}})} \quad (9)$$

$$= \frac{e^{r_x B^2 \sigma^2_{V_{Tx}}} - 1}{\frac{e^{B^2 \sigma^2_{V_{Tx}}} + (n-1)e^{r_x \sigma^2_{V_{Tx}}}}{n} - 1}$$

By equating (8) and (9) and plugging in the relationship between $\sigma_{V_{Tx}}$ and $\sigma_{V_{Ty}}$ in (6), we find that:

$$r_y = \frac{B^2 \sigma^2_{V_{Tx}}}{\ln \frac{e^{B^2 \sigma^2_{V_{Tx}}} + (n-1)e^{r_x B^2 \sigma^2_x}}{n}} \cdot r_x = \frac{\sigma^2_{V_{Tx}}}{\sigma^2_{V_{Ty}}} \cdot r_x \quad (10)$$

One can also easily prove that $1 \geq r_y \geq r_x$ and that $r_y=1$ only when $r_x=1$. Equation (10) shows an interesting observation. As devices become larger, the correlation coefficient between V_T of the devices also increases. This is because as dimensions increase, the uncorrelated variation components quickly average out leaving only the correlated variation components to appear in the overall leakage distribution.

3.2 Leakage model for continuous width multiplication ($W_y=\alpha W_x$, α: positive rational number)

Wilkinson's method cannot be directly applied to solve for the continuous width case: i.e. *given $\mu_{V_{Tx}}$ and $\sigma_{V_{Tx}}$ of V_{Tx} for a device with width W_x, find the $\mu_{V_{Ty}}$ and $\sigma_{V_{Ty}}$ of V_{Ty} for a device with width W_y where $W_y=\alpha W_x$ and α is a positive rational number.*

To solve this problem, we assume there exists a virtual reference device with width W_0 that satisfies both $W_x=mW_0$ and $W_y=nW_0$. Note that α becomes n/m. $\mu_{V_{T0}}$, $\sigma_{V_{T0}}$, and r_0 denote the mean, standard deviation, and correlation coefficient of V_T for the small virtual device. Now we can utilize the results from section 3.1 to carry out our derivation. From equation (6), we have:

$$\mu_{V_{Tx}} = \mu_{V_{T0}} - \frac{1}{2}\Delta_x / B \quad (11)$$
$$\sigma^2_{V_{Tx}} = \sigma^2_{V_{T0}} - \Delta_x / B^2$$

where $\Delta_x = B^2 \sigma^2_{V_{T0}} - \ln(\frac{e^{B^2 \sigma^2_{V_{T0}}} + (m-1) \cdot e^{r_0 B^2 \sigma^2_{V_{T0}}}}{m})$ and also:

$$\mu_{V_{Ty}} = \mu_{V_{T0}} - \frac{1}{2}\Delta_y / B \quad (12)$$
$$\sigma^2_{V_{Ty}} = \sigma^2_{V_{T0}} - \Delta_y / B^2$$

where $\Delta_y = B^2 \sigma^2_{V_{T0}} - \ln(\frac{e^{B^2 \sigma^2_{V_{T0}}} + (n-1) \cdot e^{r_0 B^2 \sigma^2_{V_{T0}}}}{n})$.

Solving equations (11) and (12) and applying results from equation (10), we finally find the relationship:

$$\mu_{V_{Ty}} = \mu_{V_{Tx}} - \frac{1}{2}\Delta / B \quad (13)$$
$$\sigma^2_{V_{Ty}} = \sigma^2_{V_{Tx}} - \Delta / B^2$$

where $\Delta = B^2 \sigma^2_{V_{Tx}} - \ln(\frac{e^{B^2 \sigma^2_{V_{Tx}}} + (\alpha-1) \cdot e^{r_x B^2 \sigma^2_{V_{Tx}}}}{\alpha})$. Similarly, we get:

$$r_y = \frac{B^2 \sigma^2_{V_{Tx}}}{\ln \frac{e^{B^2 \sigma^2_{V_{Tx}}} + (\alpha-1)e^{r_x B^2 \sigma^2_x}}{\alpha}} \cdot r_x = \frac{\sigma^2_{V_{Tx}}}{\sigma^2_{V_{Ty}}} \cdot r_x \quad (14)$$

Equations (13) and (14) have the exact same format as equations (6) and (10). This tells us that the same formulas can be applied to both discrete and continuous width cases. Although we started our derivation using a small reference device with a width of Wx, equations (13) and (14) can be used to relate the V_T characteristics between any two devices with arbitrary widths, i.e. α can be either larger than 1 or smaller 1. In other word, the derived model can accurately estimate the leakage distribution of an arbitrary width device based on given process inputs for a reference device with any width value. Note that the above derivation is not specific to a certain type of variation. Therefore, the proposed model is general to any process variation sources although RDF is considered as the major cause of variation in this work. The next section will prove the accuracy of the proposed model in (13) and (14).

4. EXPERIMENTAL RESULTS

Monte Carlo simulations were performed to compare the proposed model with the conventional square-root method. The mean and standard deviation values of the reference device were given and multiple reference devices were combined to form a larger device. This setup allows us to verify the leakage distribution for the discrete width multiplication case. Due to the lack of TCAD tools to model the RDF induced V_T shift for the continuous width multiplication case, we simply extrapolate the results from the discrete case to a continuous case. Both the theoretical analysis and simulation results exhibit no distinction between the continuous and discrete width multiplication cases.

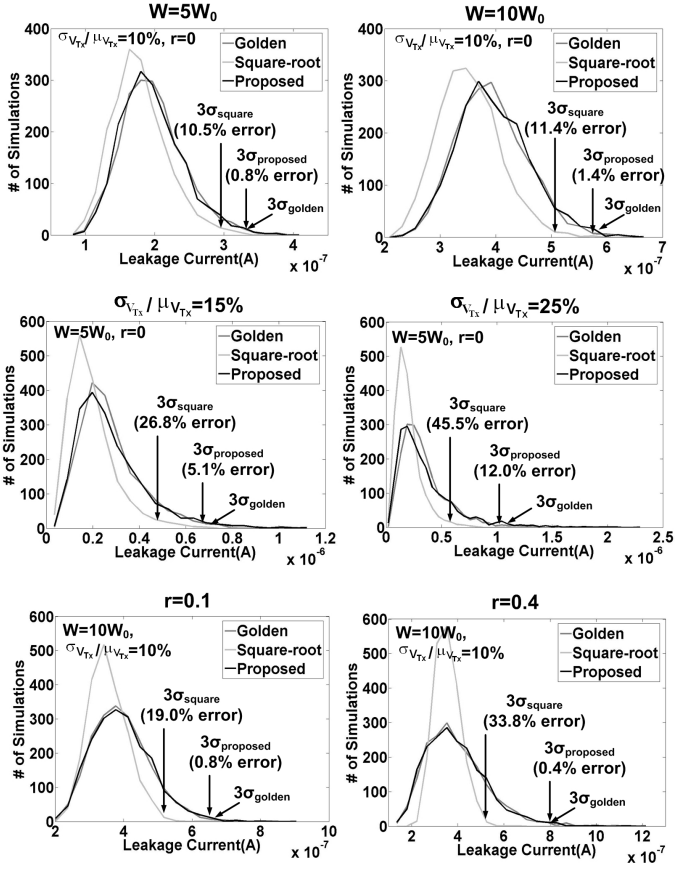

Fig. 3 Statistical leakage estimation results for the golden case, conventional method, and proposed method. (top row: different device widths, middle row: different sigma values, bottom row: different correlation coefficients).

Fig. 3 shows the leakage distribution comparisons for different widths, different V_T sigma's, and different correlation coefficients. The proposed method is compared to the conventional square-root method as well as the golden method. 3σ points on the leakage distributions are marked as a measure of the estimation error. Our proposed method shows a much closer match (less than 5% in most cases) with the golden results while the conventional square-root method exhibits discrepancies as large as 45%. Note that a slightly larger error (12%) is observed for our proposed method when the sigma of the reference device V_T is high (Fig. 3, middle right). This stems from the increased error in the Wilkinson's approximation for Gaussian variables with large standard deviations as mentioned in [20]. Even with this error due to the limitation of Wilkinson's method, the proposed method still shows a much better fit than the square-root method. Since the intra and inter-die V_T variation is normally controlled well below 30%, our model is capable of generating accurate results in a realistic CMOS process.

Fig. 4 shows the estimated mean and sigma values of the effective V_T for a continuous range of device widths. For larger devices, the mean value of the effective V_T estimated by the proposed method is significantly less than that predicted by the square-root method. The difference between the estimated sigma values was less significant. This observation is consistent with what was reported in [11]. Our model summarized in (13) explains the statistical reason behind these physical observations and provides a solution for accurate estimation.

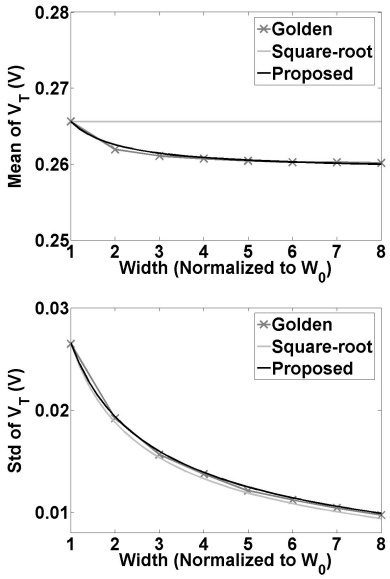

Fig. 4 Estimated mean (top) and standard deviation (bottom) of effective V_T versus normalized device width.

5. DESIGNING LEAKAGE SENSITIVE CIRCUITS USING PROPOSED MODEL

As mentioned in the introduction, accurate device leakage modeling is important for estimating the chip power consumption, but is also crucial for optimal design of leakage sensitive circuits such as SRAMs and domino circuits. This section shows design examples using the proposed leakage model for high performance circuits in nanometer CMOS technologies.

5.1 SRAM design: Bitline leakage problem

Bitline leakage from unaccessed cells in SRAM bitlines has been recognized as a major cause of read failure in low voltage SRAMs [6]. Fig. 5(a) illustrates the worst-case situation where the bitline leakage causes significant increase in read access delay. Suppose the SRAM cell being accessed stores a '1' and all the other cells attached to the same bitline contain a '0'. While $\overline{BL}$ is being discharged by the read current of the accessed cell, BL can also be discharged by the leakage from the unaccessed cells. The read access time increases compared to a situation without any bitline leakage because it takes a longer time for a sufficient BL and $\overline{BL}$ voltage difference to build up. Fig. 5(b) shows the BL and $\overline{BL}$ waveforms during the read access where the bitline sensing delay is increased from 0.35ns to 0.51ns due to the bitline leakage. In the worst case, a faulty read may occur due to an extraordinarily large bitline leakage: i.e. BL may discharge faster than $\overline{BL}$ in the given example. A statistical analysis on the SRAM bitline delay has to be correctly performed to design SRAMs with high tolerance to the bitline leakage problem.

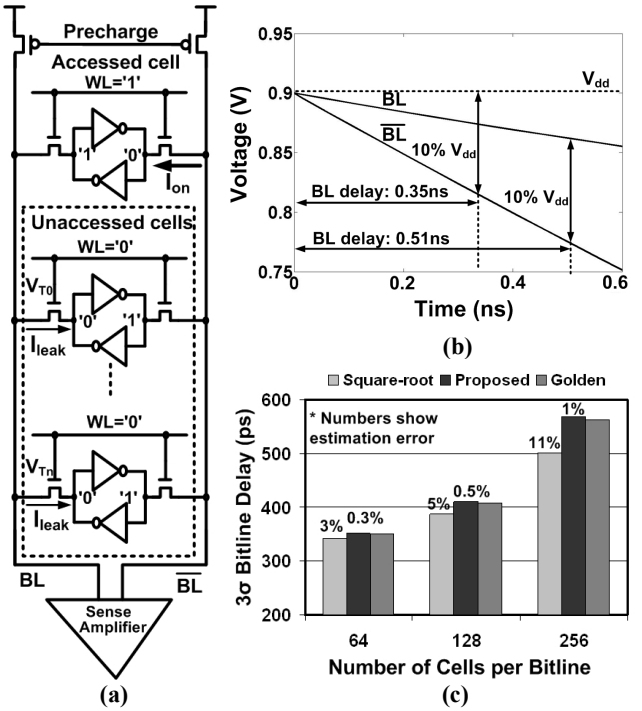

Fig. 5 SRAM bitline leakage problem and accurate bitline delay modeling using proposed method. (a) Schematic of SRAM bitline illustrating bitline leakage problem; (b) waveforms of bitlines during read access; (c) estimated 3σ value of bitline delay for different approaches.

The statistical leakage model developed in this paper can be used to accurately estimate the SRAM bitline leakage and the bitline delay distribution. To test the proposed model, we built SRAM bitlines with different number of cells attached (i.e. 64, 128, and 256). The access transistors of the unaccessed SRAM cells were lumped into a single large NMOS device whose width that can be then expressed as a multiple of the reference device width W_0. V_T of the reference devices was assumed to have a sigma of 15%. Monte Carlo simulations were performed to obtain the bitline delay defined as the time for BL and $\overline{BL}$ to develop a voltage difference of 10%·V_{dd}. Fig. 5(c) shows the 3σ bitline delay for different number of cells per bitline. The estimation error is shown on top of the bars for the square-root method and proposed method. As the bitline length increases, the estimation error of the conventional approach also increases and becomes as large as 11% while our proposed method maintains a high accuracy with less than 1% error.

5.2 Domino circuits: Keeper design

The exponential increase in leakage with process scaling has a detrimental impact on domino gate performance and noise margin. As shown in Fig. 6(a), a static keeper is used to hold the dynamic node to high when none of the pull-down paths are evaluating. However, a large pull-down leakage can accidentally discharge the dynamic node voltage causing a non-recoverable false transition in the output. Optimal sizing of keeper is important because an over-sized keeper impacts the evaluation speed while an undersized keeper results in an insufficient noise margin [7]. Our proposed model can be used to estimate the pull-down leakage distribution and find out the optimal keeper size to maintain a sufficient noise margin. Fig. 6(b) shows the simulated keeper sizes to achieve a target 3σ SNM of 15%·V_{dd}. Here, SNM is defined as the DC input voltage to the pull-down network that will cause an equal rise in the domino gate output voltage. Fig. 6(b) shows that due to the underestimation of leakage, the keeper sized based on the conventional method cannot meet the target SNM. The proposed approach, on the other hand, suggests the precise keeper sizes to meet the SNM requirement.

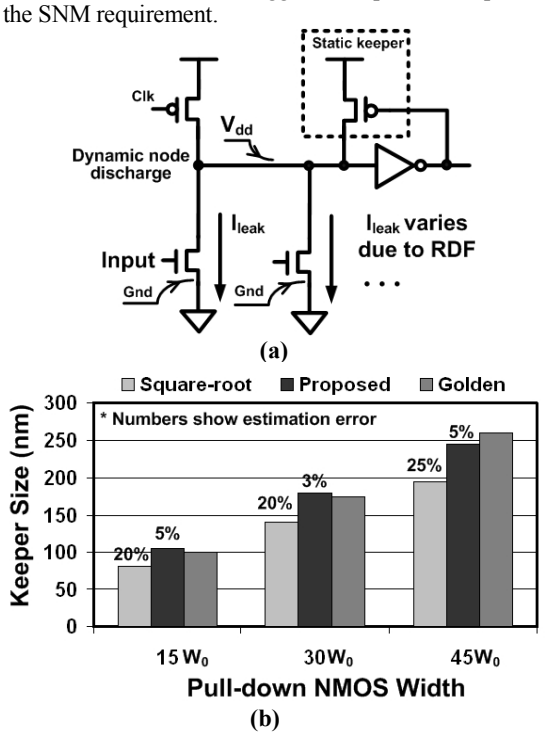

Fig. 6 Domino circuit keeper sizing using proposed model. (a) Circuit schematic; (b) keeper sizing based on different approaches to maintain a target 3σ SNM of 15%·V_{dd}.

6. CONCLUSIONS

A precise statistical leakage model is indispensable in modern VLSI design because the leakage variation not only leads to unpredictable power consumption and system performance but also holds serious threat to the circuit functionality. Statistically, leakage and V_T of an individual device has a strong dependency on the device width due to microscopic RDF. In this paper, we show that the conventionally used square-root model is inaccurate due to its incorrect modeling of the sum of lognormal distributions. Moreover, the previous method is not capable of handling leakage variation with spatial correlation. We propose an analytical formula that can model the width-dependent V_T shift for continuous device widths including spatial correlation. Monte Carlo simulations are performed to verify the accuracy of the proposed model. Results show that the conventional square-root method can have an estimation error greater than 45% while the proposed method has an error below 5%. Application of our models on leakage sensitive circuits such as SRAM and domino circuits are presented. Simulations show that designs based on the conventional approach can fail to meet the performance or noise margin goals due to the underestimated leakage. On the other hand, the bitline delay and domino gate robustness are accurately characterized using the proposed method.

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