An 8T Subthreshold SRAM Cell Utilizing Reverse Short Channel Effect for Write Margin and Read Performance Improvement

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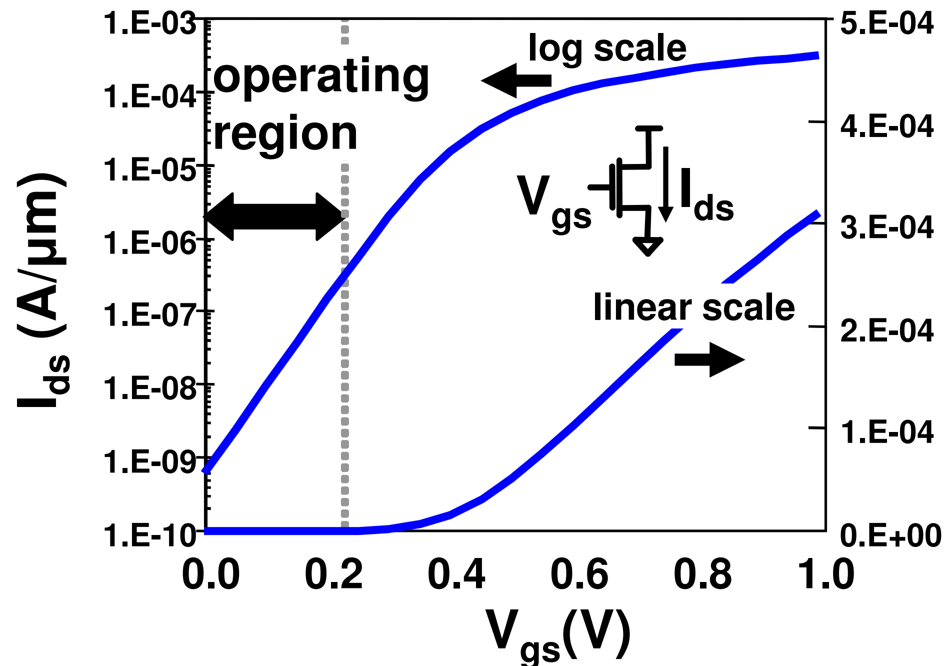
Subthreshold Operation



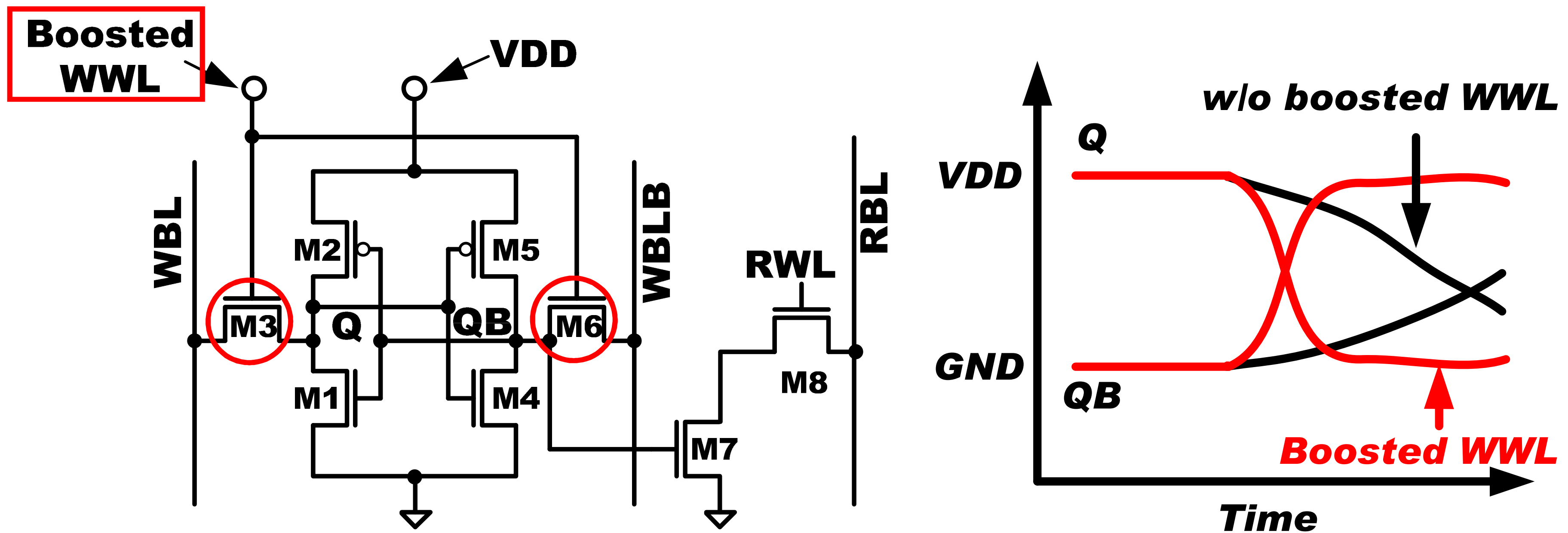
- **Main Benefit**
  - Super-linear power savings

$$P_{total} = \alpha \cdot f \cdot C \cdot V_{dd}^{2} + I_{leak} \cdot V_{dd}$$

  - Minimum energy solution for low-performance designs

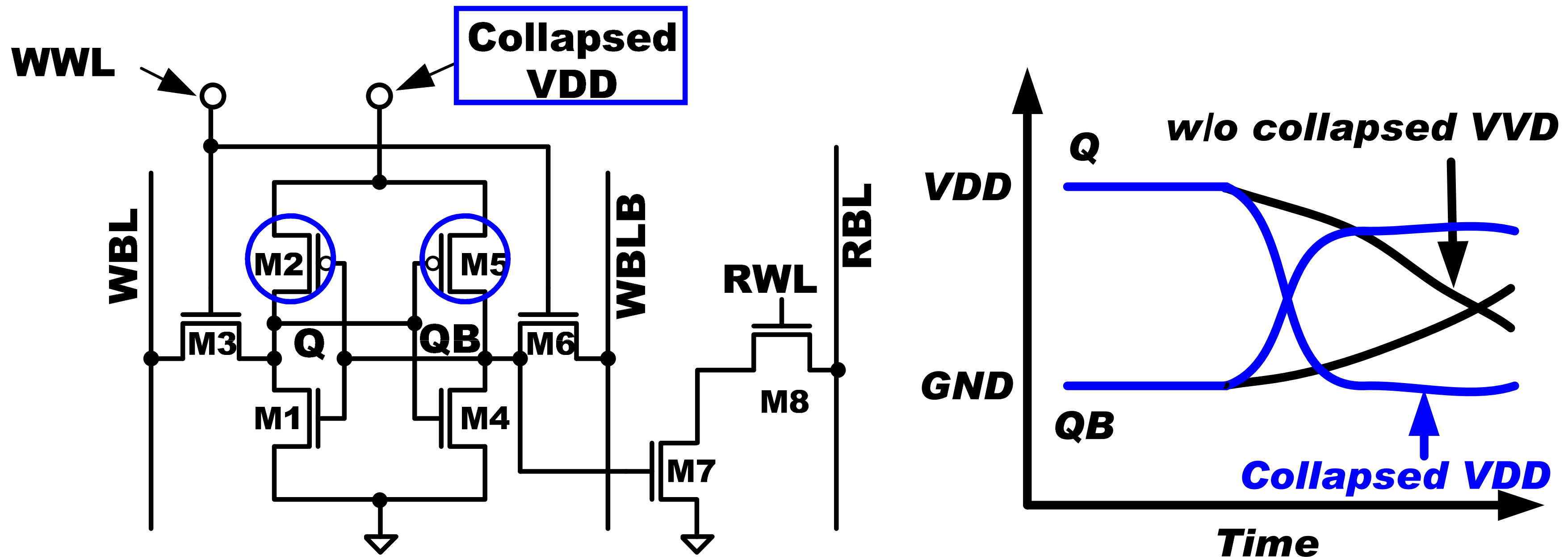
- **Limitations**
  - PVT variation
  - Interconnect delay
  - Lack of a systematic design methodology

Conventional Write Margin Improvement Technique



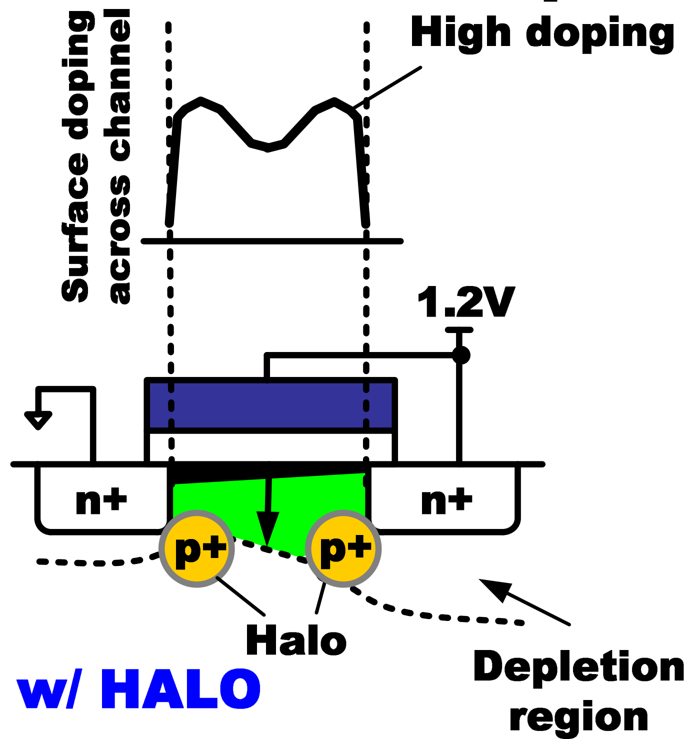
- Boosted wordline voltage to strengthen write path (M3, M6)
- Power consumption and circuit area overhead

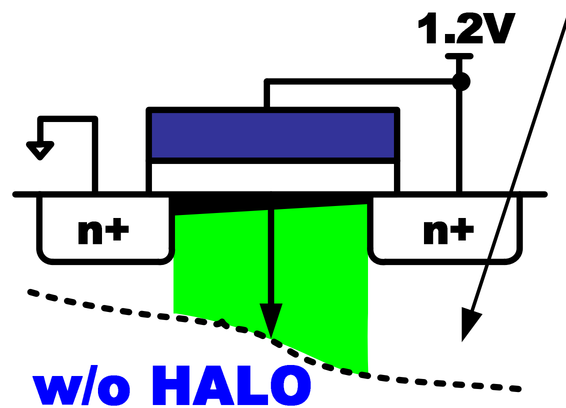
Conventional Write Margin Improvement Technique

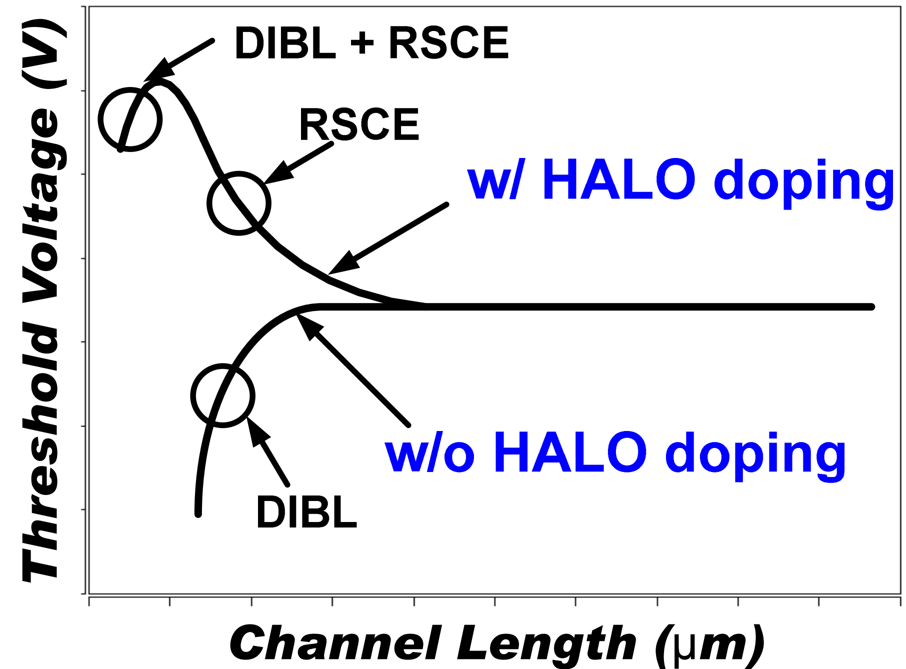


- Collapsed VDD to weaken pull-up PMOS (M2,M5)
- Stability problem in shared cells

HALO Impact in Superthreshold

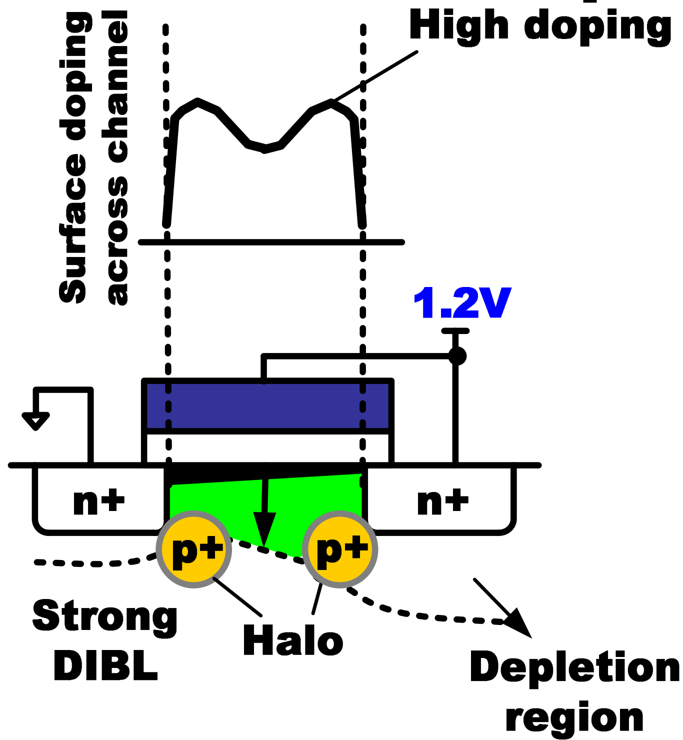


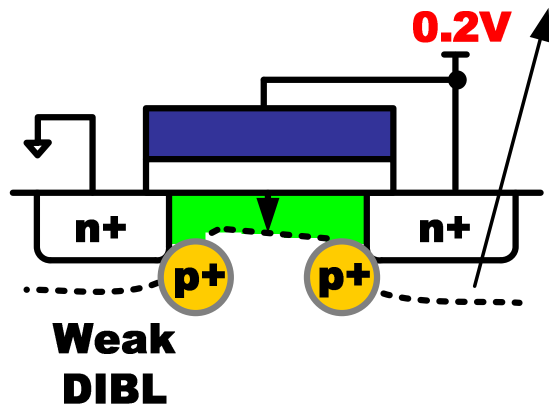


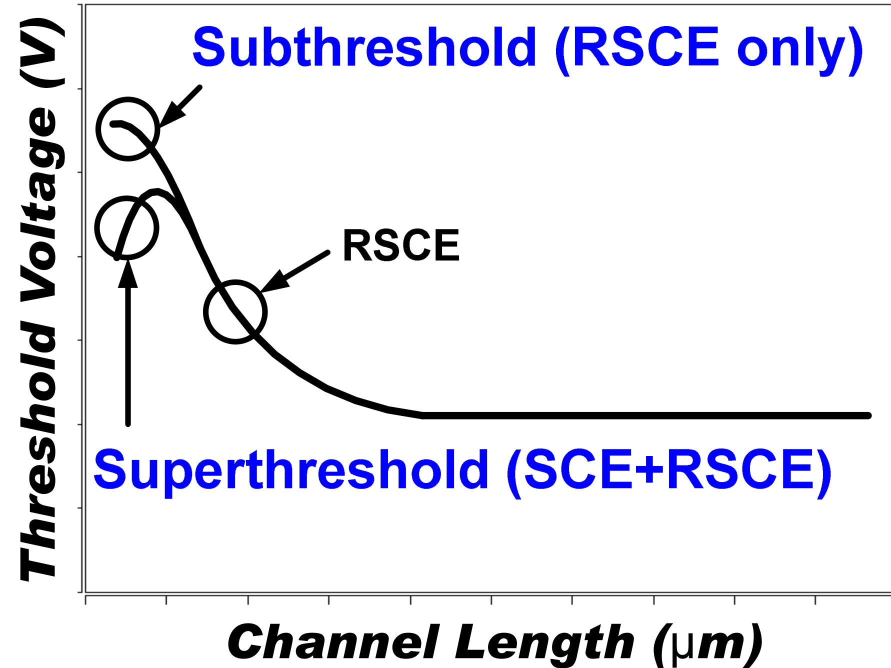


- HALO pocket implants used to mitigate the Short Channel Effect (SCE)
- Reverse Short Channel Effect (RSCE) observed due to HALO

HALO Impact in Subthreshold

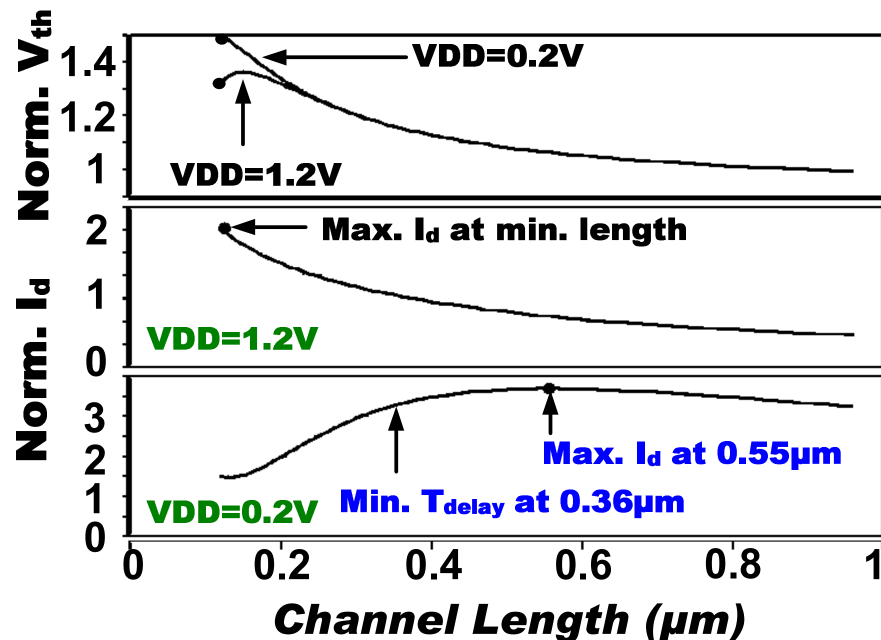


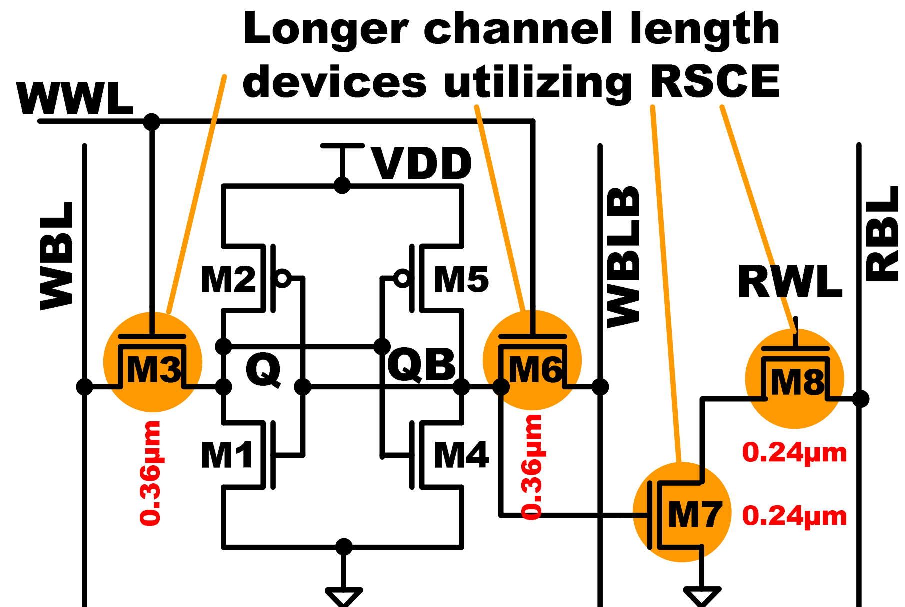




- SCE significantly reduced in the subthreshold region
- Only the RSCE is observed in subthreshold

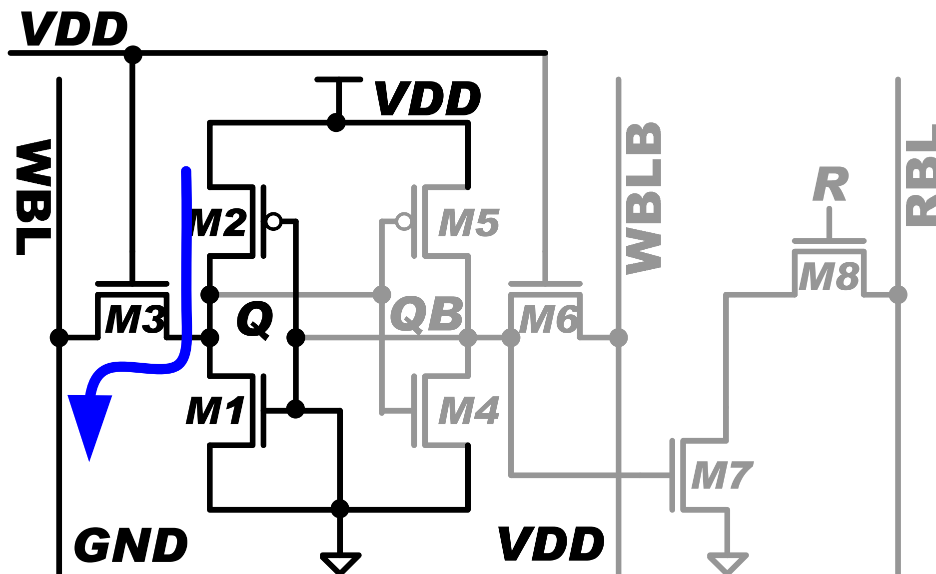
Proposed 8T SRAM Design for Noise Margin Improvement

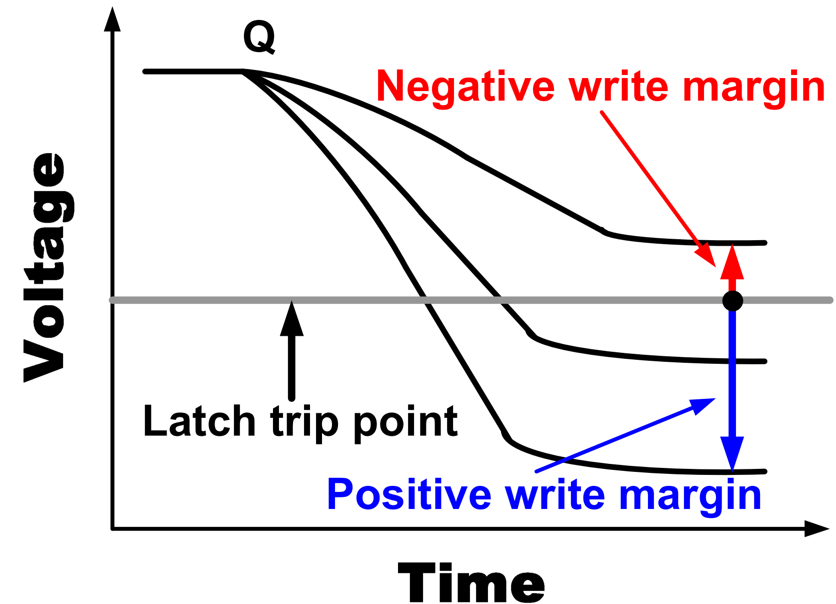




- Utilizing RSCE in write port and read port
- Increase current drivability and bitline Ion-to-Ioff ratio
- No additional circuitry or power

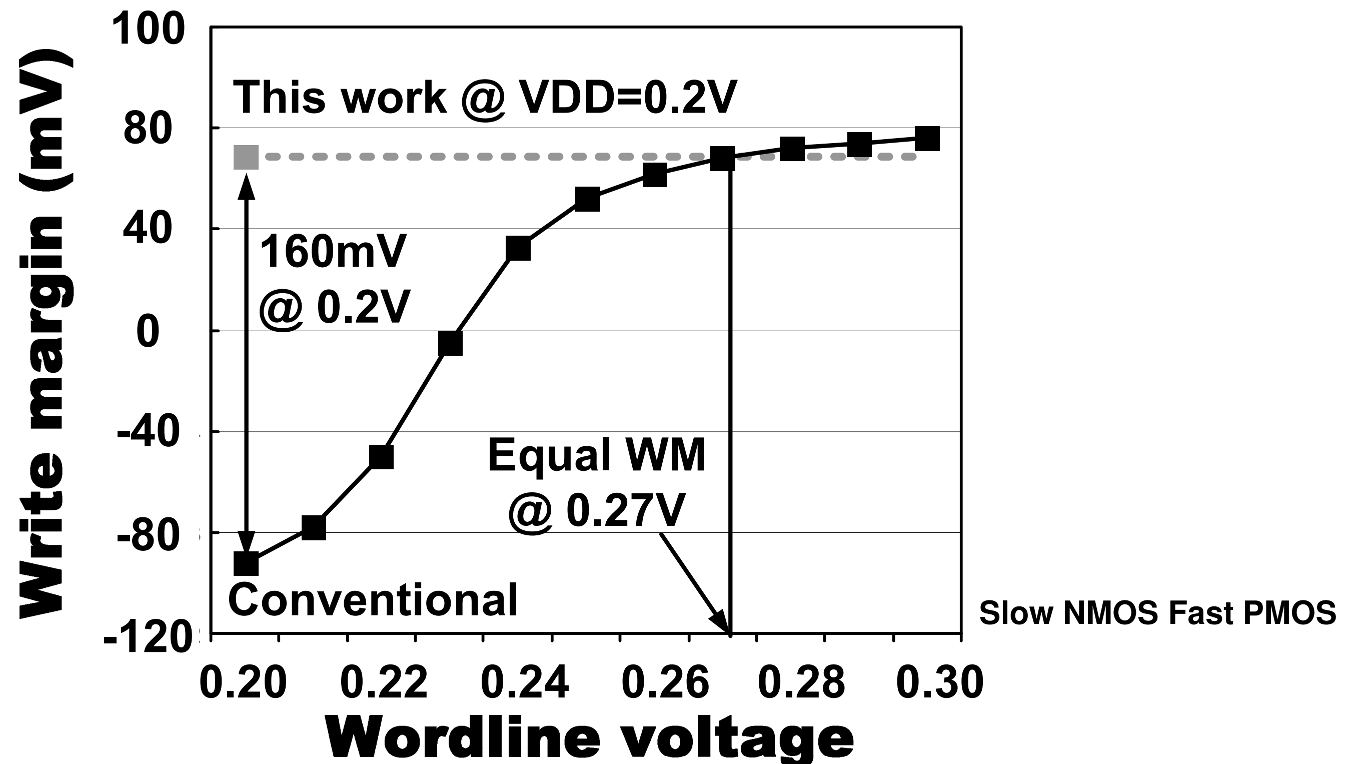
Write Margin Metric





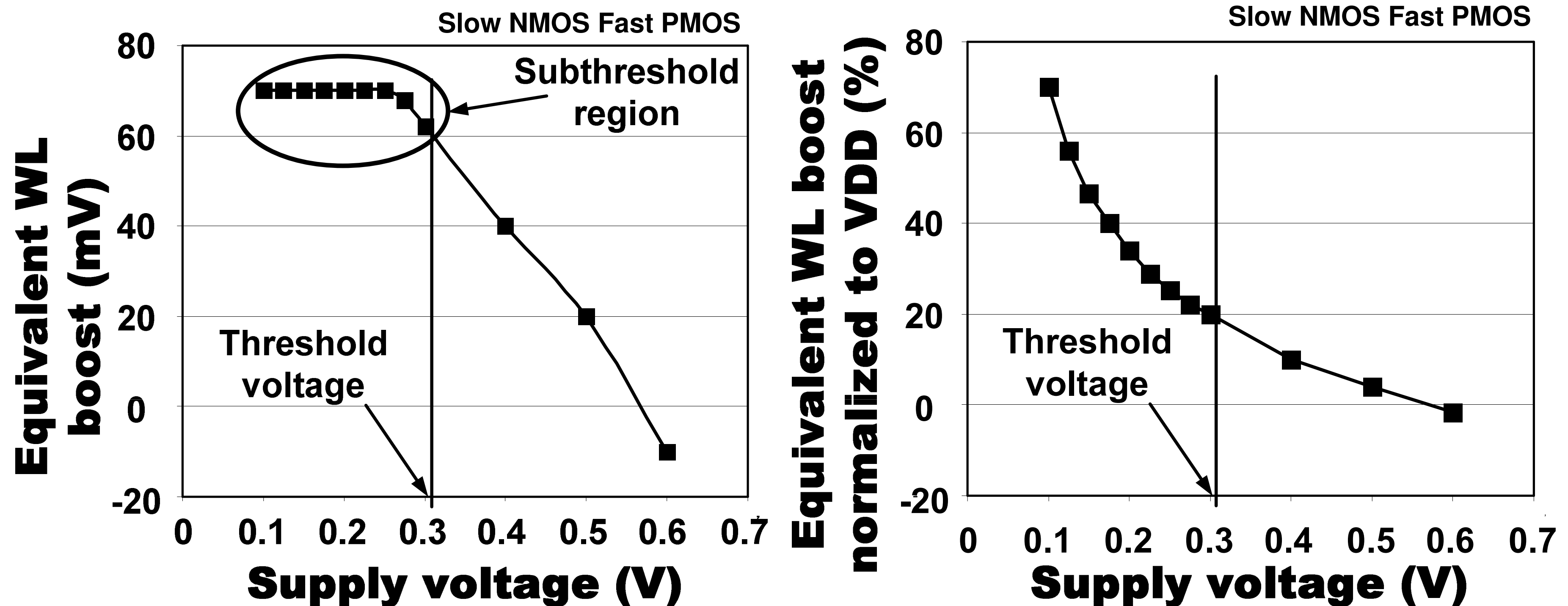
- Half circuit showing the worst case write ‘0’
- Write margin = latch trip point – voltage at Q
- Negative write margin representing write failure

Write Margin Simulation Results



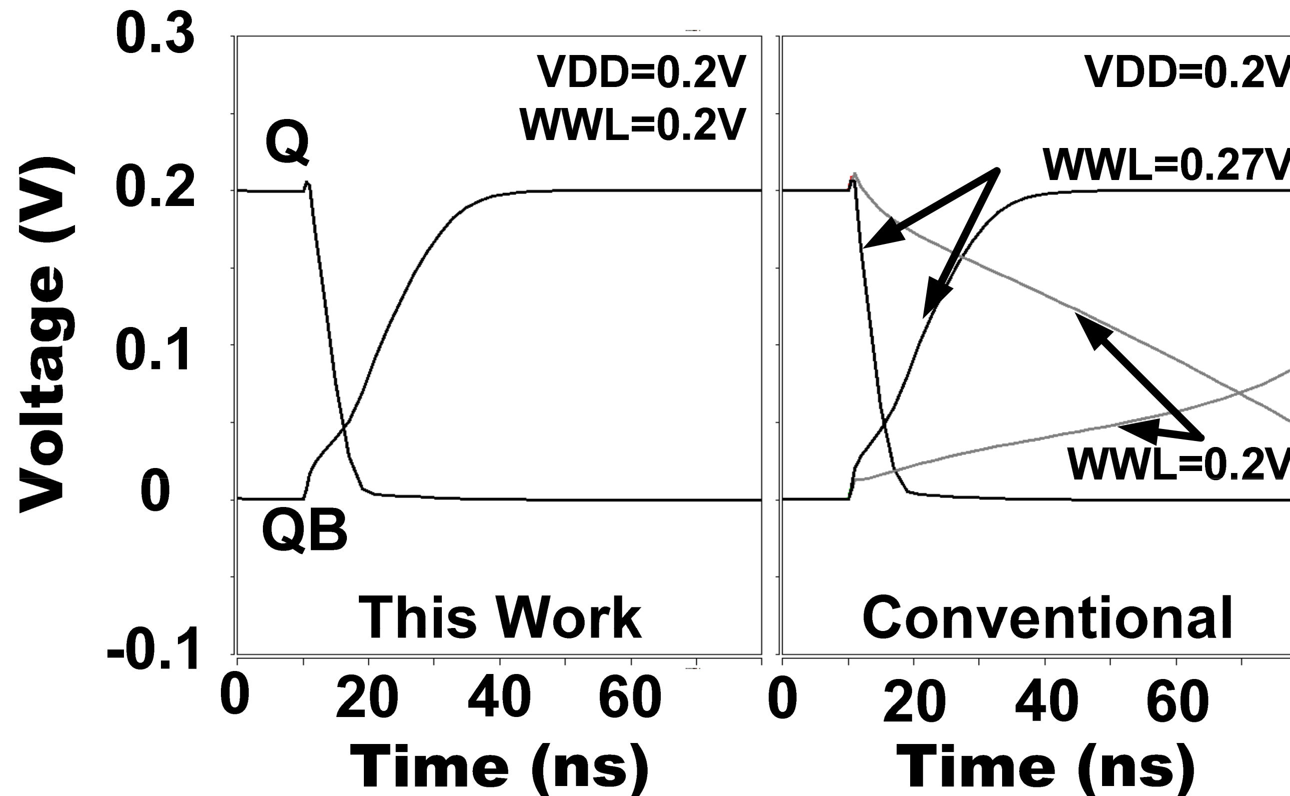
- Write margin improved by 160mV at 0.2V
- Equivalent boosted wordline voltage of 0.27V
- Technique more efficient at lower voltages

Write Margin Simulation Results



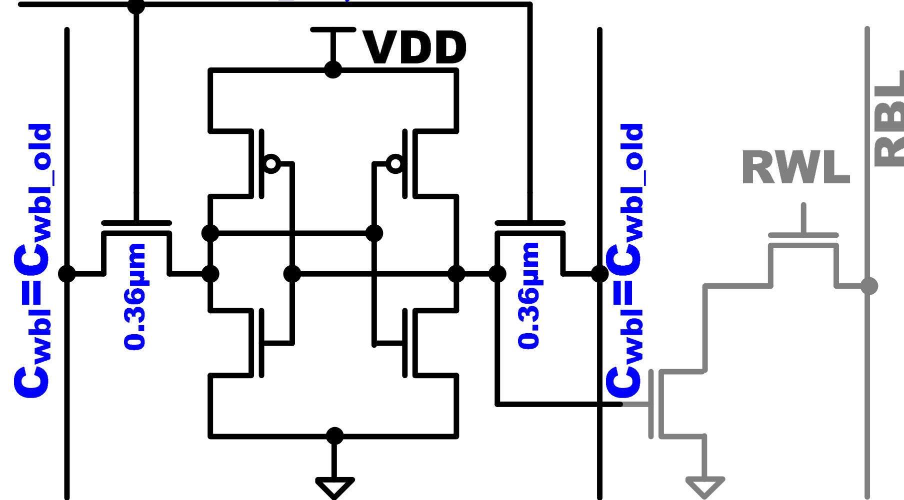
- Strong RSCE effect in subthreshold region
- Larger equivalent WWL boost in lower supply voltage

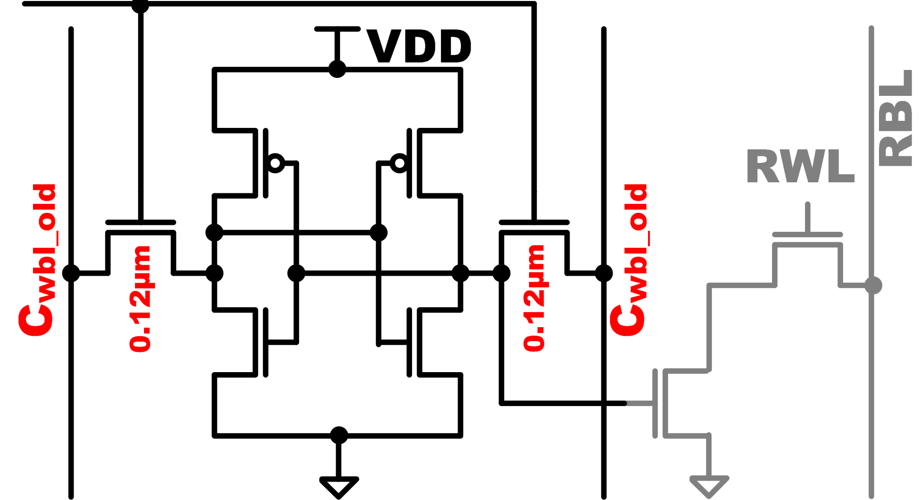
Write Margin Simulation Results



- Equivalent boosted wordline voltage of 0.27V
- Improved write speed due to the increased current drivability

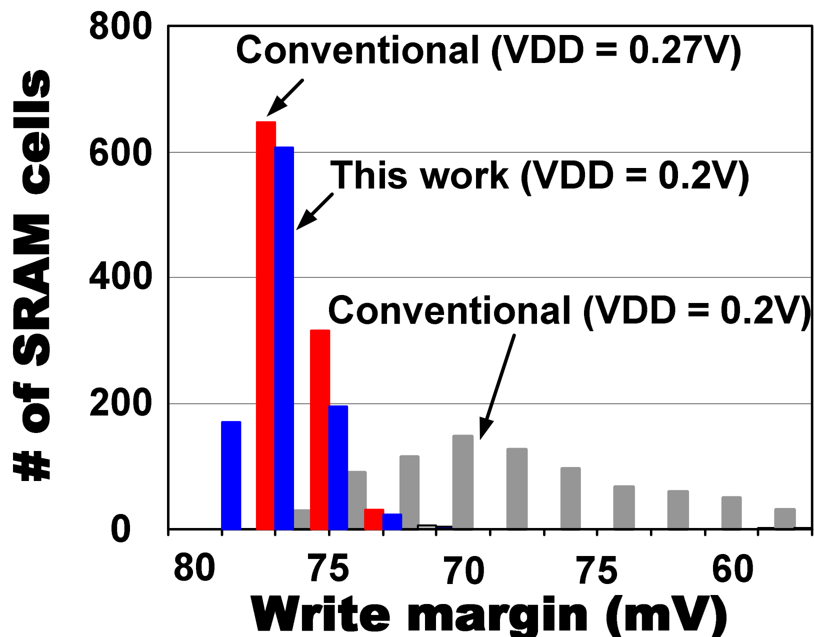
Write Power Comparison

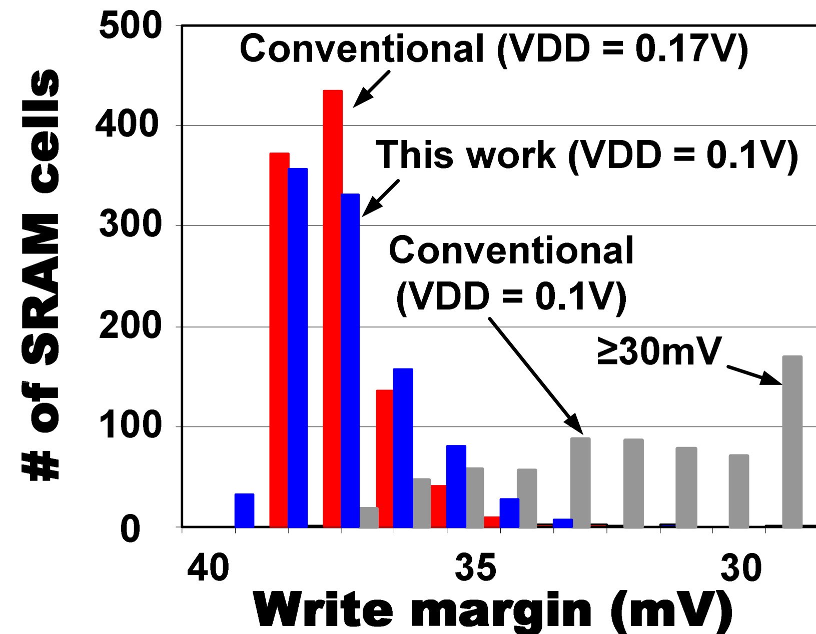




- **No change in write bitline power**
  - Longer channel length does not increase junction capacitance
- **20% reduction in wordline driver power**
  - $(1.45 \times 0.2^2)/(1 \times 0.27^2) = 0.80$

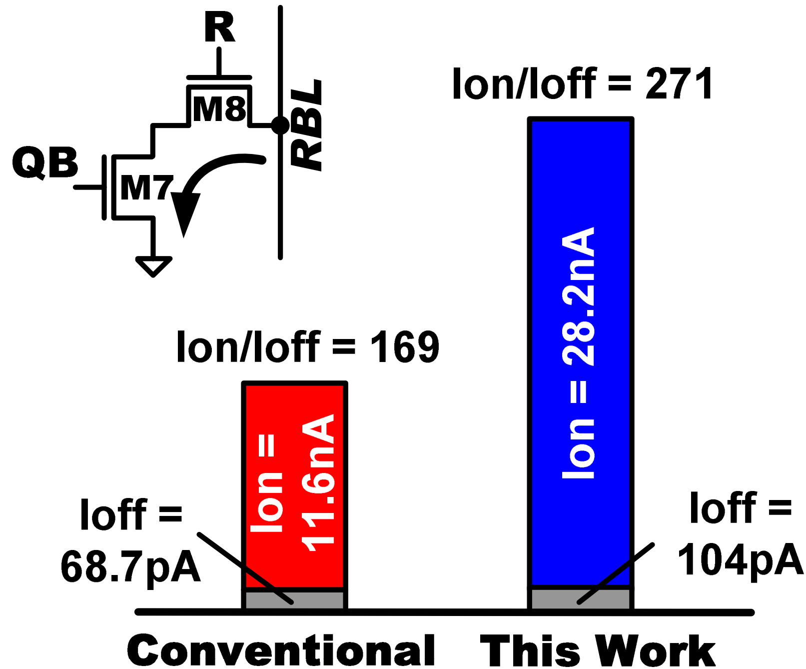
Impact of Random Dopant Fluctuations on Write Margin

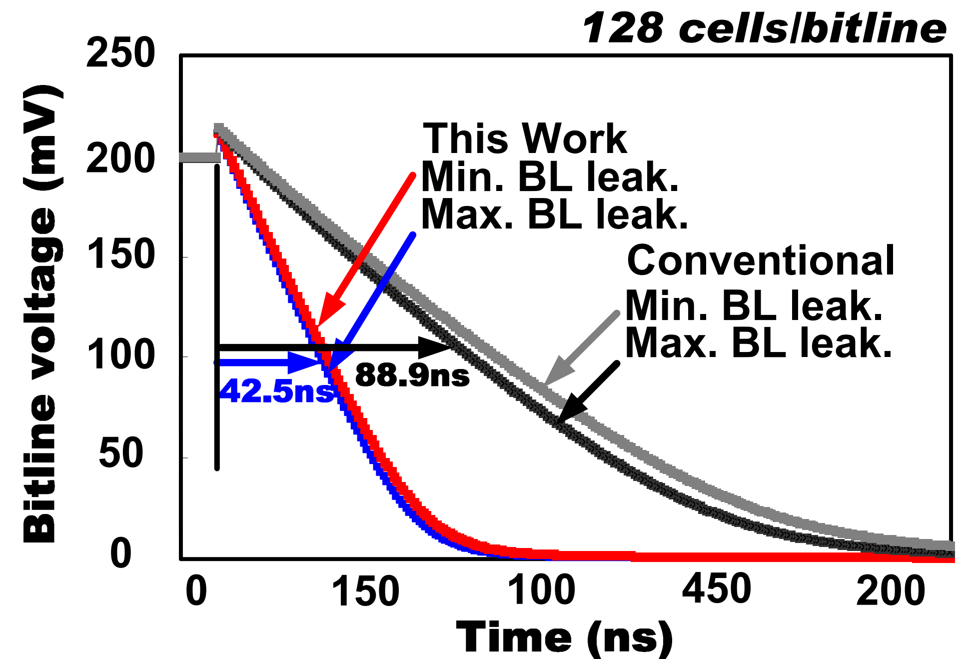




- 44% smaller σ/μ in write margin distribution due to larger device size
- Larger write margin & narrower distribution at fixed VDD

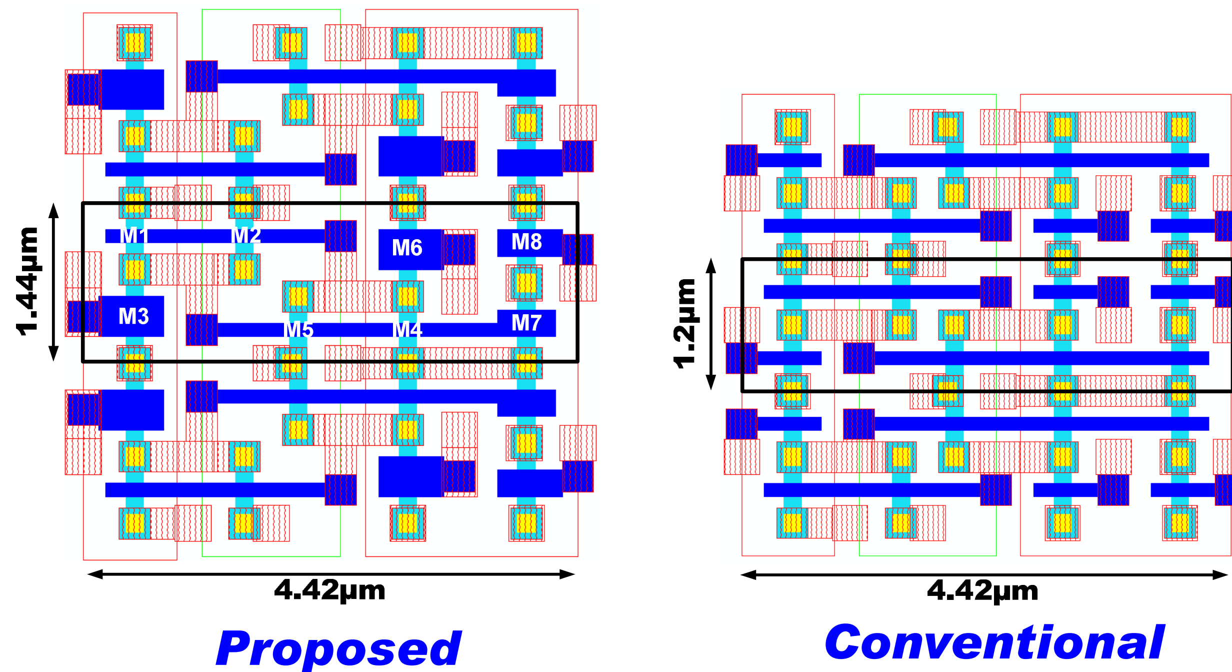
Simulation Results of Ion-to-Ioff Ratio and Read Performance





- Bitline Ion-to-Ioff ratio improves from 169 to 271
- Also improves read performance by 52%

SRAM Cell Layout Comparison



Transistors	M1, M4	M3. M6	M7, M8	M2, M5
Width/ Length	0.16µm/ 0.12µm	0.16µm/ 0.36µm	0.16µm/ 0.24µm	0.16µm/ 0.12µm
Type	NMOS	NMOS	NMOS	PMOS

- 0.13µm process technology
- 20% area overhead: 0.36µm in write port and 0.24µm in read port

Conclusions

- RSCE utilized for subthreshold 8T SRAM cells
- Proposed sizing scheme increases current drivability leading to better write margin
  - 160mV improvement in write margin
  - Equivalent to boosting write wordline voltage by 35%
- 44% smaller σ/μ in write margin distribution due to larger device area
- Improved Ion-to-Ioff ratio and read performance
  - Bitline Ion-to-Ioff improved from 169 to 271
  - Read performance improved by 52%