An 8T Subthreshold SRAM Cell Utilizing Reverse Short Channel Effect for Write Margin and Read Performance Improvement

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***Abstract*-We propose a technique for improving write margin and read performance of 8T subthreshold SRAMs by using long channel devices to utilize the pronounced reverse short channel effect. Simulations show that the proposed cell at 0.2V has a write margin equivalent to a conventional cell at 0.27V. The Ion-to-Ioff ratio of the read path also improved from 169 to 271 and a 52% speedup for read was achieved. The cell area overhead was 20%.**

I. Introduction

Subthreshold logics are becoming increasingly popular for ultra-low power applications such as portable electronics, medical instrumentations, and sensor networks where minimal power consumption is the primary design constraint [1][2]. Subthreshold logic can operate while consuming orders of magnitude less power than in the normal strong-inversion region. Characteristics of MOS transistors in the subthreshold region are significantly different from those in the strong-inversion region. The MOS saturation current becomes an exponential function of the terminal voltages in this regime leading to an exponential increase in MOS current variability under Process-Voltage-Temperature (PVT) fluctuations. Designing robust SRAM memories in the subthreshold region is a particularly challenging task due to the small Ion-to-Ioff ratio and the increased current variability. Reduced read margin, small write margin, and increased speed/power variations are the main design challenges for subthreshold SRAMs.

SRAM read stability is already a problem in conventional 6T cells in the strong inversion region as the access transistor can considerably raise the internal node voltage that stores a '0' so as to trip the cell data. This problem worsens in the subthreshold region as the current variability increases. A widely used method for improving the Static Noise Margin (SNM) in subthreshold SRAMs is decoupling the cell node from bitline by using additional read path transistors [3][4]. By doing so, the SNM in read mode becomes equal to that in hold mode. The write margin problem is exacerbated in subthreshold due to the increased current sensitivity to PVT variations. A higher wordline voltage was used in [4] to strengthen the write path and overcome the impact of variations at the cost of additional power routing/generation circuits and increased power consumption. Other previous methods used a collapsed cell supply voltage during write operation to weaken the strength of the pull up PMOS.

This paper presents a new technique for improving the write margin and read performance of 8T subthreshold SRAMs without requiring any additional supply voltage or extra circuitry. We utilize the pronounced Reverse Short Channel Effect (RSCE) [5][6][7] in the subthreshold region to increase the strength of write access devices. By simply using longer channel length access devices, the threshold voltage is reduced and the current drivability is improved due to the exponential dependency of current on threshold voltage. Similarly, the read path delay and variation tolerance was also improved by deploying longer channel length devices that utilize the RSCE.

II. Conventional 8T SRAM Cell

Fig. 1 shows the conventional 8T SRAM cell. It contains separate read and write paths with respective wordline signals WWL and RWL. Read port consists of two transistors (M7, M8) and write port includes two transistors (M3, M6). To improve the read stability, cell nodes are decoupled from the read bitline (RBL) via read devices M7 and M8. When read wordline (RWL) is enabled, the read bitline (RBL) is conditionally discharged based on the cell data. Because the cell nodes are decoupled from the RBL, this design maximizes the read stability.

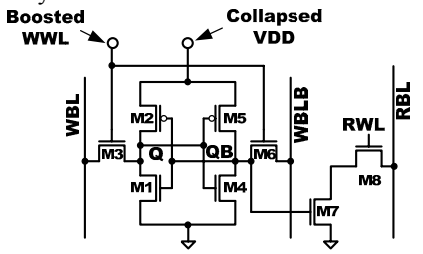


Figure 1. Conventional write margin improvement techniques for 8T SRAMs.

Write operation is executed by enabling the write wordline (WWL) after loading the data onto the write bitlines (WBL, WBLB). The current ratio between the write access transistors (M3, M6) and the pull-up transistors (M2, M5) determines the cell write margin. If the strength of the write access transistor is too weak to pull down the node voltage storing a '1' close to GND, the write operation will fail. To prevent the write failure, strong access transistors are needed to increase the write path strength. However, in the subthreshold region, sizing alone cannot solve the write margin problem due to the large process variation and area overhead. Several techniques have been proposed to improve the write margin. A higher wordline voltage has been applied to the write access transistors (M3, M6) to increase the current drivability [4]. This improves the write margin at the cost of additional power routing, extra voltage generation circuitry and increased power consumption. Another widely used method is collapsing the cell supply voltage to weaken the strength of PMOS during the write operation. However, the collapsed supply voltage deteriorates the stability of other SRAM cells which are not supposed to be written but are connected to the same bitline or wordline. The cell stability is already close to the failure point

in subthreshold SRAMs which makes the collapsed supply voltage scheme difficult to be used.

III. Proposed Subthreshold SRAM Cell Design

A. Impact of Reverse Short Channel Effect in Subthreshold

As process technology scales, V_{th} roll-off caused by Drain Induced Barrier Lowering (DIBL) becomes stronger. To compensate for the strong DIBL, non-uniform doping called HALO implants is used in the source-body and drain-body boundaries to reduce the amount of control the drain has over the channel. However, as a byproduct of using HALO implants, the threshold voltage decreases as the channel length increases, which is also referred to as the RSCE [8]. RSCE is not a major concern in conventional superthreshold designs since DIBL has a stronger impact in the minimum channel length devices used in digital circuits. However, in the subthreshold region, the RSCE effect becomes pronounced due to the significantly reduced DIBL effect. This causes the V_{th} to decrease monotonically with channel length which results in an exponential increase in device current. Increasing the channel length does not increase the device junction capacitance which is the main contributor to circuit power consumption. Fig. 2 illustrates the channel length dependency of the normalized V_{th} and current-per-width. In a 0.13µm CMOS process technology, a channel length of 0.36µm offers a 3.3X increase in current drivability.

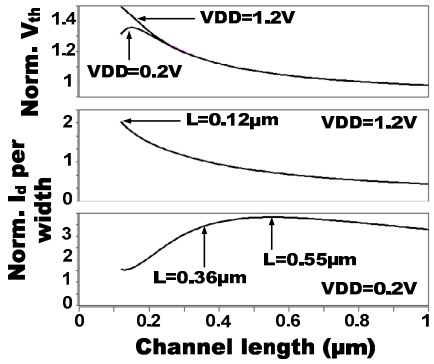


Figure 2. Dependency of normalized V_{th} and current-per-width on channel length.

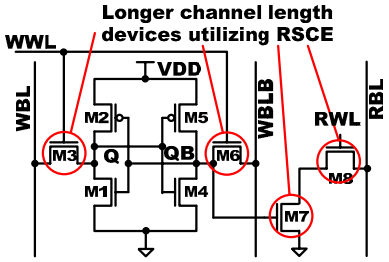


Figure 3. Proposed 8T SRAM cell utilizing RSCE.

B. Proposed 8T SRAM Cell Utilizing RSCE

Fig. 3 shows the proposed 8T SRAM cell utilizing the strong RSCE. The basic operation is identical to the conventional 8T SRAM cell except that longer channel length devices are used for the write access transistors (M3, M6) and the read path devices (M7, M8). The longer channel length devices in the write port increase the write path current drivability by 3.3X due to the reduced threshold voltage and the exponential increase in drive current. This is equivalent to applying a 70mV higher write wordline voltage at a nominal supply voltage of 0.2V. The read current and its process tolerance are also improved by using a longer channel length device for M7 and M8. The following sections describe the key benefits of the proposed cell sizing scheme in further detail.

C. Write Margin Improvement

Fig. 4 shows the write margin metric used in this paper. To emulate the worst case write condition, QB is connected to GND to increase the M2 current as shown in Fig. 4(a). The voltage difference between the trip point of latch and the cell node which is written with '0' is used as the write margin metric. If the cell node voltage is lower than the trip point of the latch, it has a positive write margin, which represents a correct write '0' operation. On the other hand, if the cell node voltage is higher than the trip point, it has a negative write margin, which means that the write operation failed.

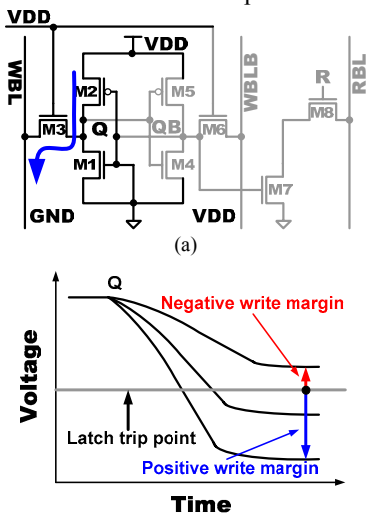
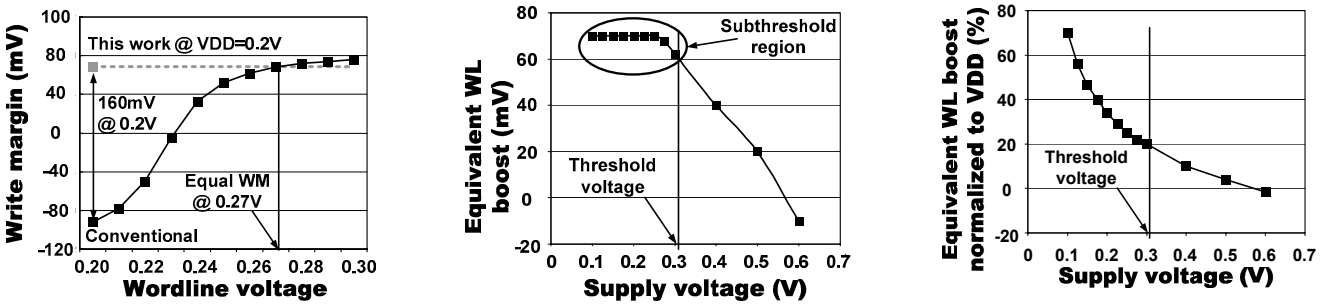


Figure 4. Write margin metric used in this paper: (a) simulation setup, (b) write margin definition

Fig. 5 shows the write margin simulation results for different supply voltages. Fast PMOS and slow NMOS process parameters were used to represent the worst case write condition. All devices have a minimum channel width. A negative write margin in Fig. 5(a) indicates a write failure. Using a channel length of 0.36µm for M3 and M6, the write margin of the proposed SRAM cell is improved from -90mV to 70mV at 0.2V. Fig. 5(b) illustrates the wordline boost required for a conventional SRAM cell to obtain a write margin equivalent to the proposed scheme. Here, we refer to an 8T cell using all minimum channel length and minimum width devices as the conventional scheme. It can be seen that the equivalent wordline boost is highest in the subthreshold operation region indicating that the proposed sizing method becomes more effective at lower supply voltages. The equivalent wordline boost normalized to the supply voltage in



(a) (b) (c)

Figure 5. Write margin improvement using long channel access devices: (a) write margin versus wordline voltage, (b) equivalent wordline boost, (c) equivalent wordline boost normalized to VDD

Fig. 5(c) also increases at lower supply voltages, which illustrates the usefulness of the proposed technique. Fig. 6 shows the simulated waveforms showing the cell node voltages during a write operation. Unlike the proposed cell, it can be seen that the conventional scheme at 0.2V suffers from the poor writability.

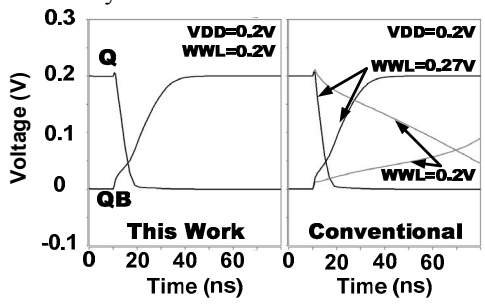
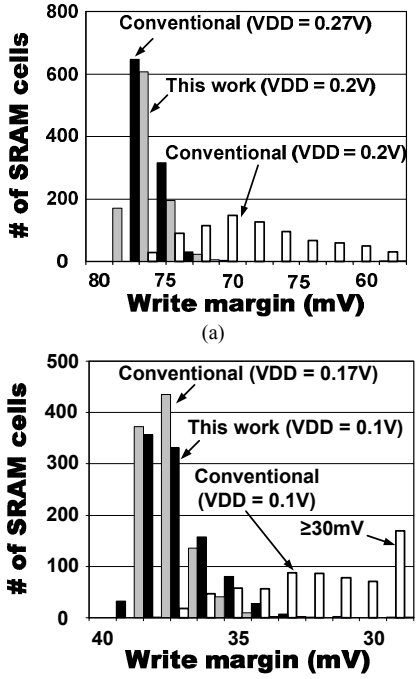


Figure 6. Simulated waveforms during write operation

D. Write Power Comparison

Power consumption during write operation mainly comes from the bitline and the wordline switching power. Wire capacitance and device junction capacitance compose the total bitline capacitance. The bitline junction capacitance is proportional to the width of write access devices. The proposed SRAM cell increases the channel length to improve the current drivability, which has no impact on the junction capacitance. Therefore, the power dissipated for charging and discharging the write bitlines does not change. Although the threshold voltage is lower for the longer channel access transistors, the improved subthreshold slope (87mV/dec → 71mV/dec) [8] results in a modest 5% increase in write bitline leakage current. Another source of power dissipation is the wordline switching power. By increasing the channel length from 0.12μm to 0.36μm, the total gate capacitance increases by 90% due to the combined effect of the increased gate area and other secondary behaviors [8]. However, the impact of the increased gate area becomes smaller due to the wire capacitance component of the wordline. In our design, the total wordline capacitance is increased by 45% at 0.2V. Compared to the conventional cell operating at 0.27V to obtain the same write margin, the power consumption of the wordline driver in the proposed SRAM cell is reduced by 20%. 128 cells are used in the rows and columns for the power simulation. Additional power reduction is expected by removing extra circuitry needed for generating and routing the higher supply voltage.



(a)

(b)

Figure 7. Write margin distribution of proposed and conventional SRAM cell: (a) VDD=0.2V, (b) VDD=0.1V

E. Impact of Random Dopant Fluctuation on Writability

Random Dopant Fluctuations (RDF) cause parameter mismatches even between devices with identical layout in close proximity [9]. The impact of RDF is more severe in the subthreshold region due to the exponential relationship between the current and threshold voltage [2]. The standard deviation (σ) of the threshold voltage distribution is known to be proportional to $(WL)^{-1/2}$ [10] where W is the device width and L is the channel length. The gate area of the access transistors M3 and M6 utilizing RSCE is $0.072\mu m^2$ (=0.2μm×0.36μm) which is 2X larger than the minimum size access transistors in conventional 8T SRAMs. This translates into a 58% smaller standard deviation in the threshold voltage reducing the write margin variability in the proposed SRAM cell. Fig. 7 shows Monte Carlo simulation results of the write margin at two different supply voltages. It is assumed that each device in the 8T SRAM has independent threshold

voltages which follow a normal distribution. Results are shown for a conventional SRAM cell at a nominal and a 70mV higher supply voltage. The average and the standard deviation of of the proposed cell's write margin are 79mV and 1.4mV, respectively, which are much better than those of the conventional cell (65mV and 15mV) at 0.2V.

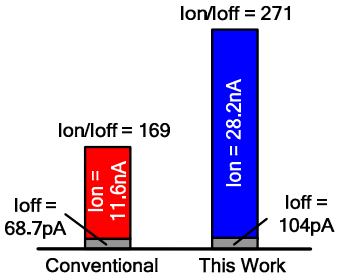


Figure 8. SRAM read port Ion-to-Ioff ratio comparison

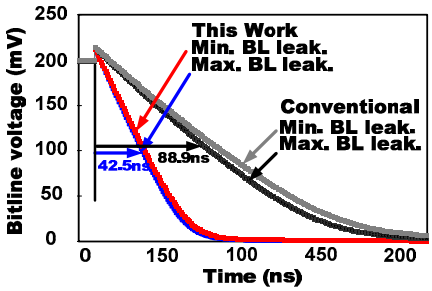
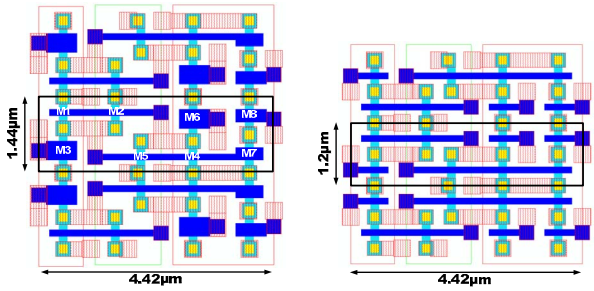


Figure 9. Bitline discharging speed comparison



(a) This work (b) Conventional

Transistors	M1, M4	M3. M6	M7, M8	M2, M5
Width/ Length	0.16mm/ 0.12mm	0.16mm/ 0.36mm	0.16mm/ 0.24mm	0.16mm/ 0.12mm
Type	NMOS	NMOS	NMOS	PMOS

Figure 10. Proposed and conventional 8T SRAM cell layout comparison

F. Read Bitline Sensitivity Improvement

2X longer channel length devices are also used in the SRAM read port to increase the current drivability. M7 and M8 in Fig. 3 have a channel length of 0.24µm, which improves read current from 11.6µA to 28.2nA. Further increase in channel length will further improve the current drivability but this comes at an added cell area penalty. Owing to the steeper subthreshold swing in longer channel devices, the Ion-to-Ioff ratio improves from 169 to 271 as shown in Fig. 8. The increased current drivability reduces the read bitline discharge time improving the read performance. Fig. 9 shows the bitline discharging speed comparison for the proposed and conventional SRAM. Two different column data patterns generating maximum and minimum bitline leakage currents are tested on a 32 cell column slice. The read delay is improved from 88.9ns to 42.5ns and shows less variation for the different column data patterns.

G. SRAM Cell Layout

Fig. 10 shows the layout of the proposed and conventional 8T SRAM cells in a 0.13µm CMOS process. The write access transistors and the read path devices in the proposed cell have longer channel lengths. SRAM cell area was 4.42µm × 1.44µm which is 20% larger than the conventional 8T SRAM cell with minimum length and minimum width devices.

IV. Conclusions

We propose an 8T subthreshold SRAM cell with improved write margin, better variation tolerance and increased Ion-to-Ioff ratio in the read port. Process scaling makes RSCE stronger due to the increased HALO doping used to negate the short channel effect. In the subthreshold region, RSCE has an even stronger impact on device behavior because of the reduced DIBL and the exponential relationship between the threshold voltage and weak-inversion current. Due to this effect, minimum channel length is not the optimal point for maximum performance in the subthreshold region. To enhance the SRAM cell writability, we use a 3X longer channel length (0.36µm) in the write access transistors to strengthen the current drivability. The proposed SRAM cell at 0.2V achieves nearly the same write margin as a conventional SRAM cell with a 70mV higher wordline voltage. No additional supply voltages or circuitry are needed. Utilizing RSCE in the read port increases the Ion-to-Ioff ratio from 169 to 271 and offers a 52% speedup in read bitline discharge time. The SRAM cell area overhead was 20%.

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