Homework # 6

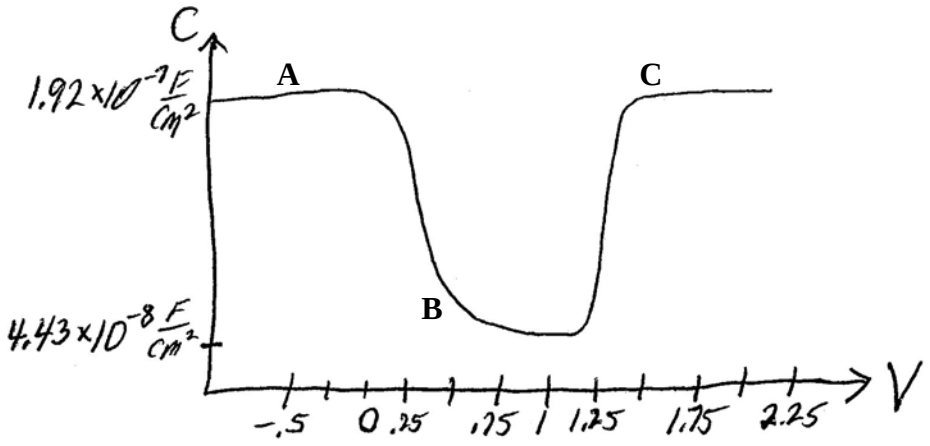
EE 3161 - Spring 2008

Due Wednesday, April 30 in class

1) Problem 16.7 of Pierret.

2) For the following C-V diagram, assume that the measurement frequency is 100 kHz and that the device is silicon-based.

a) What is the oxide thickness?
b) What is V_T?
c) What is the depletion width at threshold?
d) What is the substrate doping?
e) Is this C-V curve for a MOS capacitor or a MOS transistor? Why?
f) Draw the charge vs. x and the electric field vs. x for regions A, B, and C, where x is the depth into the MOS system. (Let x=0 be the metal-oxide interface.)



3) Consider an ideal silicon MOS capacitor with a substrate doped at $N_a = 5\times10^{16}$ cm^{-3} and an oxide thickness of 300Å.

a) Draw the C-V curve.
b) How would this C-V curve change if somehow the semiconductor were changed to GaAs but all else remained constant? (Redraw the curve.)
c) How would it change if the oxide thickness were doubled? (Redraw the curve.)

4) Problem 17.2 of Pierret, parts a) to f) only.